HB56A472E Series

4,194,304-word × 72-bit High Density Dynamic RAM Module

HITACHI

Description

The HB56A472E belongs to 8 Byte DIMM (Dual In-line Memory Module) family, and has been developed as an optimized main memory solution for 4- and 8-byte processor applications. The HB56A472E is a 4 M × 72 dynamic RAM module, mounted 18 pieces of 16-Mbit DRAM (HM5116400BTS) sealed in TSOP package and 2 pieces of 16-bit BiCMOS line driver (74ABT16244) sealed in TSSOP package. An outline of the HB56A472E is 168-pin socket type package (dual lead out). Therefore, the HB56A472E makes high density mounting possible without surface mount technology. The HB56A472E provides common data inputs and outputs. Decoupling capacitors are mounted beside each TSOP on the module board.

Features

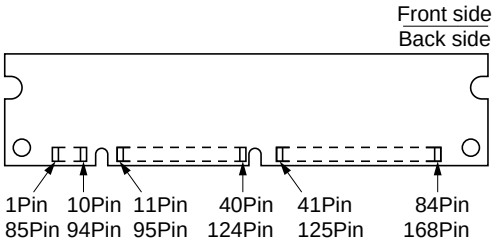
- 168-pin socket type package (dual lead out)
  - Lead pitch: 1.27 mm
- Single 5 V (± 5%) supply
- High speed
  - Access time: t_{RAC} = 60/70/80 ns (max)
  - Access time: t_{CAC} = 20/23/25 ns (max)
- Low power dissipation
  - Active mode: 7.90/6.95/6.48 W (max)
  - Standby mode (TTL): 525 mW (max)
  - Standby mode (CMOS): 431 mW (max)
- Buffered inputs except $\overline{RAS}$ and DQ
- 4 Byte interleave enabled, dual address inputs (A0/B0)
- Fast page mode capability
- 4,096 refresh cycle: 64 ms
- 2 variations of refresh
  - $\overline{RAS}$-only refresh
  - $\overline{CAS}$-before-$\overline{RAS}$ refresh
- TTL compatible

Datasheet Title

Ordering Information

Type No.	Access Time	Package	Contact Pad
HB56A472E-6B	60 ns	168-pin dual lead out socket type	Gold
HB56A472E-7B	70 ns	168-pin dual lead out socket type	Gold
HB56A472E-8B	80 ns	168-pin dual lead out socket type	Gold

Pin Arrangement



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	16	DQ12	31	$\overline{OE0}$	46	$\overline{CE4}$
2	DQ0	17	DQ13	32	V_{SS}	47	NC
3	DQ1	18	V_{CC}	33	A0	48	$\overline{WE2}$
4	DQ2	19	DQ14	34	A2	49	V_{CC}
5	DQ3	20	DQ15	35	A4	50	NC
6	V_{CC}	21	DQ16	36	A6	51	NC
7	DQ4	22	DQ17	37	A8	52	DQ18
8	DQ5	23	V_{SS}	38	A10	53	DQ19
9	DQ6	24	NC	39	NC	54	V_{SS}
10	DQ7	25	NC	40	V_{CC}	55	DQ20
11	DQ8	26	V_{CC}	41	NC	56	DQ21
12	V_{SS}	27	$\overline{WE0}$	42	NC	57	DQ22
13	DQ9	28	$\overline{CE0}$	43	V_{SS}	58	DQ23
14	DQ10	29	NC	44	$\overline{OE2}$	59	V_{CC}
15	DQ11	30	$\overline{RE0}$	45	$\overline{RE2}$	60	DQ24

Pin Arrangement (cont)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
61	NC	88	DQ38	115	NC	142	DQ59
62	NC	89	DQ39	116	V_{SS}	143	V_{CC}
63	NC	90	V_{CC}	117	A1	144	DQ60
64	NC	91	DQ40	118	A3	145	NC
65	DQ25	92	DQ41	119	A5	146	NC
66	DQ26	93	DQ42	120	A7	147	NC
67	DQ27	94	DQ43	121	A9	148	NC
68	V_{SS}	95	DQ44	122	A11	149	DQ61
69	DQ28	96	V_{SS}	123	NC	150	DQ62
70	DQ29	97	DQ45	124	V_{CC}	151	DQ63
71	DQ30	98	DQ46	125	NC	152	V_{SS}
72	DQ31	99	DQ47	126	B0	153	DQ64
73	V_{CC}	100	DQ48	127	V_{SS}	154	DQ65
74	DQ32	101	DQ49	128	NC	155	DQ66
75	DQ33	102	V_{CC}	129	NC	156	DQ67
76	DQ34	103	DQ50	130	NC	157	V_{CC}
77	DQ35	104	DQ51	131	NC	158	DQ68
78	V_{SS}	105	DQ52	132	$\overline{PDE}$	159	DQ69
79	PD1	106	DQ53	133	V_{CC}	160D	DQ70
80	PD3	107	V_{SS}	134	NC	161	DQ71
81	PD5	108	NC	135	NC	162	V_{SS}
82	PD7	109	NC	136	DQ54	163	PD2
83	ID0 (V_{SS})	110	V_{CC}	137	DQ55	164	PD4
84	V_{CC}	111	NC	138	V_{SS}	165	PD6
85	V_{SS}	112	NC	139	DQ56	166	PD8
86	DQ36	113	NC	140	DQ57	167	ID1 (V_{SS})
87	DQ37	114	NC	141	DQ58	168	V_{CC}

Pin Description

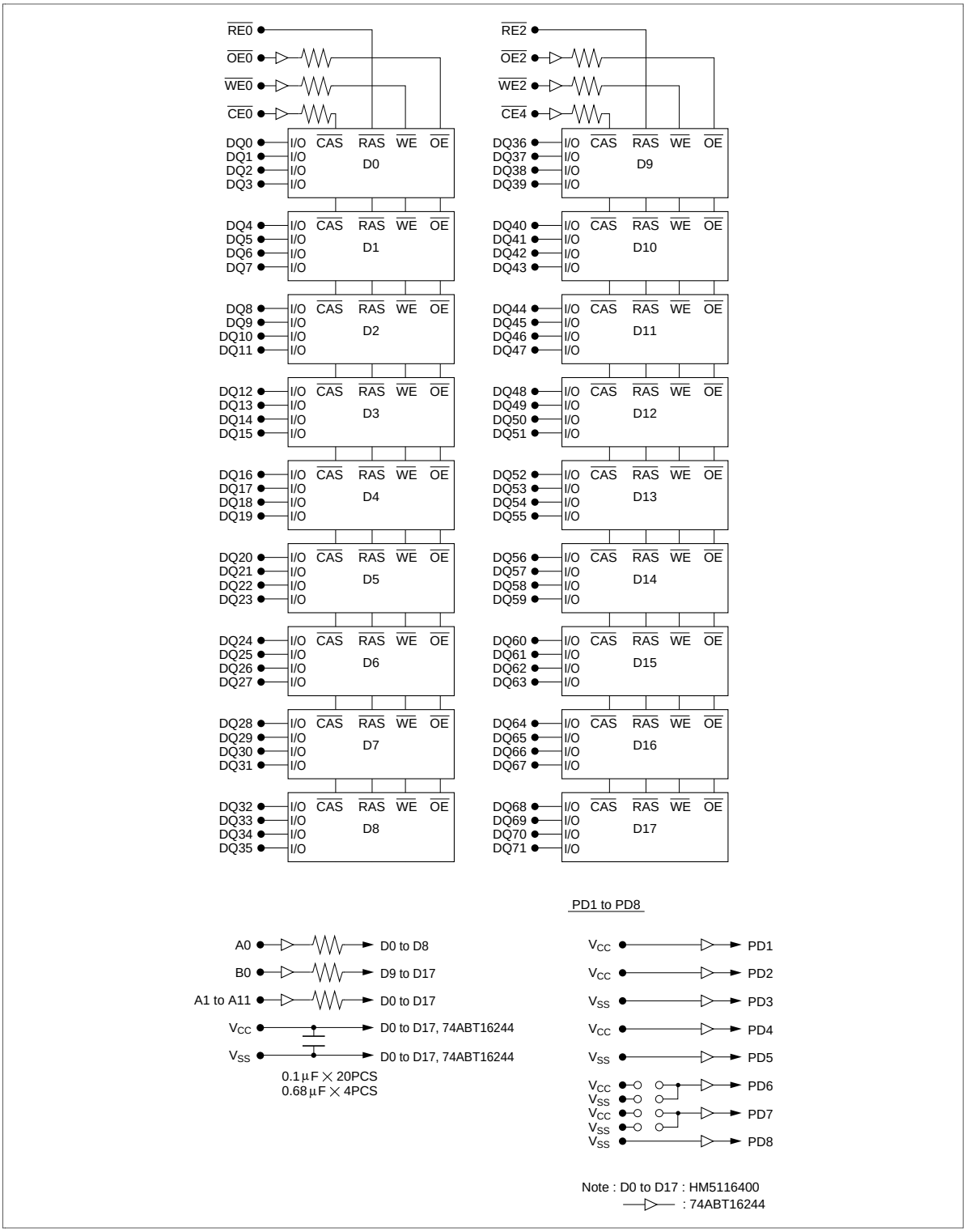
Pin Name	Function
A0–A11, B0	Address input: A0–A11, B0 Row address: A0–A11, B0 Column address: A0–A9, B0 Refresh address: A0–A11, B0
DQ0–DQ71	Data-in/Data-out
$\overline{RE0}$, $\overline{RE2}$	Row address strobe ($\overline{RAS}$)
$\overline{CE0}$, $\overline{CE4}$	Column address strobe ($\overline{CAS}$)
$\overline{WE0}$, $\overline{WE2}$	Read/write enable
$\overline{OE0}$, $\overline{OE2}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground
PD1–PD8	Presence detect
ID0, ID1	ID bit
$\overline{PDE}$	Presence detect enable
NC	No connection

Presence Detect Pin Assignment

		$\overline{PDE}$ = Low			$\overline{PDE}$ = High
Pin Name	**Pin No.**	**60 ns**	**70 ns**	**80 ns**	**All**
PD1	79	1	1	1	High-Z
PD2	163	1	1	1	High-Z
PD3	80	0	0	0	High-Z
PD4	164	1	1	1	High-Z
PD5	81	0	0	0	High-Z
PD6	165	1	0	1	High-Z
PD7	82	1	1	0	High-Z
PD8	166	0	0	0	High-Z

Note: 1: High level (driver output)
0: Low level (driver output)

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–0.5 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	–0.5 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	19	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	–0.5	—	0.8	V	1

Note: 1. All voltage referred to V_{SS}

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V)

		HB56A472E								
		60 ns		70 ns		80 ns				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**	**Notes**
Operating current	I_{CC1}	—	1504	—	1324	—	1234	mA	t_{RC} = min	1,2
Standby current	I_{CC2}	—	100	—	100	—	100	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	82	—	82	—	82	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC}-0.2 V Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	1504	—	1324	—	1234	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	154	—	154	—	154	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	1504	—	1324	—	1234	mA	t_{RC} = min	
Fast page mode current	I_{CC7}	—	1324	—	1144	—	964	mA	t_{PC} = min	1, 3
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 5.5 V	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	0 V ≤ Vout ≤ 5.5 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V_{CC}	2.4	V	High Iout = –5.0 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 5%)

Parameter	**Symbol**	**Typ**	**Max**	**Unit**	**Notes**
Input capacitance (Address)	C_{I1}	—	20	pF	1
Input capacitance ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{I2}	—	20	pF	1
Input capacitance ($\overline{RAS}$)	C_{I3}	—	78	pF	1
I/O capacitance (DQ)	$C_{I/O}$	—	20	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to 70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V)[*1, *2, *18]

Test Conditions

- Input rise and fall time: 5 ns
- Input timing reference levels: 0.8 V, 2.4 V
- Output load: 2 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write, and Refresh Cycles (Common parameters)

		HB56A472E							
		60 ns		70 ns		80 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Random read or write cycle time	t_{RC}	110	—	130	—	150	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	40	—	50	—	60	—	ns	
$\overline{CAS}$ precharge	t_{CP}	10	—	10	—	10	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	80	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10000	18	10000	20	10000	ns	
Row address setup time	t_{ASR}	5	—	5	—	5	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	10	—	15	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	47	20	55	ns	3
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	ns	4
$\overline{RAS}$ hold time	t_{RSH}	20	—	23	—	25	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	60	—	70	—	80	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	ns	
$\overline{OE}$ to Din delay time	t_{OED}	20	—	23	—	25	—	ns	5
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	0	—	ns	6
$\overline{CAS}$ delay time from Din	t_{DZC}	0	—	0	—	0	—	ns	6
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	7
Refresh period	t_{REF}	—	64	—	64	—	64	ms	19

Read Cycle

		HB56A472E							
		60 ns		70 ns		80 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Access time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	ns	8, 19
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	23	—	25	ns	9, 10, 17
Access time from address	t_{AA}	—	35	—	40	—	45	ns	9, 11, 17
Access time from $\overline{OE}$	t_{OEA}	—	20	—	23	—	25	ns	9
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	12
Read command hold time to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	12
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	40	—	45	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	30	—	35	—	40	—	ns	
$\overline{CAS}$ to output in low-Z	t_{CLZ}	2	—	2	—	2	—	ns	
Output data hold time	t_{OH}	3	—	3	—	3	—	ns	
Output data hold time from $\overline{OE}$	t_{OHO}	3	—	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	20	—	20	—	20	ns	13
Output buffer turn-off to $\overline{OE}$	t_{OEZ}	—	20	—	20	—	20	ns	13
$\overline{CAS}$ to Din delay time	t_{CDD}	20	—	23	—	25	—	ns	5

Write Cycle

		HB56A472E							
		60 ns		70 ns		80 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	14
Write command hold time	t_{WCH}	10	—	15	—	15	—	ns	
Write command pulse width	t_{WP}	10	—	10	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	23	—	25	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	—	18	—	20	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	15
Data-in hold time	t_{DH}	15	—	20	—	20	—	ns	15

Read-Modify-Write Cycle

		HB56A472E							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	t_{RWC}	155	—	181	—	205	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	90	—	103	—	115	—	ns	14
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	40	—	46	—	50	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	55	—	63	—	70	—	ns	14
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	15	—	18	—	20	—	ns	

Refresh Cycle

		HB56A472E							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	10	—	10	—	10	—	ns	
$\overline{WE}$ setup time (CBR refresh cycle)	t_{WRP}	5	—	5	—	5	—	ns	
$\overline{WE}$ hold time (CBR refresh cycle)	t_{WRH}	10	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	0	—	0	—	0	—	ns	

Fast Page Mode Cycle

		HB56A472E							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Fast page mode cycle time	t_{PC}	40	—	45	—	50	—	ns	
Fast page mode $\overline{RAS}$ pulse width	t_{RASP}	—	100000	—	100000	—	100000	ns	16
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	40	—	45	—	50	ns	9, 17
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{CPRH}	40	—	45	—	50	—	ns	

Fast Page Mode Read-Modify-Write Cycle

		HB56A472E							
		60 ns		70 ns		80 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Fast page mode read-modify-write cycle time	t_{PRWC}	85	—	96	—	105	—	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	t_{CPW}	60	—	68	—	75	—	ns	14

Notes:
1. AC measurements assume t_T = 5 ns.
2. An initial pause of 200 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-only refresh or $\overline{CAS}$-before-$\overline{RAS}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
5. Either t_{OED} or t_{CDD} must be satisfied.
6. Either t_{DZO} or t_{DZC} must be satisfied.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
8. Assumes that $t_{RCD} < t_{RCD}$ (max) and $t_{RAD} < t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
9. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
10. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max)
11. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
13. t_{OFF} (max) and t_{OEZ} (max) are defined the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
14. t_{WCS}, t_{RWD}, $t_{CWD,}$ t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), or $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. These parameters are referred to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycle.
16. t_{RASP} defines $\overline{RAS}$ pulse width in fast page mode cycles.
17. Access time is determined by the longest among t_{AA}, t_{CAC} and t_{CPA}.
18. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device. After $\overline{RAS}$ is reset, if $t_{OEH} \geq t_{CWL}$, the DQ pins will remain open circuit (high impedance); if $t_{OEH} \leq t_{CWL}$, invalid data will be out at each DQ.
19. t_{REF} is determined by 4,096 refresh cycle.

Timing Waveforms

Refer to the HM5116400B Series data sheet.

Physical Outline

Unit: mm/inch