Winbond Electronics Corp.

128K × 36 PIPELINED ZWS SRAM

GENERAL DESCRIPTION

The W25Z040A is a high-speed, low-power, Zero-Wait-State (ZWS) Synchronous Pipelined CMOS Static RAM organized as 131,072 × 36 bits. A built-in two-bit burst address counter supports both Linear and Interleaved burst mode. The mode to be executed is controlled by the $\overline{LBO}$ pin. A snooze mode can reduce the power dissipation.

The ZWS SRAM is optimized for 100 percent bus utilization by eliminating wait states when transitioning from read to write, or vice versa. All addresses, data inputs, clock enable ($\overline{CLKE}$), write enable ($\overline{WE}$), byte-write enables ($\overline{BW}$ [4:1]) and chip enables ($\overline{CE1}$, CE2 and $\overline{CE3}$ for easy depth expansion) are synchronously sampled with by a positive-edge-triggered clock (CLK). Asynchronous inputs include the output enable ($\overline{OE}$), clock (CLK) and snooze (ZZ).

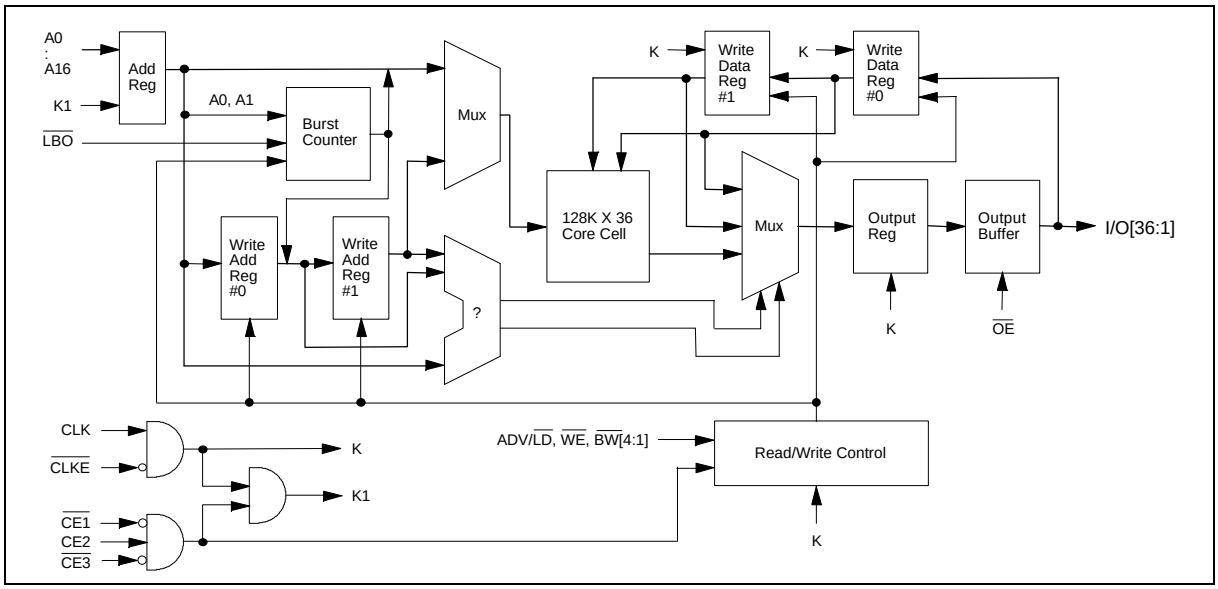
To provide 100 percent use of the data bus, the pipelined ZWS SRAM uses the two-stage write address registers. For example, when the address and control signals are applied to the SRAM in clock cycle one, the data associated with the address occurs two cycles later, or the clock cycle three.

The W25Z040A operates on a single 3.3V power supply, with all inputs and outputs compatible with the LVTTL interface. Based on the bus efficiency, the device is ideal for high bandwidth application systems.

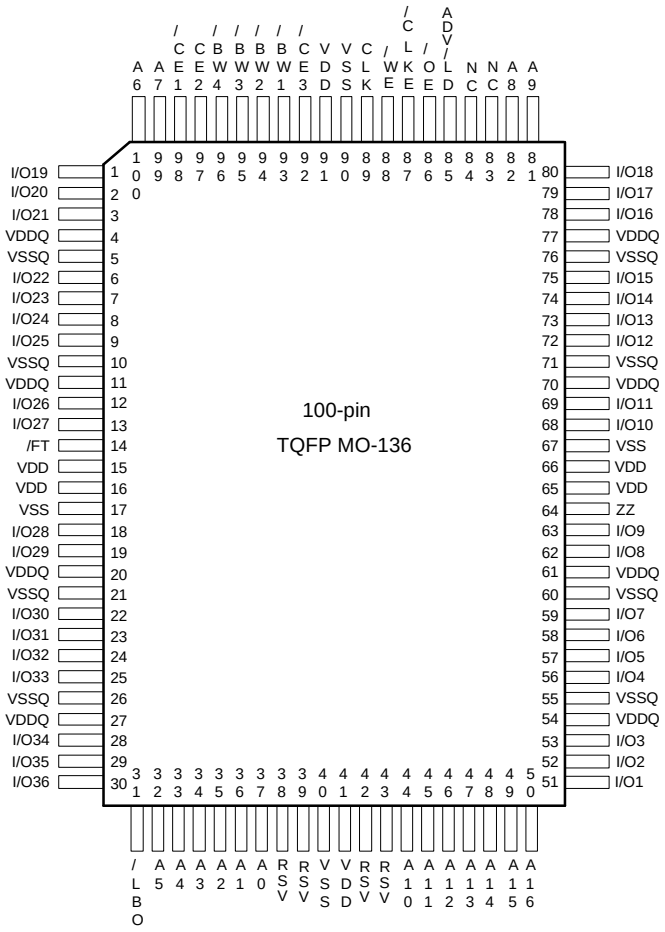
FEATURES

- Synchronous operation
- High-speed access time: 3.8/4.2/4.5/5 nS
- Single +3.3V power supply
- Individual byte write capability
- 3.3V LVTTL compatible I/O
- Clock-controlled and registered input
- Asynchronous output enable
- Zero wait states between read/write cycles
- Supports snooze mode (low-power state)
- Internal burst counter supports Interleaved burst mode & linear burst mode
- Packaged in 100-pin TQFP

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	TYPE	DESCRIPTION
A0–A16	Input, Synchronous	Host Address
I/O1–I/O36	I/O, Synchronous	Data Inputs/Outputs
CLK	Input, Clock	Processor Host Bus Clock
$\overline{CLKE}$	Input, Synchronous	Clock Enable
$\overline{CE1}$, CE2, $\overline{CE3}$	Input, Synchronous	Chip Enables
$\overline{WE}$	Input, Synchronous	Write Enable from System Controller
$\overline{BW1}$ – $\overline{BW4}$	Input, Synchronous	Host Bus Byte Enables used with $\overline{WE}$
$\overline{OE}$	Input, Asynchronous	Output Enable Input
ADV/$\overline{LD}$	Input, Synchronous	Internal Burst Address Counter Advance(Sampled High) / Load External Address (Sampled Low)
ZZ	Input, Asynchronous	Snooze Pin for Low-power State, internally pulled low
$\overline{FT}$	Input, Static	This pin should be connected to V_{DD} or unconnected to meet the specification in pipelined mode operation.
$\overline{LBO}$	Input, Static	Lower Address Burst Order Connected to V_{SS}: Device operates in linear mode. Connected to V_{DD} or unconnected: Device is in non-linear mode.
V_{DDQ}		I/O Power Supply
V_{SSQ}		I/O Ground
V_{DD}		Power Supply
V_{SS}		Ground
RSV		Reserved Pin, Don't Use These Pins
NC		No Connection

FUNCTIONAL DESCRIPTION

Read Operation

The address is registered on the rising edge of CLK and the associated output data will be valid after two cycles later.

Write Operation

During the write operation, the input data follows the address by two cycles later. The new incoming address and data are transferred into a two-stage write buffer while the residing address which are received two write cycles earlier are used for actual write operation. Data stored in these two-stage write data registers are used for first two write cycles following the read or unselected cycle. A subsequent read which matches the address in either write buffer allows the corresponding buffer data to be passed directly to output register.

Truth Table

CYCLE	ADDRESS USED	ZZ	$\overline{CE1}$	CE2	$\overline{CE3}$	$\overline{CLKE}$	ADV/$\overline{LD}$	$\overline{WE}$	$\overline{BWx}$	DATA	NOTES
Unselected	No	0	1	X	X	0	0	X	X	Hi-Z	
Unselected	No	0	X	0	X	0	0	X	X	Hi-Z	
Unselected	No	0	X	X	1	0	0	X	X	Hi-Z	
Begin Read	External	0	0	1	0	0	0	1	X	D-Out	3
Continue Read	Next	0	X	X	X	0	1	X	X	D-Out	3
Begin Write	External	0	0	1	0	0	0	0	0	D-In	
Begin Write /NOP	None	0	0	1	0	0	0	0	1	Hi-Z	4
Continue Write	Next	0	X	X	X	0	1	X	0	D-In	
Continue Write /NOP	Next	0	X	X	X	0	1	X	1	Hi-Z	4
Stall	Current	0	X	X	X	1	X	X	X	-	5
Snooze	None	1	X	X	X	X	X	X	X	Hi-Z	

Notes:

1. For a detailed definition of read/write, see the Write Table below.
2. An "X" means don't care, "1" means logic high, and "0" means logic low.
3. The $\overline{OE}$ pin enables the data output and is not sampled with the clock. All signals of the SRAM are sampled synchronously with the bus clock except for the $\overline{OE}$ pin.
4. NOP can be seen as No Operation.
5. If clock enable sampled high occurs during READ cycle, the bus will remain active (valid data). If clock enable sampled high occurs during WRITE cycle the bus will remain in high-Z state.

Write Table

READ/WRITE FUNCTION	$\overline{WE}$	$\overline{BW4}$	$\overline{BW3}$	$\overline{BW2}$	$\overline{BW1}$
Read	1	X	X	X	X
Write/NOP	0	1	1	1	1
Write byte 1 I/O1–I/O9	0	1	1	1	0
Write byte 2 I/O10–I/O18	0	1	1	0	1
Write byte 2, byte 1	0	1	1	0	0
Write byte 3 I/O19–I/O27	0	1	0	1	1
Write byte 3, byte 1	0	1	0	1	0
Write byte 3, byte 2	0	1	0	0	1
Write byte 3, byte 2, byte 1	0	1	0	0	0
Write byte 4 I/O28–I/O36	0	0	1	1	1
Write byte 4, byte 1	0	0	1	1	0
Write byte 4, byte 2	0	0	1	0	1
Write byte 4, byte 2, byte 1	0	0	1	0	0
Write byte 4, byte 3	0	0	0	1	1
Write byte 4, byte 3, byte 1	0	0	0	1	0
Write byte 4, byte 3, byte 2	0	0	0	0	1
Write all bytes I/O1–I/O36	0	0	0	0	0

Read-Write-Read Operation

There is no wait state to be asserted for a read-write-read operation. i.e. there is no extra dead bus cycle for read-write or write-read recovering and the bus utilization is 100%.

Burst Mode Operation

Burst read or write is activated if ADV/$\overline{LD}$ = HIGH at the rising edge of CLK, where the new address is composed of 2 new bits from burst counter and the remaining bits from the previous address. The sequencing of the counter can be either linear if $\overline{LBO}$ = LOW or interleaved if $\overline{LBO}$ = HIGH. $\overline{CE}$[3:1] and $\overline{WE}$ controls are ignored during burst mode.

Burst Address Sequence

	INTERLEAVED MODE ($\overline{LBO}$ = V_{DD})				**LINEAR MODE ($\overline{LBO}$ = V_{SS})**			
	A[1:0]	A[1:0]	A[1:0]	A[1:0]	A[1:0]	A[1:0]	A[1:0]	A[1:0]
External Start Address	00	01	10	11	00	01	10	11
Second Address	01	00	11	10	01	10	11	00
Third Address	10	11	00	01	10	11	00	01
Fourth Address	11	10	01	00	11	00	01	10

Stall Cycle

Stall cycle occurs when $\overline{CLKE}$ = HIGH is sampled. No internal clocks are generated. All addresses and control signals are ignored. If the previous cycle is a READ, output remains the same. If the previous cycle is a WRITE, output remains tri-stated. Any stall cycle will be added to increase the latency of output and input data.

Unselect Cycle

When $\overline{CE}$ = HIGH is sampled, a unselect state is entered. Output is tri-stated. By setting ADV/$\overline{LD}$ = HIGH for the following sampling cycle, the unselect state can be continued.

NOP Cycle

For a WRITE cycle with no asserted Byte-Write select signal, the device achieves a NOP operation. No addresses will be sampled.

Power Down Mode

An asynchronous ZZ pin can be set High to force the device into a power down mode. Outputs will go into High-Z state and the device draws only standby power. Minimum of 2 CLK cycles are required after setting ZZ to High before the device is forced into power down operation. Any operation pending when entering power down mode (read or write) is not guaranteed to successfully complete. Therefore, ZZ mode must not be initiated until valid pending operations are completed. When exiting ZZ mode during T_{ZZR}, only the unselect or read cycle should be given while the SRAM will be waken up again.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Core Supply Voltage to Vss	-0.5 to 4.6	V
I/O Supply Voltage to Vss	-0.5 to 4.6	V
Input/Output to V_{SSQ} Potential	V_{SSQ} -0.5 to V_{DDQ} +0.5	V
Allowable Power Dissipation	1.5	W
Storage Temperature	-65 to 150	°C
Operating Temperature	0 to +70	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

OPERATING CHARACTERISTICS

(V_{DD}/V_{DDQ} = 3.3V± 5%, V_{SS}/V_{SSQ} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input Low Voltage	V_{IL}	-		-0.5	-	+0.8	V
Input High Voltage	V_{IH}	-		+2.0	-	V_{DD} +0.3	V
Input Leakage Current	I_{LI}	V_{IN} = V_{SSQ} to V_{DDQ}		-1	-	+1	µA
Output Leakage Current	I_{LO}	$V_{I/O}$ = V_{SSQ} to V_{DDQ}, and data I/O pins in high-Z state defined in truth table		-1	-	+1	µA
Output Low Voltage	V_{OL}	I_{OL} = +8.0 mA		-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0 mA		2.4	-	-	V
Operating Current	I_{DD}	All inputs ≥ V_{IH} or ≤ V_{IL}, T_{CYC} ≥ min., I/O = 0 mA	-3A	-	-	420	mA
			-4	-	-	370	mA
			-4A	-	-	330	mA
			-5	-	-	300	mA
Standby Current	I_{SB1}	Device unselected, ZZ ≤ VSS + 0.2, All inputs ≤ VSS + 0.2 or ≥ VDD -0.2, and static I/O = 0 mA , CLK frequency = 0		-	-	10	mA
Standby Current	I_{SB2}	Device unselected, ZZ = V_{IL}, All inputs ≤ V_{IL} or ≥ V_{IH}, I/O = 0 mA, CLK frequency = 0		-	-	25	mA
ZZ Mode Current	I_{ZZ}	ZZ ≥ V_{IH}, All inputs ≤ V_{IL} or ≥ V_{IH}, I/O = 0 mA		-	-	10	mA

Note: Typical characteristics are measured at V_{DD} = 3.3V, T_A = 25° C.

CAPACITANCE

(V_{DD} = 3.3V, T_A = 25° C, Freq. = 1 MHz)

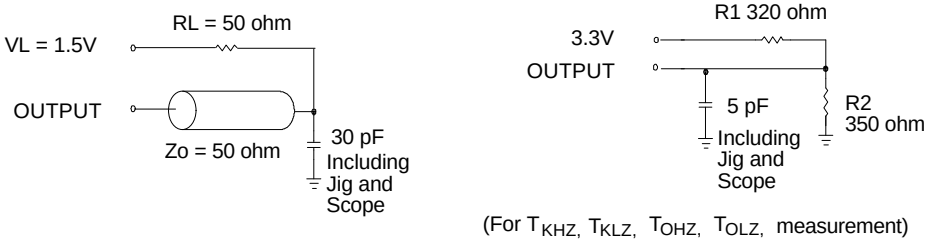
PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Address Input Capacitance	C_{ADD}	V_{IN} = 0V	3.5	pF
Clock & Control Input Capacitance	C_{CLK}	V_{CLK} = 0V	4	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	5	pF

Note: These parameters are sampled but not 100% tested.

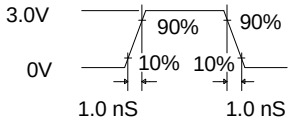
AC TEST CONDITIONS

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	1 nS
Input and Output Timing Reference Level	1.5V
Output Load	C_L = 30 pF, I_{OH}/I_{OL} = -4 mA/8 mA

AC TEST LOADS AND WAVEFORM



(For T_{KHZ}, T_{KLZ}, T_{OHZ}, T_{OLZ}, measurement)



AC TIMING CHARACTERISTICS

(V_{DD}/V_{DDQ} = 3.3V± 5%, V_{SS}/V_{SSQ} = 0V, T_A = 0 to 70° C, all timings measured in pipelined mode)

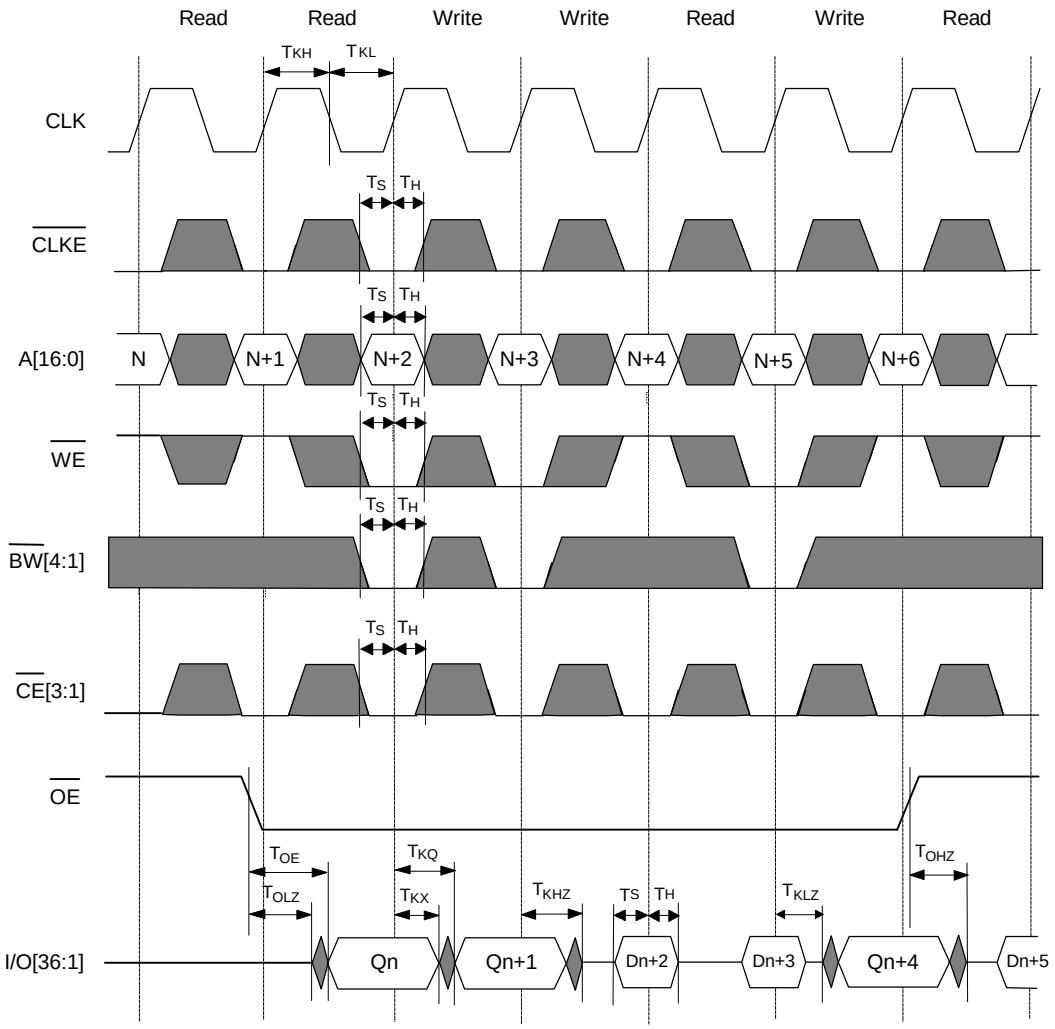
PARAMETER	SYM.	W25Z040A -3A		W25Z040A -4		W25Z040A -4A		W25Z040A -5		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Clock Cycle Time	T_{CYC}	6.7	-	7.5	-	8.5	-	10.0	-	nS	
Clock High Pulse Width	T_{KH}	2.5	-	3.0	-	3.0	-	3.5	-	nS	
Clock Low Pulse Width	T_{KL}	2.5	-	3.0	-	3.0	-	3.5	-	nS	
Input Setup Time	T_S	1.5	-	1.5	-	2.0	-	2.0	-	nS	
Input Hold Time	T_H	0.5	-	0.5	-	0.5	-	0.5	-	nS	
Clock Access Time	T_{KQ}	-	3.8	-	4.2	-	4.5	-	5.0	nS	
Output Hold from Clock High	T_{KX}	1.5	-	1.5	-	1.5	-	1.5	-	nS	
Clock High to Output Low-Z	T_{KLZ}	1.5	-	1.5	-	1.5	-	1.5	-	nS	1
Clock High to Output High-Z	T_{KHZ}	-	3.0	-	3.5	-	3.5	-	3.5	nS	1
Output Enable to Output Valid	T_{OE}	-	3.8	-	4.2	-	4.5	-	5.0	nS	
Output Enable to Output Low-Z	T_{OLZ}	0		0		0		0		nS	1
Output Disable to Output High-Z	T_{OHZ}	-	3.0	-	3.5	-	3.5	-	3.5	nS	1
ZZ Standby Time	T_{ZZS}	-	2	-	2	-	2	-	2	Cycle	
ZZ Recover Time	T_{ZZR}	-	20	-	20	-	20	-	20	nS	4

Notes:

1. These parameters are sampled but not 100% tested.
2. In the ZZ mode, the SRAM will enter a low-power state. In this mode, data retention is guaranteed and the clock is active.
3. Configuration signals $\overline{LBO}$ and $\overline{FT}$ are static and should not be changed during operation.
4. Write cycle should not be given for at least 20 nS while the SRAM is transitioning out of ZZ mode.

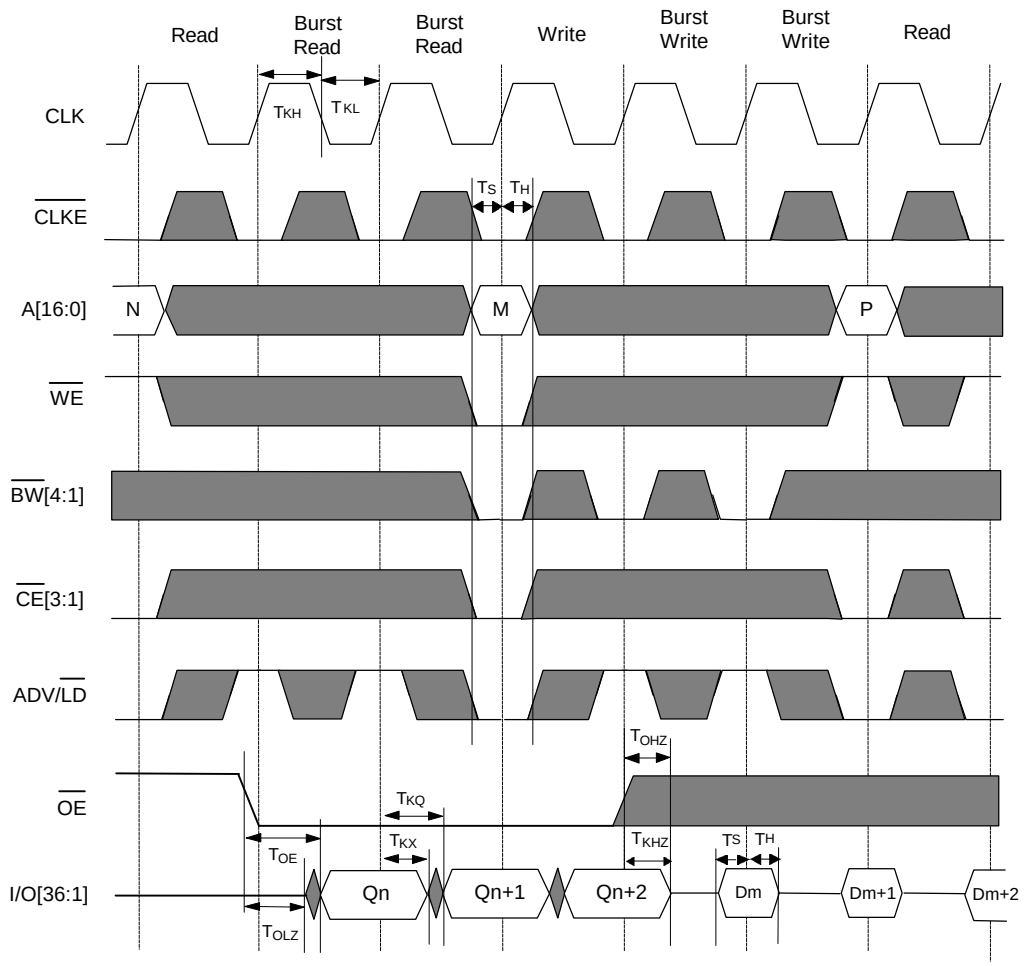
TIMING WAVEFORMS

Read/Write Cycle Timing



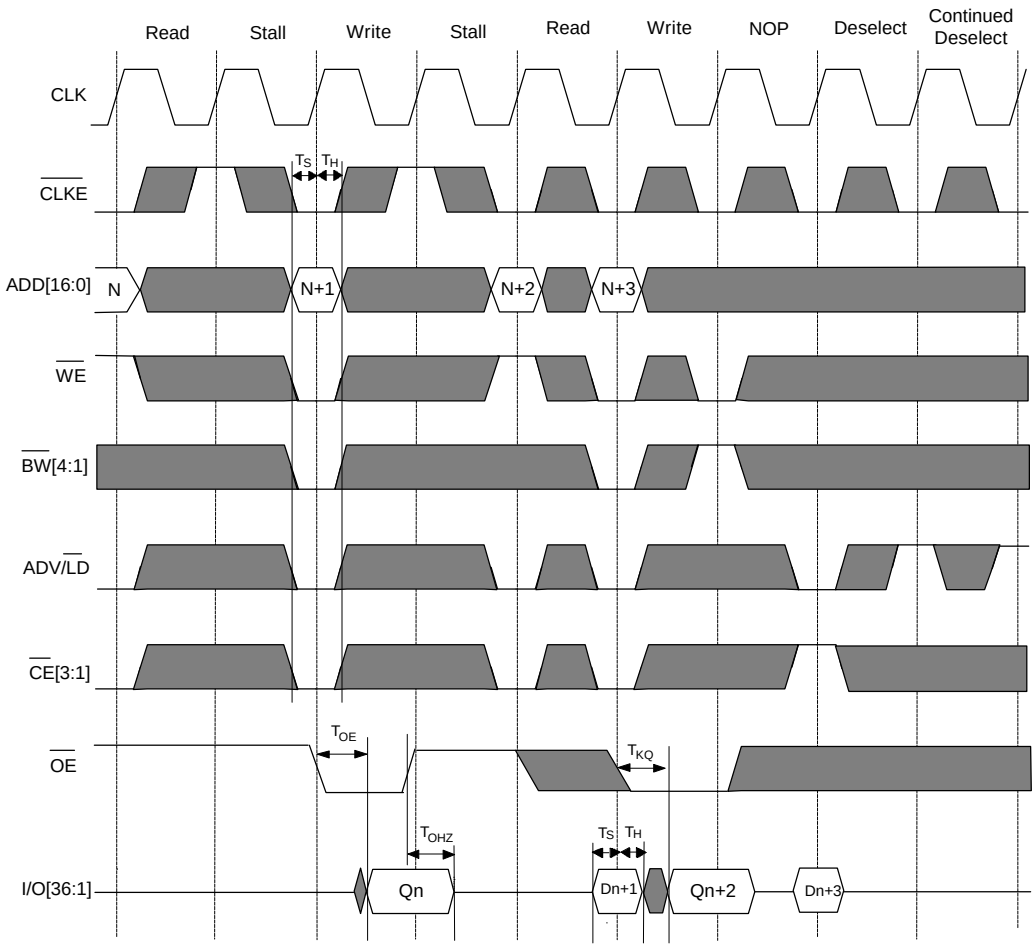
Timing Waveforms, continued

Burst Read/Write Cycle Timing



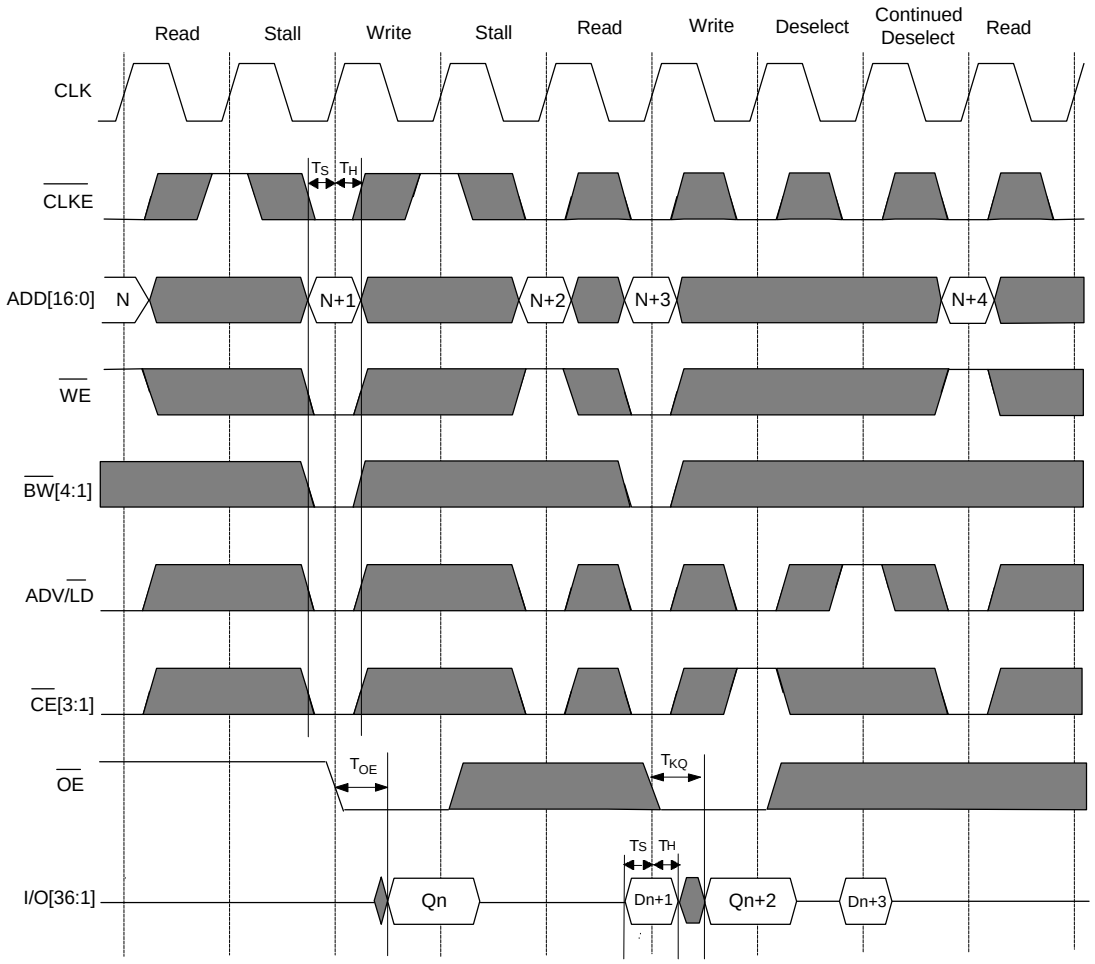
Timing Waveforms, continued

Stall NOP and Unselect Cycle Timing 1



Timing Waveforms, continued

Stall NOP and Unselect Cycle Timing 2



ORDERING INFORMATION

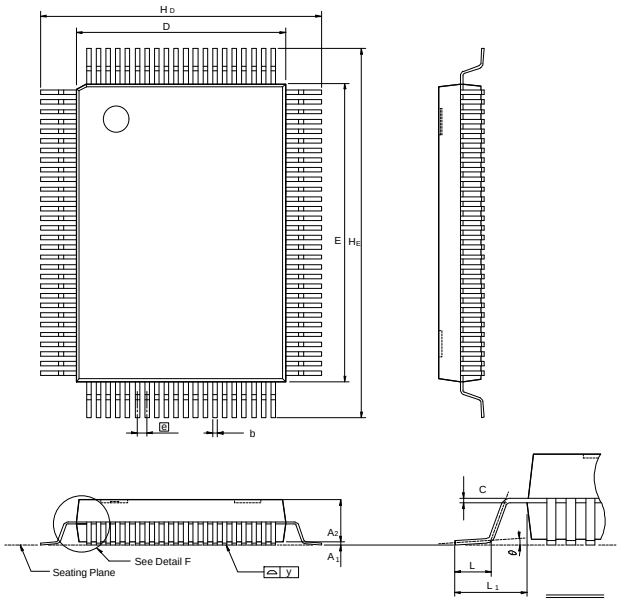
PART NO.	ACCESS TIME (nS)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (mA)	PACKAGE
W25Z040AD-3A	3.8	420	25	100-pin TQFP
W25Z040AD-4	4.2	370	25	100-pin TQFP
W25Z040AD-4A	4.5	330	25	100-pin TQFP
W25Z040AD-5	5.0	300	25	100-pin TQFP

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

PACKAGE DIMENSIONS

100-pin TQFP



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1035	1.40	1.45
b	0.009	0.013	0.015	0.22	0.32	0.38
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.547	0.551	0.555	13.90	14.00	14.10
E	0.783	0.787	0.791	19.90	20.00	20.10
e	0.020	0.026	0.032	0.498	0.65	0.802
H_D	0.626	0.630	0.634	15.90	16.00	16.10
H_E	0.862	0.866	0.870	21.90	22.00	22.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
y	—	—	0.003	—	—	0.08
θ	0°	—	7°	0°	—	7°

Notes:
1. Dimensions D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeters
4. General appearance spec. should be based on final visual inspection spec.

VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Mar. 1998		Initial Issued
A2	Apr. 1999	1, 4, 6, 7, 9, 14	Change speed bin from 133 to 150 MHz Cancel packaged in 100-pin QFP
		3	DC functional pins ($\overline{LBO}$, $\overline{FT}$) connect to V_{SS} or V_{DD}
		10~13	Marks the detail specifications in the waveforms

Headquarters
No. 4, Creation Rd. III,
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5796096
http://www.winbond.com.tw/
Voice & Fax-on-demand: 886-2-27197006

Taipei Office
11F, No. 115, Sec. 3, Min-Sheng East Rd.,
Taipei, Taiwan
TEL: 886-2-27190505
FAX: 886-2-27197502

Winbond Electronics (H.K.) Ltd.
Rm. 803, World Trade Square, Tower II,
123 Hoi Bun Rd., Kwun Tong,
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064

Winbond Electronics North America Corp.
Winbond Memory Lab.
Winbond Microelectronics Corp.
Winbond Systems Lab.
2727 N. First Street, San Jose,
CA 95134, U.S.A.
TEL: 408-9436666
FAX: 408-5441798