

Description

The μPD27C512 is an ultraviolet erasable, electrically programmable 524,288-bit ROM fabricated with an advanced CMOS process for substantial power savings. The device is organized as 64K words by 8 bits and operates from a single +5-volt power supply. All inputs and outputs are TTL-compatible. The device is available in a 28-pin cerdip package with quartz window.

Features

- ☐ 64K x 8-bit organization
- ☐ Ultraviolet erasable and electrically programmable
- ☐ High-speed programming mode
- ☐ Low power dissipation
 - 30 mA max (active)
 - 100 μA max (standby)
- ☐ TTL-compatible inputs and outputs
- ☐ Single +5-volt power supply
- ☐ Three-state outputs
- ☐ Advanced CMOS technology
- ☐ 28-pin cerdip with quartz window

Ordering Information

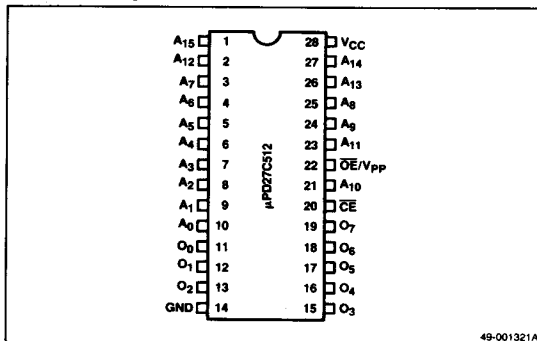
Part Number	Access Time (max)	Package
μPD27C512D-15	150 ns	28-pin cerdip with quartz window
D-20	200 ns	

Pin Identification

Symbol	Function
A ₀ -A ₁₅	Address inputs
O ₀ -O ₇	Data outputs
CE	Chip enable
OE/V _{PP}	Output enable/program voltage
GND	Ground
V _{CC}	Power supply

Pin Configuration

28-Pin Cerdip

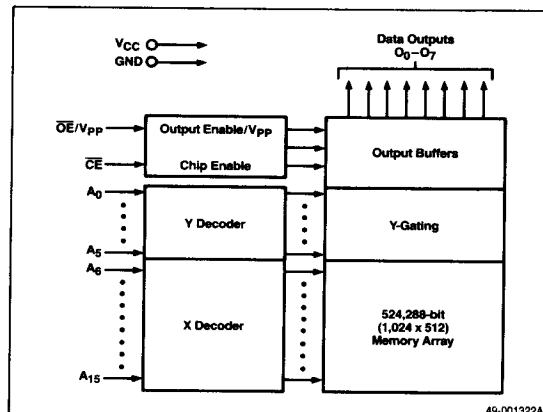


Absolute Maximum Ratings

Output voltage, V _O	-0.6 to +7.0 V
Input voltage, V _I	-0.6 to +7.0 V
Input voltage, A ₉	-0.6 to +13.5 V
Supply voltage, V _{CC}	-0.6 to +7.0 V
Supply voltage, V _{PP}	-0.6 to +13.5 V
Operating temperature, T _{OPR}	-10 to +80°C
Storage temperature, T _{STG}	-65 to +125°C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Block Diagram



Mode Selection

Mode	CE	OE/V _{PP}	V _{CC}	Outputs
Read	V _{IL}	V _{IL}	+5 V	D _{OUT}
Output disable	V _{IL}	V _{IH}	+5 V	High-Z
Standby	V _{IH}	X	+5 V	High-Z
Program	V _{IL}	V _{PP}	+6 V	D _{IN}
Program verify	V _{IL}	V _{IL}	+6 V	D _{OUT}
Program inhibit	V _{IH}	V _{PP}	+6 V	High-Z

Notes:

(1) X = V_{IL} or V_{IH}

DC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Read and Standby Modes						
Input voltage, high	V _{IH}	2.0		V _{CC} + 0.3	V	
Input voltage, low	V _{IL}	−0.3		0.8	V	
Output voltage, high	V _{OH1}	2.4			V	I _{OH} = −400 μA
	V _{OH2}	V _{CC} − 0.7			V	I _{OH} = −100 μA
Output voltage, low	V _{OL}			0.45	V	I _{OL} = 2.1 mA
Output leakage current	I _{LO}			10	μA	V _O = 0 to V _{CC} ; $\overline{\text{OE}}$ = V _{IH}
Input leakage current	I _{LI}			10	μA	V _I = 0 to V _{CC}
V _{CC} current, active	I _{CCA1}			30	mA	$\overline{\text{CE}}$ = V _{IL} ; V _I = V _{IH}
	I _{CCA2}			30	mA	f = 5 MHz; I _{OUT} = 0 mA
V _{CC} current, standby	I _{CCS1}			1	mA	$\overline{\text{CE}}$ = V _{IH}
	I _{CCS2}		1	100	μA	$\overline{\text{CE}}$ = V _{CC} ; V _I = 0 to V _{CC}

Programming Modes

T_A = 25 ±5°C; V_{CC} = 6.0 ±0.25 V; V_{PP} = 12.5 ±0.3 V

Input voltage, high	V _{IH}	2.0		V _{CC} + 0.3	V	
Input voltage, low	V _{IL}	-0.3		0.8	V	
Input leakage current	I _{LI}			10	μA	V _I = V _{IL} or V _{IH}
Output voltage, high	V _{OH}	2.4			V	I _{OH} = -400 μA
Output voltage, low	V _{OL}			0.45	V	I _{OL} = 2.1 mA
V _{PP} current	I _{PP}			30	mA	CE = V _{IL} ; OE/V _{PP} = V _{IH}
V _{CC} current	I _{CC}			30	mA	

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Input capacitance	C _{IN1}			6	pF	V _I = 0 V
	C _{IN2}			20	pF	OE/V _{PP} ; V _I = 0 V
Output capacitance	C _{OUT}			12	pF	V _O = 0 V

AC Characteristics, Read and Standby Modes

$T_A = 0 \text{ to } +70^\circ\text{C}$; $V_{CC} = 5.0 \text{ V} \pm 10\%$

Parameter	Symbol	Limits				Unit	Test Conditions
		μPD27C512-15		μPD27C512-20			
		Min	Max	Min	Max		
Address to output delay	t _{ACC}		150		200	ns	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$
\overline{CE} to output delay	t _{CE}		150		200	ns	$\overline{OE}/V_{PP} = V_{IL}$
\overline{OE}/V_{PP} to output delay	t _{OE}		75		75	ns	$\overline{CE} = V_{IL}$
\overline{OE}/V_{PP} high to output float	t _{DF}	0	60	0	60	ns	$\overline{CE} = V_{IL}$
Output hold from address, \overline{CE} or \overline{OE} , whichever transition occurs first	t _{OH}	0		0		ns	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$

Notes:

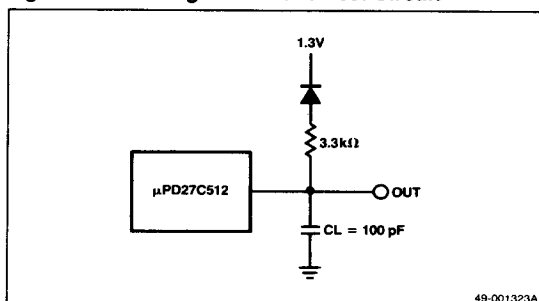
- (1) Output load: see figure 1. Input rise and fall times $\leq 20 \text{ ns}$. Input pulse levels: 0.45 and 2.4 V. Timing measurement reference levels: inputs and outputs = 0.8 and 2.0 V

AC Characteristics, Programming Modes

$T_A = 25 \pm 5^\circ\text{C}$; $V_{CC} = 6.0 \pm 0.25 \text{ V}$; $V_{PP} = 12.5 \pm 0.3 \text{ V}$

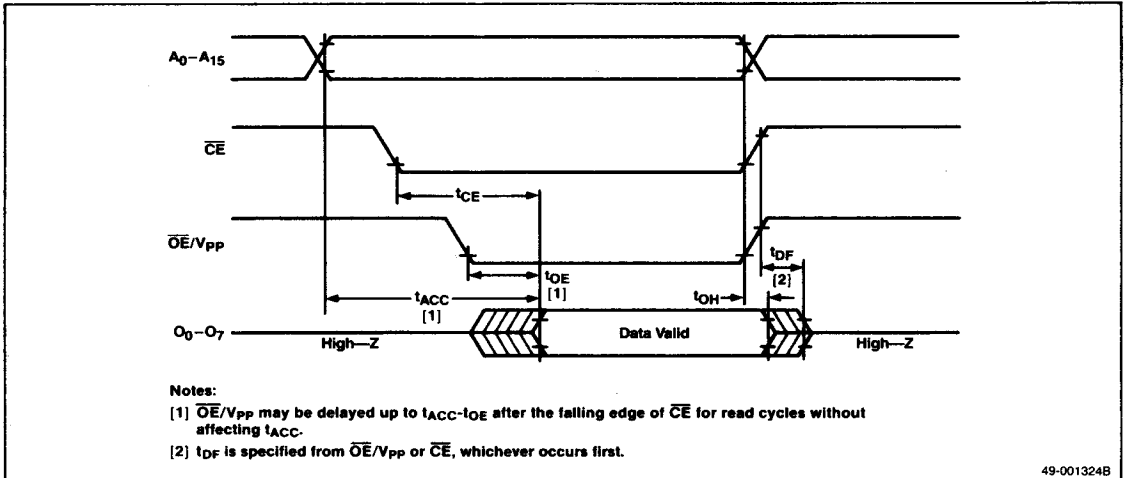
Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Address setup time	t_{AS}	2			μs	
\overline{OE} setup time	t_{OES}	2			μs	
Data setup time	t_{DS}	2			μs	
Address hold time	t_{AH}	2			μs	
Data hold time	t_{DH}	2			μs	
\overline{CE} to output float time	t_{DF}	0		130	ns	
V_{CC} setup time	t_{VCS}	2			μs	
Initial program pulse width	t_{PW}	0.95	1.0	1.05	ms	
Overprogram pulse width	t_{OPW}	2.85		78.75	ms	
\overline{CE} to output delay	t_{DV}			1	μs	$\overline{OE}/V_{PP} = V_{IL}$
\overline{OE}/V_{PP} hold time	t_{OEH}	2			μs	
\overline{OE}/V_{PP} recovery time	t_{VR}	2			μs	
\overline{OE}/V_{PP} rise time	t_{PRT}	50			ns	

Figure 1. Loading Conditions Test Circuit

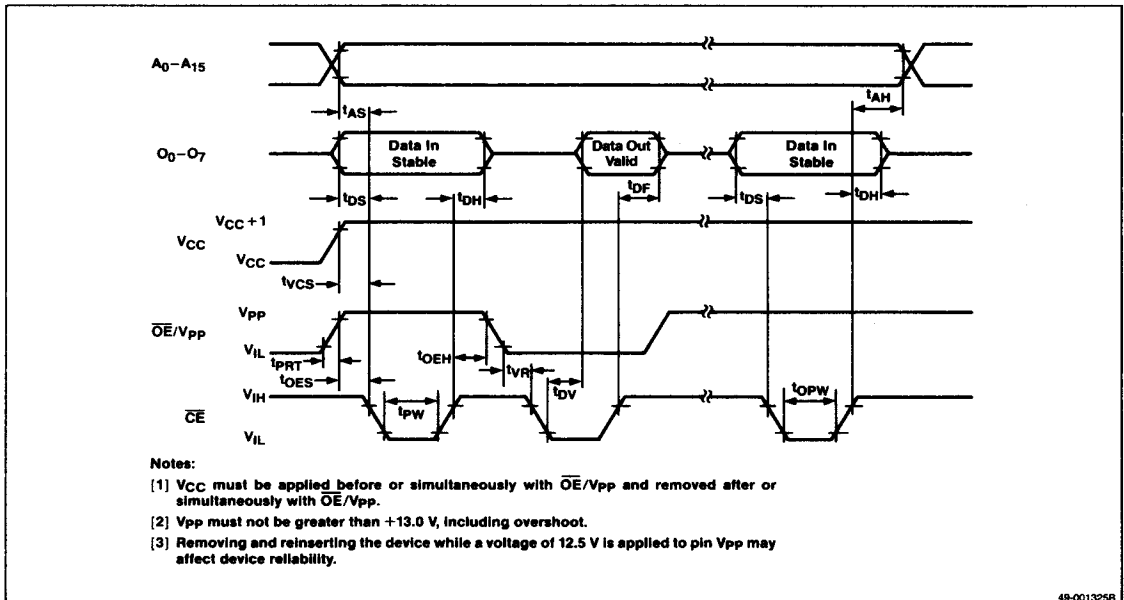


Timing Waveforms

Read Mode



Programming Mode



Programming Operation

High-Speed Programming Mode

Begin programming by erasing all data; this places all bits in the high-level (1) state. Enter data by programming a low-level (0) TTL signal into the chosen bit location.

Address the first location and apply valid data at the eight output pins. Raise V_{CC} to $+6\text{ V} \pm 0.25\text{ V}$; then raise \overline{OE}/V_{PP} to $+12.5\text{ V} \pm 0.3\text{ V}$. Apply a 1-ms ($\pm 5\%$) program pulse to \overline{CE} as shown in the programming mode timing waveform. The bit is verified and the program/no-program decision is made. If the bit is not programmed, apply another 1-ms pulse to \overline{CE} , up to a maximum of 25 times. If the bit is programmed within 25 tries, apply an additional overprogram pulse of "x" ms (where "x" equals the number of tries multiplied by 3) and input the next address. If the bit is not programmed in 25 tries, reject the device as a program failure.

Programming Inhibit Mode

Use the programming inhibit mode to program multiple μPD27C512s connected in parallel. All like inputs (except \overline{CE} , but including \overline{OE}/V_{PP}) may be common. Program individual devices by applying a low-level (0) TTL pulse to the \overline{CE} input of the μPD27C512 to be programmed. Applying a high level (1) to the \overline{CE} input of the other devices prevents them from being programmed.

Program Verify Mode

Perform verification on the programmed bits to determine that the data was correctly programmed. The program verification can be performed with \overline{CE} and \overline{OE}/V_{PP} at low levels (0).

Erase

Erase data on the μPD27C512 by exposing it to light with a wavelength shorter than 400 nm. Exposure to direct sunlight or fluorescent light could also erase the data. Consequently, mask the window to prevent unintentional erasure by ultraviolet rays.

Data is typically erased by 254-nm ultraviolet rays. A minimum lighting level of 15 W sec/cm^2 (ultraviolet ray intensity multiplied by exposure time) is required to completely erase written data.

An ultraviolet lamp rated at $12,000\text{ μW/cm}^2$ takes approximately 15 to 20 minutes to complete erasure. Place the μPD27C512 within 2.5 cm of the lamp tubes. Remove any filter on the lamp.