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MITEL SEMICONDUCTOR

CMOS **MT9315**
Acoustic Echo Canceller
Advance Information

DS5038 ISSUE 3 February 1999

Ordering Information

MT9315AP	28 Pin PLCC
MT9315AE	28 Pin PDIP

-40 °C to + 85 °C

Features

- Contains two echo cancellers: 112ms acoustic echo canceller + 16ms line echo canceller
- Works with low cost voice codec. ITU-T G.711 or signed mag μ/A-Law, or linear 2's comp
- Each port may operate in different format.
- Advanced NLP design - full duplex speech with no switched loss on audio paths
- Fast re-convergence time: tracks changing echo environment quickly
- Adaptation algorithm converges even during Double-Talk
- Designed for exceptional performance in high background noise environments
- Provides protection against narrow-band signal divergence
- Howling prevention stops uncontrolled oscillation in high loop gain conditions
- Offset nulling of all PCM channels
- Serial micro-controller interface
- ST-BUS or variable-rate SSI PCM interfaces
- User gain control provided for speaker path (-24dB to +21dB in 3dB steps)
- AGC on speaker path
- Handles up to 0 dB acoustic echo return loss and 0dB line ERL
- Transparent data transfer and mute options
- 20 MHz master clock operation
- Low power mode during PCM Bypass

Applications

- Full duplex speaker-phone for digital telephone
- Echo cancellation for video conferencing
- Handsfree in automobile environment
- Full duplex speaker-phone for PC

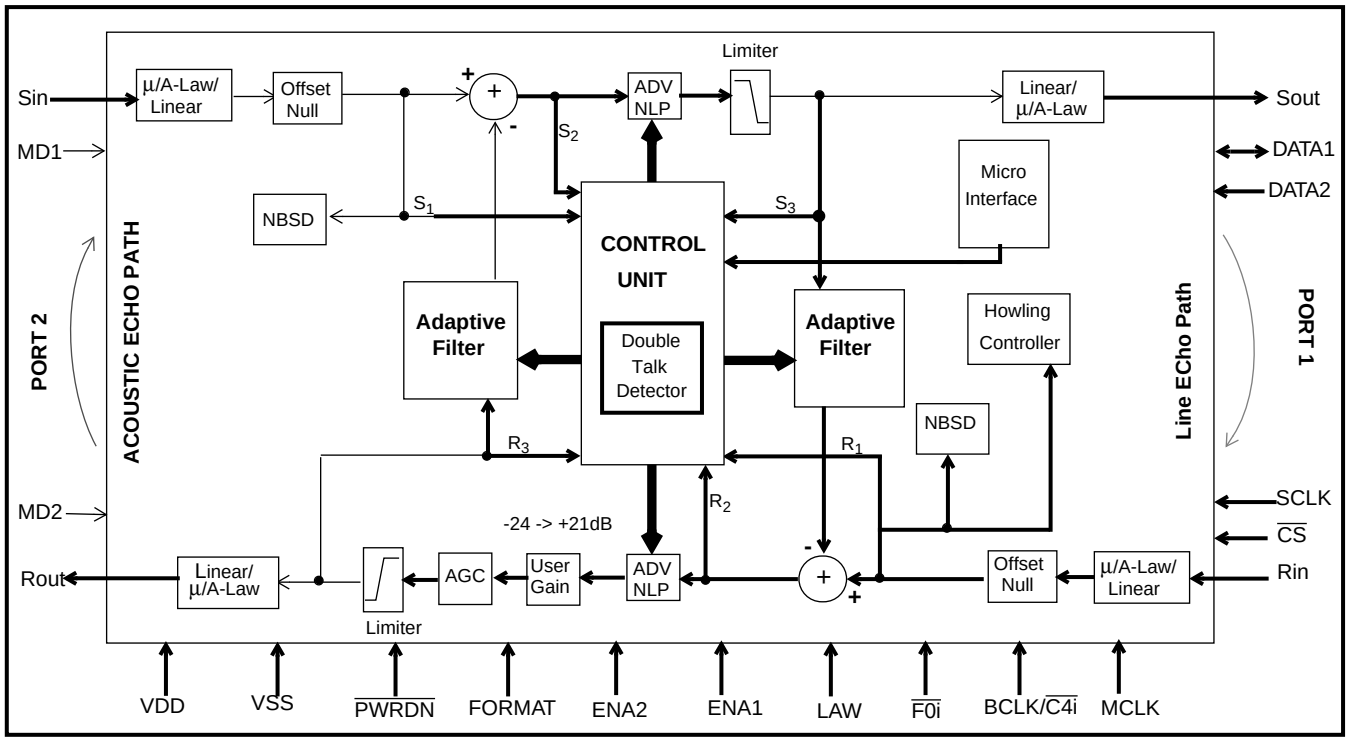


Figure 1 - Functional Block Diagram

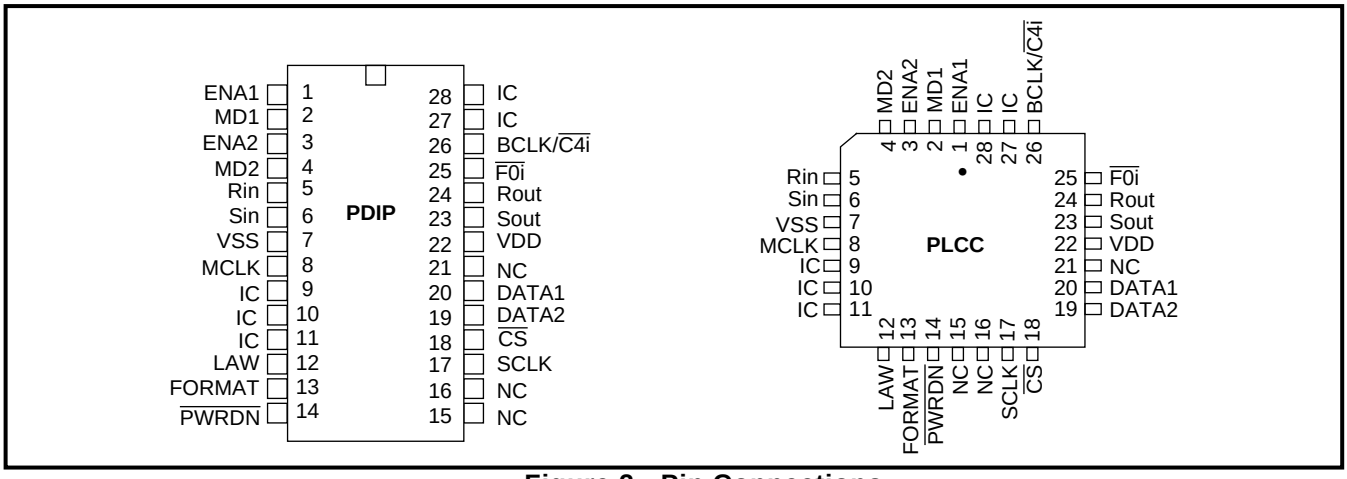


Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
1	ENA1	**SSI Enable Strobe / ST-BUS Mode for Rin/Sout (Input)**. This pin has dual functions depending on whether SSI or ST-BUS is selected. For SSI, this strobe must be present for frame synchronization. This is an active high channel enable strobe, 8 or 16 data bits wide, enabling serial PCM data transfer for on Rin/Sout pins. Strobe period is 125 microseconds. For ST-BUS, this pin, in conjunction with the MD1 pin, will select the proper ST-BUS mode for Rin/Sout pins (see ST-BUS Operation description).
2	MD1	**ST-BUS Mode for Rin/Sout (Input)**. When in ST-BUS mode, this pin, in conjunction with the ENA1 pin, will select the proper ST-BUS mode for Rin/Sout pins (see ST-BUS Operation description). Connect this pin to Vss in SSI mode.
3	ENA2	**SSI Enable Strobe / ST-BUS Mode for Sin/Rout (Input)**.This pin has dual functions depending on whether SSI or ST-BUS is selected. For SSI, this is an active high channel enable strobe, 8 or 16 data bits wide, enabling serial PCM data transfer on Sin/Rout pins. Strobe period is 125 microseconds. For ST-BUS, this pin, in conjunction with the MD2 pin, will select the proper ST-BUS mode for Sin/Rout pins (see ST-BUS Operation description).
4	MD2	**ST-BUS Mode for Sin/Rout (Input)**.When in ST-BUS mode, this pin in conjunction with the ENA2 pin, will select the proper ST-BUS mode for Sin/Rout pins (see ST-BUS Operation description). Connect this pin to Vss in SSI mode.
5	Rin	**Receive PCM Signal Input (Input).** 128 kbit/s to 4096 kbit/s serial PCM input stream. Data may be in either companded or 2's complement linear format. This is the Receive Input channel from the line (or line) side. Data bits are clocked in following SSI or ST-BUS timing requirements.
6	Sin	**Send PCM Signal Input (Input).** 128 kbit/s to 4096 kbit/s serial PCM input stream. Data may be in either companded or 2's complement linear format. This is the Send Input channel (from the microphone). Data bits are clocked in following SSI or ST-BUS timing requirements.
7	VSS	**Digital Ground:** Nominally 0 volt.
8	MCLK	**Master Clock (Input):** Nominal 20 MHz Master Clock input. May be connected to an asynchronous (relative to frame signal) clock source.
9	IC	**Internal Connection (Input):** Must be tied to Vss.
10, 11	IC	**Internal Connection (Input).** Tie to Vss.
12	LAW	**A/$\overline{\mu}$ Law Select (Input).** When low, selects μ–Law companded PCM. When high, selects A-Law companded PCM. This control is for both serial pcm ports.

Pin Description (continued)

Pin #	Name	Description
13	FORMAT	**ITU-T/$\overline{\text{Sign Mag}}$ (Input).** When low, selects sign-magnitude PCM code. When high, selects ITU-T (G.711) PCM code. This control is for both serial pcm ports.
14	$\overline{\text{PWRDN}}$	**Power-down (Input).** An active low resets the device and puts the MT9315 into a low-power stand-by mode.
15, 16	NC	**No Connect (Output).** This pin should be left un-connected.
17	SCLK	**Serial Port Synchronous Clock (Input).** Data clock for the serial microport interface.
18	$\overline{\text{CS}}$	**Serial Port Chip Select (Input).** Enables serial microport interface data transfers. Active low.
19	DATA2	**Serial Data Receive (Input).** In Motorola/National serial microport operation, the DATA2 pin is used for receiving data. In Intel serial microport operation, the DATA2 pin is not used and must be tied to Vss or Vdd.
20	DATA1	**Serial Data Port (Bidirectional).** In Motorola/National serial microport operation, the DATA1 pin is used for transmitting data. In Intel serial microport operation, the DATA1 pin is used for transmitting and receiving data.
21	NC	**No Connect (Output).** This pin should be left un-connected.
22	VDD	Positive Power Supply. Nominal is 5V
23	Sout	**Send PCM Signal Output (Output).** 128 kbit/s to 4096 kbit/s serial PCM output stream. Data may be in either companded or 2's complement linear PCM format. This is the Send Out signal after acoustic echo cancellation and Non-linear processing. Data bits are clocked out following SSI or ST-BUS timing requirements.
24	Rout	**Receive PCM Signal Output (Output).** 128 kbit/s to 4096 kbit/s serial PCM output stream. Data may be in either companded or 2's complement linear PCM format. This is the Receive out signal after line echo cancellation Non-linear processing, AGC, and gain control. Data bits are clocked out following SSI or ST-BUS timing requirements.
25	$\overline{\text{F0i}}$	**Frame Pulse (Input).** In ST-BUS operation, this is an active-low frame alignment pulse. SSI operation is enabled by connecting this pin to Vss.
26	BCLK/$\overline{\text{C4i}}$	**Bit Clock/ST-BUS Clock (Input)**. In SSI operation, BCLK pin is a 128 kHz to 4.096 MHz bit clock. This clock must be synchronous with ENA1, and ENA2 enable strobes. In ST-BUS operation, $\overline{\text{C4i}}$ pin must be connected to the 4.096MHz ($\overline{\text{C4}}$) system clock.
27, 28	IC	**Internal Connection (Input).** Tie to Vss.

Notes:

1. All inputs have TTL compatible logic levels except for MCLK, Sin and Rin pins which have CMOS compatible logic levels and $\overline{\text{PWRDN}}$ pin which has Schmitt trigger compatible logic levels.
2. All outputs are CMOS pins with CMOS logic levels except DATA1 which is TTL bidirectional.

Glossary

Double-Talk	Simultaneous signals present on Rin and Sin.
Near-end Single-Talk	Signals only present at Sin input.
Far-end Single-Talk	Signals only present at Rin input.
ADV NLP	Advanced Non-Linear-Processor
Howling	Oscillation caused by feedback from acoustic and line echo paths
Narrowband	Any mono or dual sinusoidal signals
NBSD	Narrow Band Signal Detector
Noise-Gating	Audible switching of background noise
Offset Nulling	Removal of DC component
Reverberation time	The time duration before an echo level decays to -60dBm
ERL	Echo Return Loss
ERLE	Echo Return Loss Enhancement
AGC	Automatic Gain Control

Functional Description

The MT9315 device contains two echo cancellers, as well as the many control functions necessary to operate the echo cancellers. One canceller is for acoustic speaker to microphone echo, and one for line echo cancellation. The MT9315 provides clear signal transmission in both audio path directions to ensure reliable voice communication, even with low level signals. The MT9315 does not use variable attenuators during double-talk or single-talk periods of speech, as do many other acoustic echo cancellers for speaker-phones. Instead, the MT9315 provides high performance full-duplex operation similar to network echo cancellers, so that users experience clear speech and un-interrupted background signals during the conversation. This prevents subjective sound quality problems associated with “noise gating” or “noise contrasting”.

The MT9315 uses an advanced adaptive filter algorithm that is double-talk stable, which means that convergence takes place even while both parties are talking [1]. This algorithm allows continual tracking of changes in the echo path, regardless of double-talk, as long as a reference signal is available for the echo canceller.

(1. Patent Pending)

The echo tail cancellation capability of the acoustic echo canceller has been sized appropriately (112ms) to cancel echo in an average sized office with a reverberation time of less than 112ms. The 16ms line echo canceller is sufficient to ensure a high ERLE for most line circuits.

In addition to the echo cancellers, the following functions are supported:

- Control of adaptive filter convergence speed during periods of double-talk, far end single-talk, and near-end echo path changes.
- Control of Non-Linear Processor thresholds for suppression of residual non-linear echo.
- Howling detector to identify when instability is starting to occur, and to take action to prevent oscillation.
- Narrow-Band Detector for preventing adaptive filter divergence caused by narrow-band signals
- Offset Nulling filters for removal of DC components in PCM channels.
- Limiters that introduce controlled saturation levels.
- Serial controller interface compatible with Motorola, National and Intel microcontrollers.
- PCM encoder/decoder compatible with μ/A-Law ITU-T G.711, μ/A-Law Sign-Mag or linear 2’s complement coding.
- Automatic gain control on the receive speaker path.

Adaptation Speed Control

The adaptation speed of the acoustic echo canceller is designed to optimize the convergence speed versus divergence caused by interfering near-end signals. Adaptation speed algorithm takes into account many different factors such as relative double-talk condition, far end signal power, echo path change, and noise levels to achieve fast convergence.

Advanced Non-Linear Processor (ADV-NLP)[2]

(2. Patent Pending)

After echo cancellation, there is likely to be residual echo which needs to be removed so that it will not be audible. The MT9315 uses an NLP to remove low level residual echo signals which are not comprised of background noise. The operation of the NLP depends upon a dynamic activation threshold, as well as a double-talk detector which disables the NLP during double-talk periods.

The MT9315 keeps the perceived noise level constant, without the need for any variable attenuators or gain switching that causes audible “noise gating”. The noise level is constant and identical to the original background noise even when the NLP is activated.

For each audio path, the NLP can be disabled by setting the NLP- bit to 1 in the LEC or AEC control registers.

Narrow Band Signal Detector (NBSD) [3]

(3. Patent Pending)

Single or multi-frequency tones (e.g. DTMF, or signalling tones) present in the reference input of an echo canceller for a prolonged period of time may cause the adaptive filter to diverge. The Narrow Band Signal Detector (NBSD) is designed to prevent this divergence by detecting single or multi-tones of arbitrary frequency, phase, and amplitude. When narrow band signals are detected, the filter adaptation process is stopped but the echo canceller continues to cancel echo.

The NBSD can be disabled by setting the NB- bit to 1 in the MC control registers.

Howling Detector (HWLD) [4]

(4. Patent Pending)

The Howling detector is part of an Anti-Howling control, designed to prevent oscillation as a result of positive feedback in the audio paths.

The HWLD can be disabled by setting the AH- bit to 1 in the (MC) control register.

Offset Null Filter

To ensure robust performance of the adaptive filters at all times, any DC offset that may be present on either the Rin signal or the Sin signal, is removed by highpass filters. These filters have a corner frequency placed at 40Hz.

The offset null filters can be disabled by setting the HPF- bit to 1 in the LEC or AEC control registers.

Limiters

To prevent clipping in the echo paths, two limiters with variable thresholds are provided at the outputs.

The Rout limiter threshold is in Rout Limiter Register 1 and 2. The Sout limiter threshold is in Sout Limiter Register. Both output limiters are always enabled.

User Gain

The user gain function provides the ability for users to adjust the audio gain in the receive path (speaker path). This gain is adjustable from -24dB to +21dB in 3dB steps. It is important to use ONLY this user gain function to adjust the speaker volume. The user gain function in the MT9315 is optimally placed between the two echo cancellers such that no reconvergence is necessary after gain changes.

The gain can be accessed through Receive Gain Control Register.

AGC

The AGC function is provided to limit the volume in the speaker path. The gain of the speaker path is automatically reduced during the following conditions:

- When clipping of the receive signal occurs.
- When initial convergence of the acoustic echo canceller detects unusually large echo return.
- When howling is detected.

The AGC can be disabled by setting the AGC- bit to 1 in MC control register.

Mute Function

A pcm mute function is provided for independent control of the Receive and Send audio paths. Setting the MUTE_R or MUTE_S bit in the MC register, causes quiet code to be transmitted on the Rout or Sout paths respectively.

Quiet code is defined according to the following table.

	LINEAR 16 bits 2's complement	SIGN/ MAGNITUDE μ-Law A-Law	CCITT (G.711)	
			μ-Law	A-Law
+Zero (quiet code)	0000h	80h	FFh	D5h

Table 1 - Quiet PCM Code Assignment

Bypass Control

A PCM bypass function is provided to allow transparent transmission of pcm data through the MT9315. When the bypass function is active, pcm data passes transparently from Rin to Rout and from Sin to Sout, with bit-wise integrity preserved.

When the Bypass function is selected, most internal functions are powered down to provide low power consumption.

The BYPASS control bit is located in the main control MC register.

Adaptation Enable/Disable

Adaptation control bits are located in the AEC and LEC control registers. When the ADAPT- bit is set to 1, the adaptive filter is frozen at the current state. In this state, the device continues to cancel echo with the current echo model.

When the ADAPT- bit is set to 0, the adaptive filter is continually updated. This allows the echo canceller to adapt and track changes in the echo path. This is the normal operating state.

MT9315 Throughput Delay

In all modes, voice channels always have 2 frames of delay. In ST-BUS operation, the D and C channels have a delay of one frame.

Power Down

Forcing the $\overline{\text{PWRDN}}$ pin to logic low, will put the MT9315 into a power down state. In this state all internal clocks are halted, the DATA1, Sout and Rout pins are tristated.

The user should hold the $\overline{\text{PWRDN}}$ pin low for 200 msec on Power-up. This will insure that the device powers up in a proper state.

The device will automatically begin the execution of initialization routines when the $\overline{\text{PWRDN}}$ pin is returned to logic high and a clock is applied to the MCLK pin. The initialization routines execute for one frame and will set the MT9315 to default register values.

After power down, the user waits for 2 complete 8 KHz frames prior to writing to the device registers.

PCM Data I/O

The PCM data transfer for the MT9315 is provided through two PCM ports. One port consists of Rin and Sout pins while the second port consists of Sin and Rout pins. The data are transferred through these ports according to either ST-BUS or SSI conventions. The device determines the convention by monitoring the signal applied to the $\overline{\text{F0i}}$ pin. When a valid ST-BUS frame pulse is applied to the $\overline{\text{F0i}}$ pin, the MT9315 will assume ST-BUS operation. If $\overline{\text{F0i}}$ is tied continuously to Vss, the MT9315 will assume SSI operation.

ST-BUS Operation

The ST-BUS PCM interface conforms to Mitel's ST-BUS standard and it is used to transport 8 bit companded PCM data (using one timeslot) or 16 bit 2's complement linear PCM data (using two timeslots). The MD1/ENA1 pins select the timeslot on the Rin/Sout port while the MD2/ENA2 pin selects the timeslot on the Sin/Rout port. See Table 2 and Figures 3 to 6.

PORT1 Rin/Sout		ST-BUS Mode Selection	PORT2 Sin/Rout	
Enable Pins			Enable Pins	
MD1	ENA1		MD2	ENA2
0	0	Mode 1. 8 bit companded PCM I/O on timeslot 0	0	0
0	1	Mode 2. 8 bit companded PCM I/O on timeslot 2.	0	1
1	0	Mode 3. 8 bit companded PCM I/O on timeslot 2. Includes D & C channel bypass in timeslots 0 & 1.	1	0
1	1	Mode 4. 16 bit 2's complement linear PCM I/O on timeslots 0 & 1.	1	1

Table 2 - ST-BUS Mode Select

SSI Operation

The SSI PCM interface consists of data input pins (Rin, Sin), data output pins (Sout, Rout), a variable rate bit clock (BCLK), and two enable pins (ENA1, ENA2) to provide strobes for data transfers. The active high enable may be either 8 or 16 BCLK cycles in duration. Automatic detection of the data type (8 bit companded or 16 bit 2's complement linear) is accomplished internally. The data type cannot change dynamically from one frame to the next.

In SSI operation, the frame boundary is determined by the rising edge of the ENA1 enable strobe (see Figure 7). The other enable strobe (ENA2) is used for parsing input/output data and it must pulse within 125 microseconds of the rising edge of ENA1.

In SSI operation, the enable strobes may be a mixed combination of 8 or 16 BCLK cycles allowing the flexibility to mix 2's complement linear data on one port (e.g., Rin/Sout) with companded data on the other port (e.g., Sin/Rout).

Enable Strobe Pin	Designated PCM I/O Port
ENA1	Line Side Echo Path (PORT 1)
ENA2	Acoustic Side Echo Path (PORT 2)

Table 3 - SSI Enable Strobe Pins

PCM Law and Format Control (LAW, FORMAT)

The PCM companding/coding law used by the MT9315 is controlled through the LAW and FORMAT pins. ITU-T G.711 companding curves for μ-Law and A-Law are selected by the LAW pin. PCM coding ITU-T G.711 and Sign-Magnitude are selected by the FORMAT pin. See Table 4.

PCM Code	Sign-Magnitude FORMAT=0	ITU-T (G.711) FORMAT=1	
	μ/A-LAW LAW = 0 or 1	μ-LAW LAW = 0	A-LAW LAW =1
+ Full Scale	1111 1111	1000 0000	1010 1010
+ Zero	1000 0000	1111 1111	1101 0101
- Zero	0000 0000	0111 1111	0101 0101
- Full Scale	0111 1111	0000 0000	0010 1010

Table 4 - Companded PCM

Linear PCM

The 16-bit 2's complement PCM linear coding permits a dynamic range beyond that which is specified in ITU-T G.711 for companded PCM. The echo-cancellation algorithm will accept 16 bits 2's complement linear code which gives a maximum signal level of +15dBm0.

Bit Clock (BCLK/C4i)

The BCLK/$\overline{C4i}$ pin is used to clock the PCM data in both SSI (BCLK) and ST-BUS ($\overline{C4i}$) operations.

In SSI operation, the bit rate is determined by the BCLK frequency. This input must contain either eight or sixteen clock cycles within the valid enable strobe window. BCLK may be any rate between 128 KHz to 4.096 MHz and can be discontinuous outside of the enable strobe windows defined by ENA1, ENA2 pins. Incoming PCM data (Rin, Sin) are sampled on the falling edge of BCLK while outgoing PCM data (Sout, Rout) are clocked out on the rising edge of BCLK. See Figure 11.

In ST-BUS operation, connect the system $\overline{C4}$ (4.096MHz) clock to the $\overline{C4i}$ pin.

Master Clock (MCLK)

A nominal 20MHz master clock (MCLK) is required. The MCLK input may be asynchronous with the 8KHz frame.

Microport

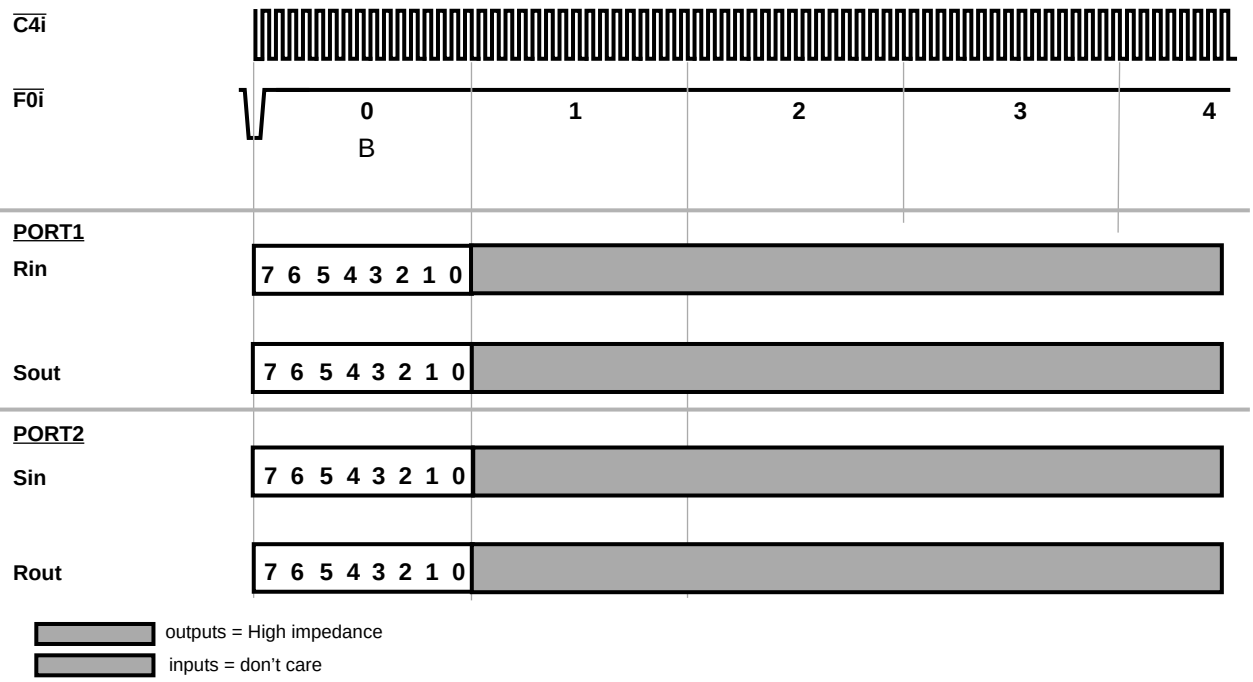
The serial microport provides access to all MT9315 internal read and write registers. This microport is compatible with Intel MCS-51 (mode 0), Motorola SPI (CPOL=0, CPHA=0), and National Semiconductor Microwire specifications. The microport consists of a transmit/receive data pin (DATA1), a receive data pin (DATA2), a chip select pin ($\overline{CS}$) and a synchronous data clock pin (SCLK).

The MT9315 automatically adjusts its internal timing and pin configuration to conform to Intel or Motorola/ National requirements. The microport dynamically senses the state of the SCLK pin each time $\overline{CS}$ pin becomes active (i.e. high to low transition). If SCLK pin is high during $\overline{CS}$ activation, then Intel mode 0 timing is assumed. In this case DATA1 pin is defined as a bi-directional (transmit/receive) serial port and DATA2 is internally disconnected. If SCLK is low during $\overline{CS}$ activation, then Motorola/National timing is assumed and DATA1 is defined as the data transmit pin while DATA2 becomes the data receive pin. The MT9315 supports Motorola half-duplex processor mode (CPOL=0 and CPHA=0). This means that during a write to the MT9315, by the Motorola processor, output data from the DATA1 pin must be ignored. This also means that input data on the DATA2 pin is ignored by the MT9315 during a valid read by the Motorola processor.

All data transfers through the microport are two bytes long. This requires the transmission of a Command/ Address byte followed by the data byte to be written to or read from the addressed register. $\overline{CS}$ must remain low for the duration of this two-byte transfer. As shown in Figures 8 and 9, the falling edge of $\overline{CS}$ indicates to the MT9315 that a microport transfer is about to begin. The first 8 clock cycles of SCLK after the falling edge of $\overline{CS}$ are always used to receive the Command/Address byte from the microcontroller. The Command/Address byte contains information detailing whether the second byte transfer will be a read or a write operation and at what address. The next 8 clock cycles are used to transfer the data byte between the MT9315 and the microcontroller. At the end of the two-byte transfer, $\overline{CS}$ is brought high again to terminate the session. The rising edge of $\overline{CS}$ will tri-state the DATA1 pin. The DATA1 pin will remain tri-stated as long as $\overline{CS}$ is high.

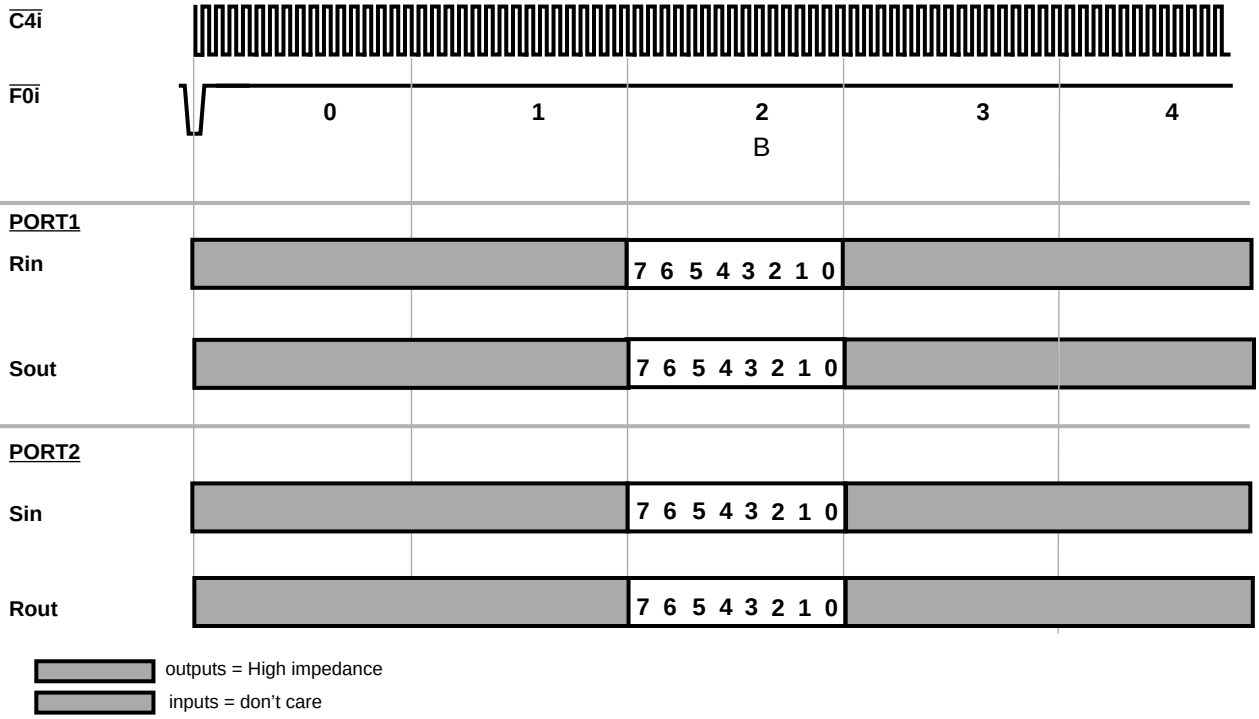
Intel processors utilize Least Significant Bit (LSB) first transmission while Motorola/National processors use Most Significant Bit (MSB) first transmission. The MT9315 microport automatically accommodates these two schemes for normal data bytes. However, to ensure timely decoding of the R/$\overline{W}$ and address information, the Command/Address byte is defined differently for Intel and Motorola/National operations. Refer to the relative timing diagrams of Figure 8 and Figure 9.

Receive data bits are sampled on the rising edge of SCLK while transmit data is clocked out on the falling edge of SCLK. Detailed microport timing is shown in Figure 13 and Figure 14.



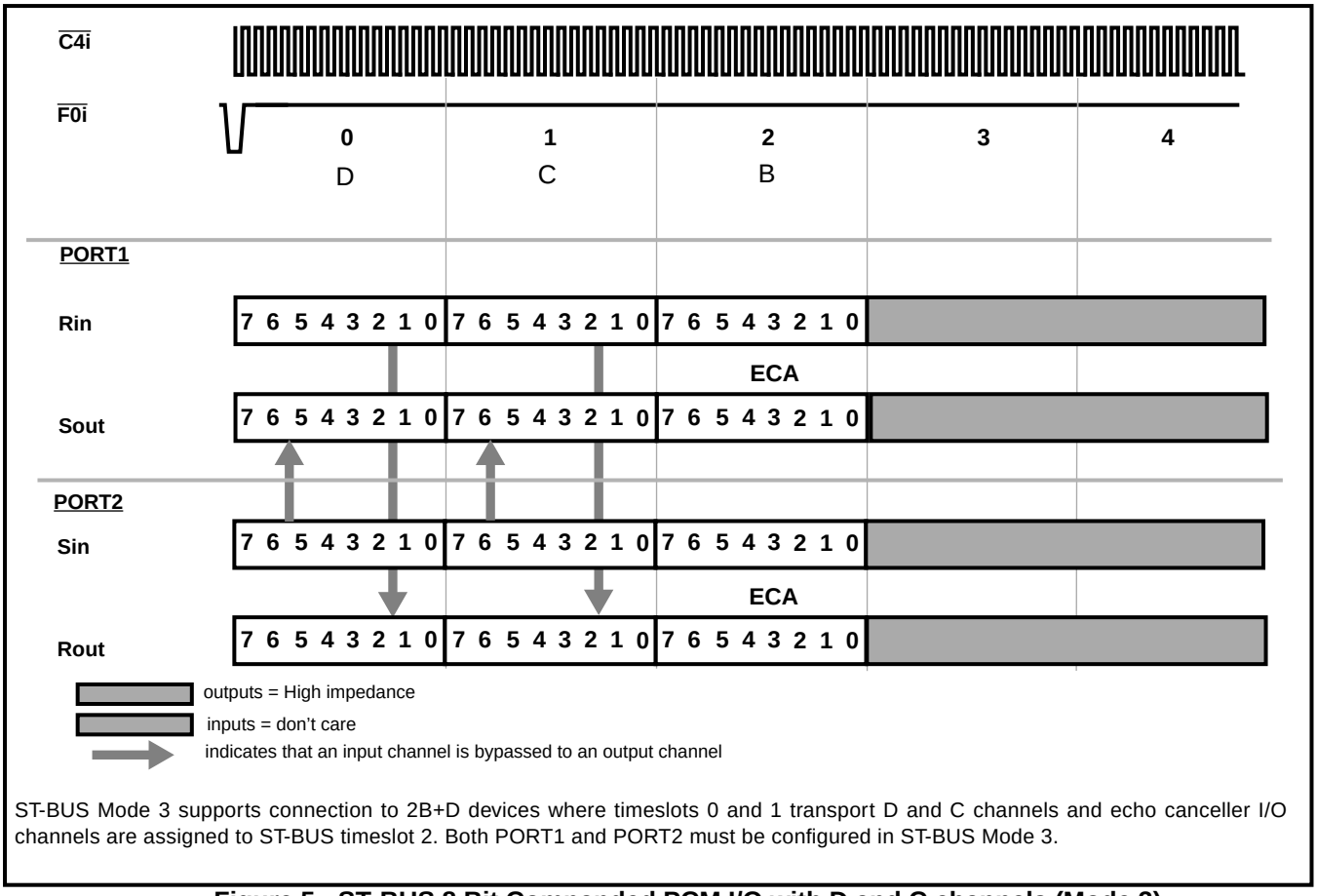
In ST-BUS Mode 1, echo canceller I/O channels are assigned to ST-BUS timeslot 0. Note that the user could configure PORT1 and PORT2 into different ST-BUS modes.

Figure 3 - ST-BUS 8 Bit Companded PCM I/O on Timeslot 0 (Mode 1)



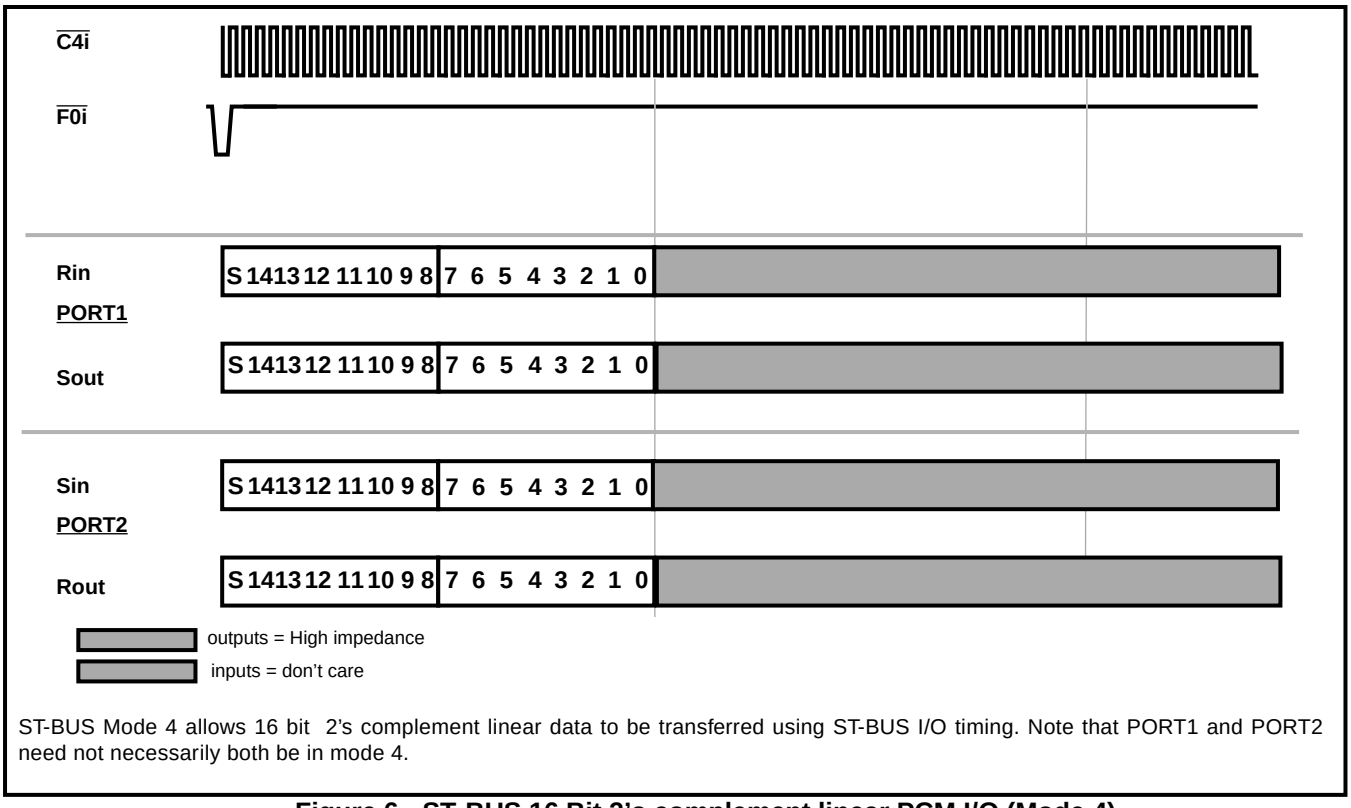
In ST-BUS Mode 2, echo canceller I/O channels are assigned to ST-BUS timeslot 2. Note that the user could configure PORT1 and PORT2 into different ST-BUS modes.

Figure 4 - ST-BUS 8 Bit Companded PCM I/O on Timeslot 2 (Mode 2)



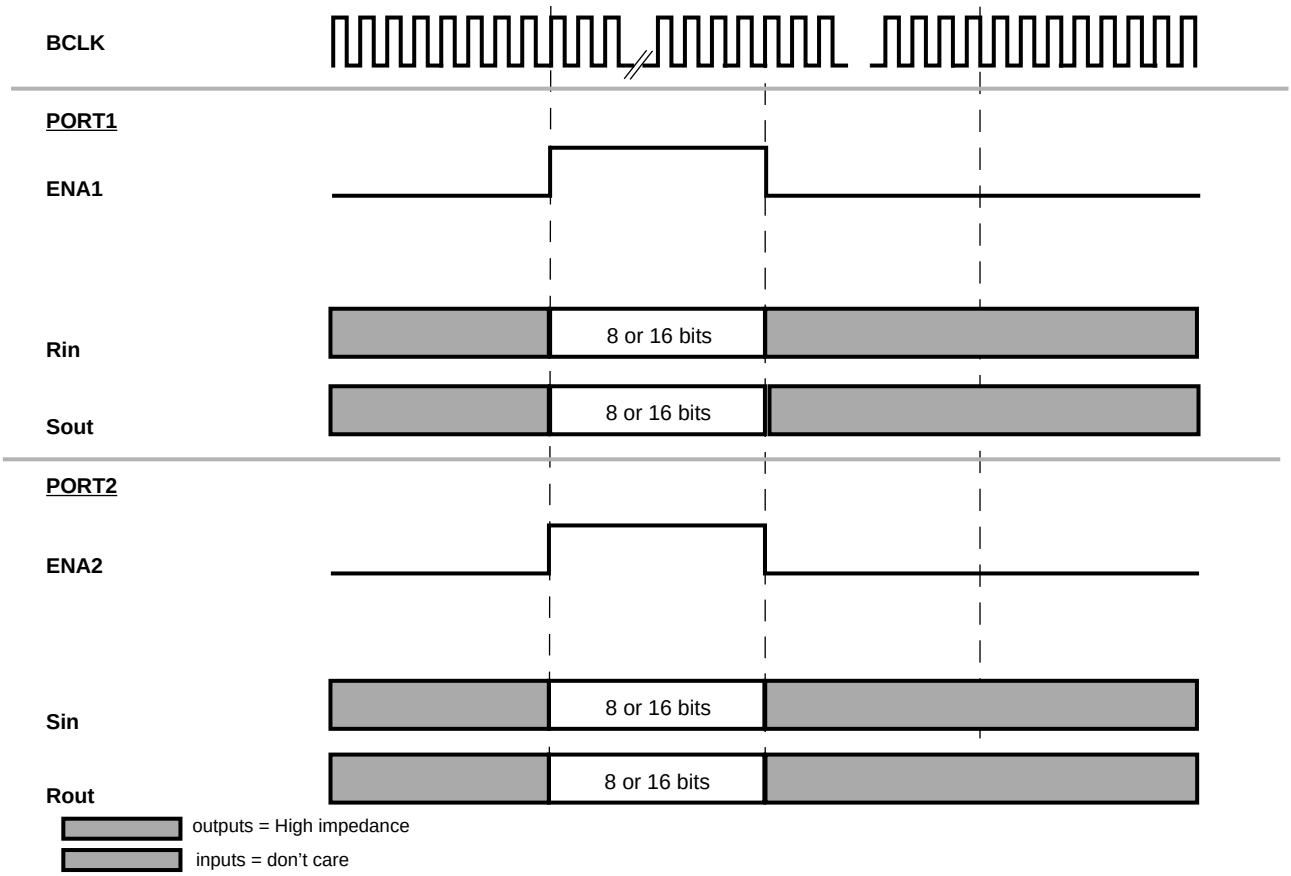
ST-BUS Mode 3 supports connection to 2B+D devices where timeslots 0 and 1 transport D and C channels and echo canceller I/O channels are assigned to ST-BUS timeslot 2. Both PORT1 and PORT2 must be configured in ST-BUS Mode 3.

Figure 5 - ST-BUS 8 Bit Companded PCM I/O with D and C channels (Mode 3)



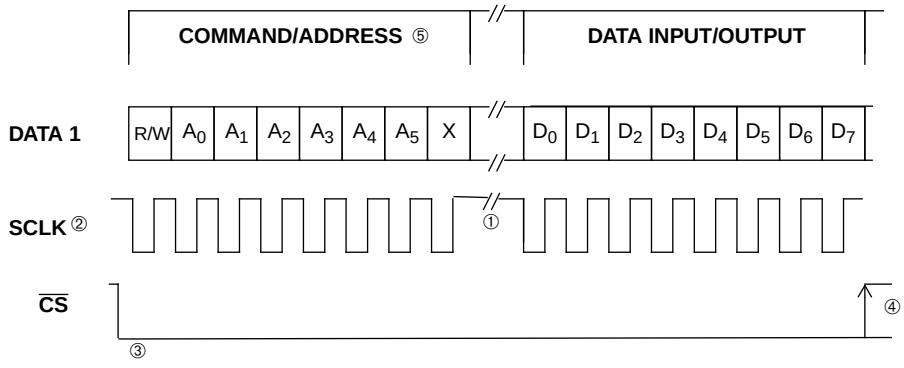
ST-BUS Mode 4 allows 16 bit 2's complement linear data to be transferred using ST-BUS I/O timing. Note that PORT1 and PORT2 need not necessarily both be in mode 4.

Figure 6 - ST-BUS 16 Bit 2's complement linear PCM I/O (Mode 4)



Note that the two ports are independent so that, for example, PORT1 can operate with 8 bit enable strobes and PORT2 can operate with 16 bit enable strobes.

Figure 7 - SSI Operation



① This delay is due to internal processor timing and is equal to Tsch time. The delay is transparent to MT9315.

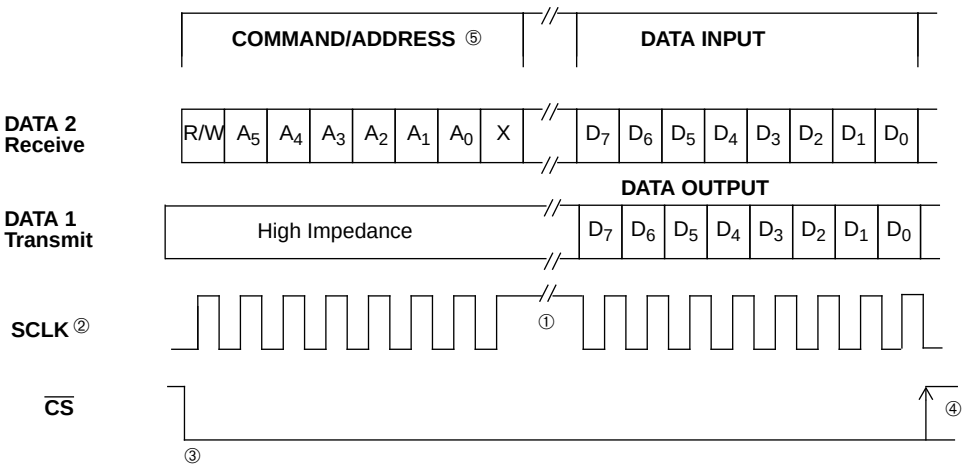
② The MT9315: latches receive data on the rising edge of SCLK
outputs transmit data on the falling edge of SCLK

③ The falling edge of $\overline{CS}$ indicates that a COMMAND/ADDRESS byte will be transmitted from the microprocessor. The subsequent byte is always data followed by $\overline{CS}$ returning high.

④ A new COMMAND/ADDRESS byte may be loaded only by $\overline{CS}$ cycling high then low again.

⑤ The COMMAND/ADDRESS byte contains: 1 bit - Read/$\overline{Write}$
6 bits - Addressing Data
1 bit - Unused

Figure 8 - Serial Microport Timing for Intel Mode 0



① This delay is due to internal processor timing and is equal to Tsch time. The delay is transparent to MT9315.

② The MT9315: latches receive data on the rising edge of SCLK
outputs transmit data on the falling edge of SCLK

③ The falling edge of $\overline{CS}$ indicates that a COMMAND/ADDRESS byte will be transmitted from the microprocessor. The subsequent byte is always data followed by $\overline{CS}$ returning high.

④ A new COMMAND/ADDRESS byte may be loaded only by $\overline{CS}$ cycling high then low again.

⑤ The COMMAND/ADDRESS byte contains: 1 bit - Read/$\overline{Write}$
6 bits - Addressing Data
1 bit - Unused

Figure 9 - Serial Microport Timing for Motorola Mode 00 or National Microwire

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage	V_{DD}-V_{SS}	-0.3	7.0	V
2	Input Voltage	V_i	V_{SS}-0.3	V_{DD}+ 0.3	V
3	Output Voltage Swing	V_o	V_{SS}-0.3	V_{DD}+ 0.3	V
4	Continuous Current on any digital pin	$I_{i/o}$		±20	mA
5	Storage Temperature	T_{ST}	-65	150	°C
6	Package Power Dissipation	P_D(5v)		500	mW

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Supply Voltage	V_{DD}	4.5	5.0	5.5	V	
2	TTL Input High Voltage		2.4		V_{DD}	V	
3	TTL Input Low Voltage		V_{SS}		0.4	V	
4	CMOS Input High Voltage		2.1		V_{DD}	V	
5	CMOS Input Low Voltage		V_{SS}		0.5	V	
6	Operating Temperature	T_A	-40		+85	°C	

Echo Return Limits -

	Characteristics	Min	Typ	Max	Units	Test Conditions
1	Acoustic Echo Return			0	dB	Measured from Rout -> Sin
2	Line Echo Return			0	dB	Measured from Sout -> Rin

DC Electrical Characteristics*- Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Conditions/Notes
1	Standby Supply Current:	I_{CC}			60	µA	$\overline{PWRDN}$ = 0
	Operating Supply Current:	I_{DD}		50		mA	$\overline{PWRDN}$ = 1, clocks active
2	Input HIGH voltage (TTL)	V_{IH}	2.0			V	All except MCLK,Sin,Rin
3	Input LOW voltage (TTL)	V_{IL}			0.8	V	All except MCLK,Sin,Rin
4	Input HIGH voltage (CMOS)	V_{IHC}	0.7V_{DD}			V	MCLK,Sin,Rin
5	Input LOW voltage (CMOS)	V_{ILC}			0.3V_{DD}	V	MCLK,Sin,Rin
6	Input leakage current	I_{IH}/I_{IL}		0.1	10	µA	V_{IN}=V_{SS} to V_{DD}
7	High level output voltage	V_{OH}	0.9V_{DD}			V	I_{OH}=2.5mA
8	Low level output voltage	V_{OL}			0.1V_{DD}	V	I_{OL}=5.0mA
9	High impedance leakage	I_{OZ}		1	10	µA	V_{IN}=V_{SS} to V_{DD}
10	Output capacitance	C_o		10		pF	

DC Electrical Characteristics*- Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Conditions/Notes
11	Input capacitance	C_i		8		pF	
12	$\overline{PWRDN}$ Positive Threshold Voltage Hysteresis Negative Threshold Voltage	 V+ V_H V-	 $0.75V_{DD}$	 1.0	 $0.25V_{DD}$	 V V V	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
*DC Electrical Characteristics are over recommended temperature and supply voltage.

AC Electrical Characteristics† - Serial Data Interfaces - Voltages are with respect to ground (V_{SS}) unless otherwise stated

	Characteristics	Sym	Min	Typ	Max	Units	Test Notes
1	MCLK Clock High	t_{MCH}	20			ns	
2	MCLK Clock Low	t_{MCL}	20			ns	
3	MCLK Frequency	f_{CLK}	19.15		20.5	MHz	
4	BCLK/$\overline{C4i}$ Clock High	t_{BCH}, t_{C4H}	90			ns	
5	BCLK/$\overline{C4i}$ Clock Low	t_{BLL}, t_{C4L}	90			ns	
6	BCLK/$\overline{C4i}$ Period	t_{BCP}	240		7900	ns	
7	SSI Enable Strobe to Data Delay (first bit)	t_{SD}	80			ns	C_L=150pF
8	SSI Data Output Delay (excluding first bit)	t_{DD}	80			ns	C_L=150pF
9	SSI Output Active to High Impedance	t_{AHZ}	80			ns	C_L=150pF
10	SSI Enable Strobe Signal Setup	t_{SSS}	10		t_{BCP} -15	ns	
11	SSI Enable Strobe Signal Hold	t_{SSH}	15		t_{BCP} -10	ns	
12	SSI Data Input Setup	t_{DIS}	10			ns	
13	SSI Data Input Hold	t_{DIH}	15			ns	
14	$\overline{F0i}$ Setup	t_{F0iS}	20		150	ns	
15	$\overline{F0i}$ Hold	t_{F0iH}	20		150	ns	
16	ST-BUS Data Output delay	t_{DSD}	80			ns	C_L=150pF
17	ST-BUS Output Active to High Impedance	t_{ASHZ}	80			ns	C_L=150pF
18	ST-BUS Data Input Hold time	t_{DSH}	20			ns	
19	ST-BUS Data Input Setup time	t_{DSS}	20			ns	

† Timing is over recommended temperature and power supply voltages.

AC Electrical Characteristics† - Microport Timing

	Characteristics	Sym	Min	Typ	Max	Units	Test Notes
1	Input Data Setup	t_{IDS}	100			ns	
2	Input Data Hold	t_{IDH}	30			ns	
3	Output Data Delay	t_{ODD}	100			ns	C_L=150pF
4	Serial Clock Period	t_{SCP}	500			ns	
5	SCLK Pulse Width High	t_{SCH}	250			ns	
6	SCLK Pulse Width Low	t_{SCL}	250			ns	
7	$\overline{CS}$ Setup-Intel	t_{CSSI}	200			ns	
8	$\overline{CS}$ Setup-Motorola	t_{CSSM}	100			ns	
9	$\overline{CS}$ Hold	t_{CSH}	100			ns	
10	$\overline{CS}$ to Output High Impedance	t_{OHZ}	100			ns	C_L=150pF

† Timing is over recommended temperature range and recommended power supply voltages.

Characteristic	Symbol	TTL Pin	CMOS Pin	Units
TTL reference level	V_{TT}	1.5	-	V
CMOS reference level	V_{CT}	-	$0.5*V_{DD}$	V
Input HIGH level	V_H	2.4	$0.9*V_{DD}$	V
Input LOW level	V_L	0.4	$0.1*V_{DD}$	V
Rise/Fall HIGH measurement point	V_{HM}	2.0	$0.7*V_{DD}$	V
Rise/Fall LOW measurement point	V_{HL}	0.8	$0.3*V_{DD}$	V

Table 8 - Reference Level Definition for Timing Measurements

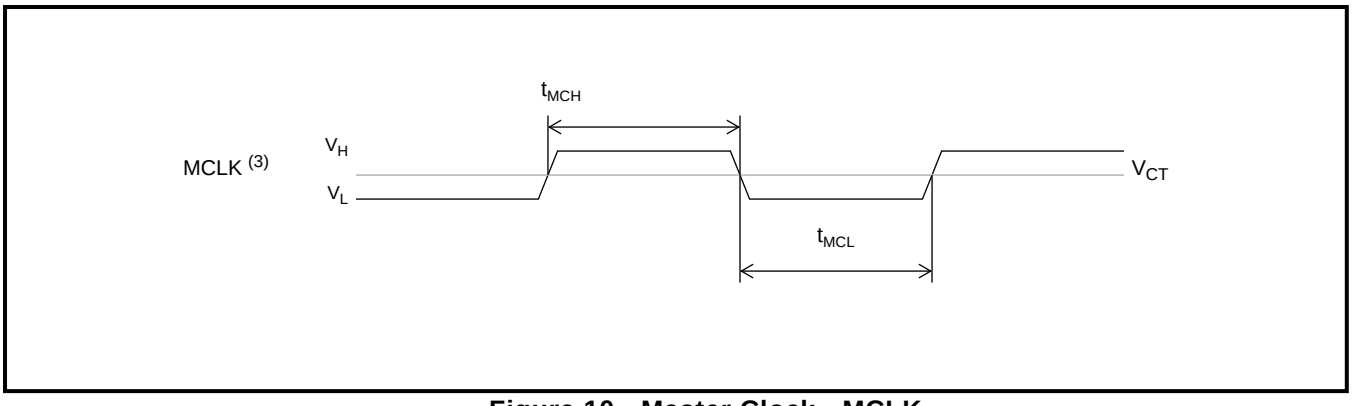


Figure 10 - Master Clock - MCLK

Notes: 1. CMOS output
2. TTL input compatible
3. CMOS input
(see Table 8 for symbol definitions)

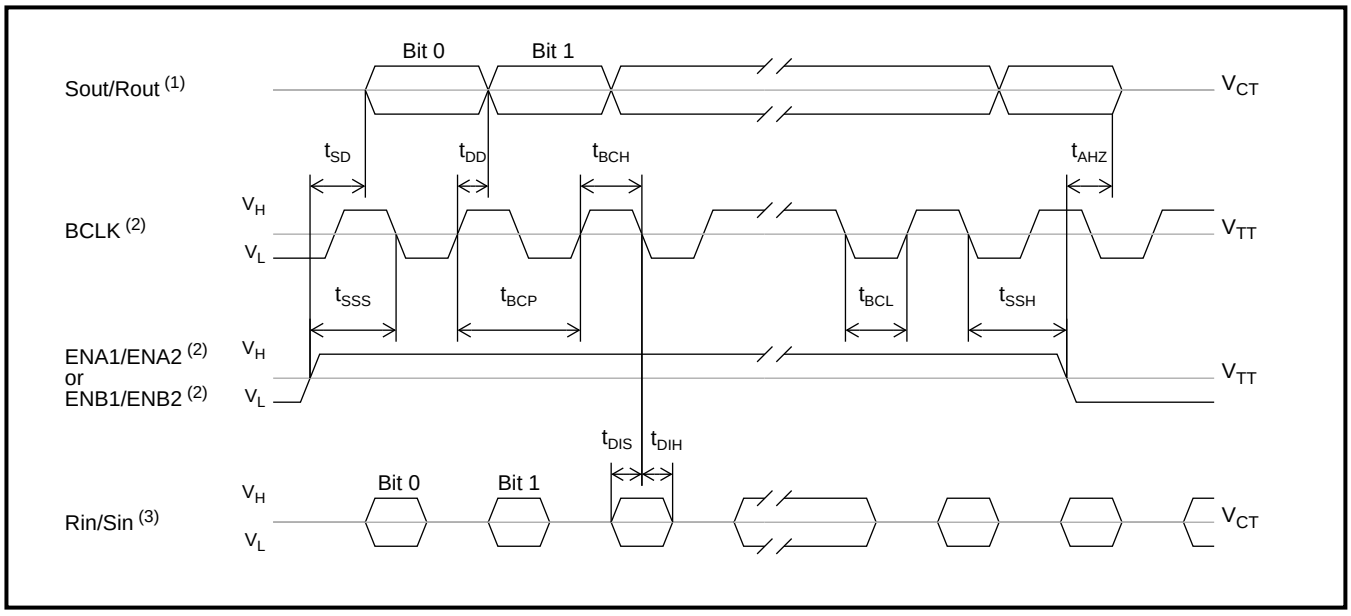


Figure 11 - SSI Data Port Timing

Notes: 1. CMOS output
2. TTL input compatible
3. CMOS input
(see Table 8 for symbol definitions)

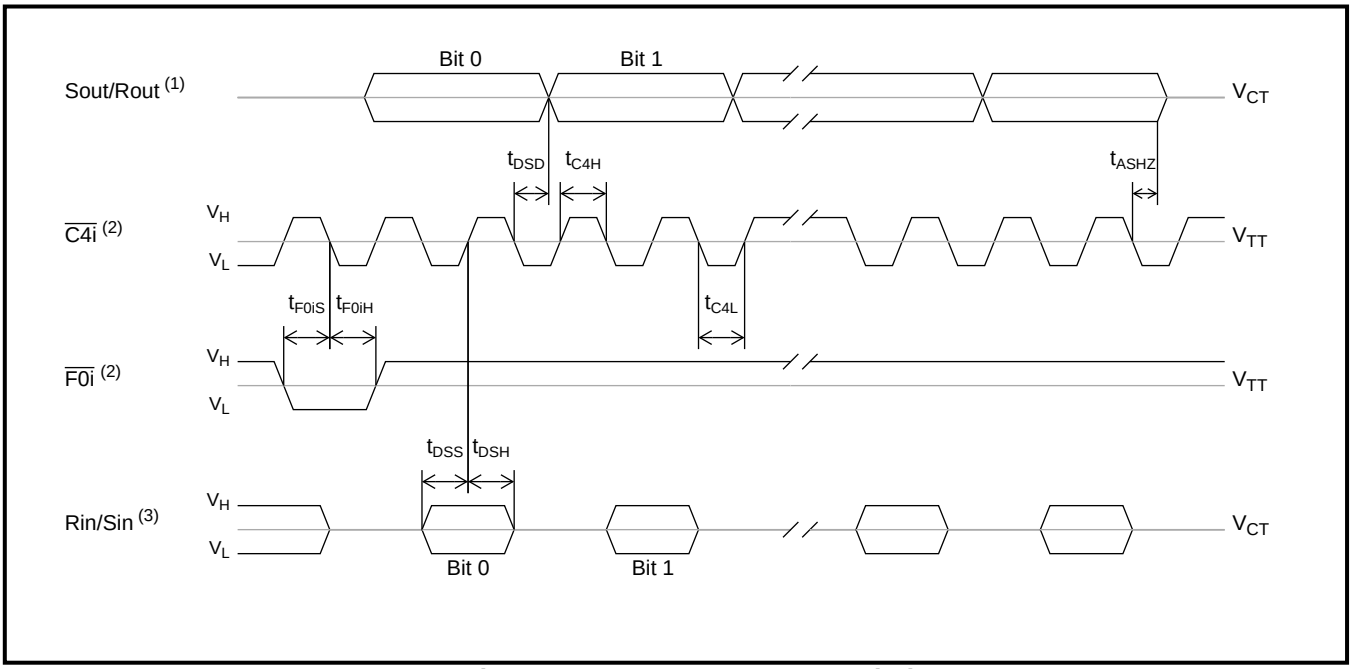


Figure 12 - ST-BUS Data Port Timing

Notes: 1. CMOS output
2. TTL input compatible
3. CMOS input
(see Table 8 for symbol definitions)

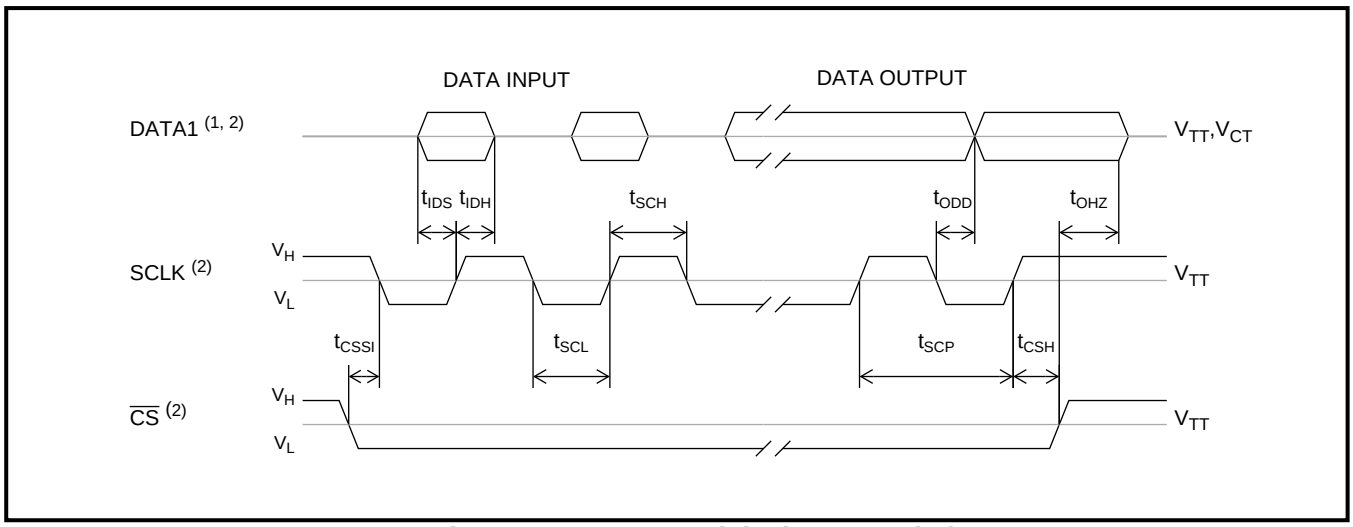


Figure 13 - INTEL Serial Microport Timing

Notes: 1. CMOS output
2. TTL input compatible
3. CMOS input
(see Table 8 for symbol definitions)

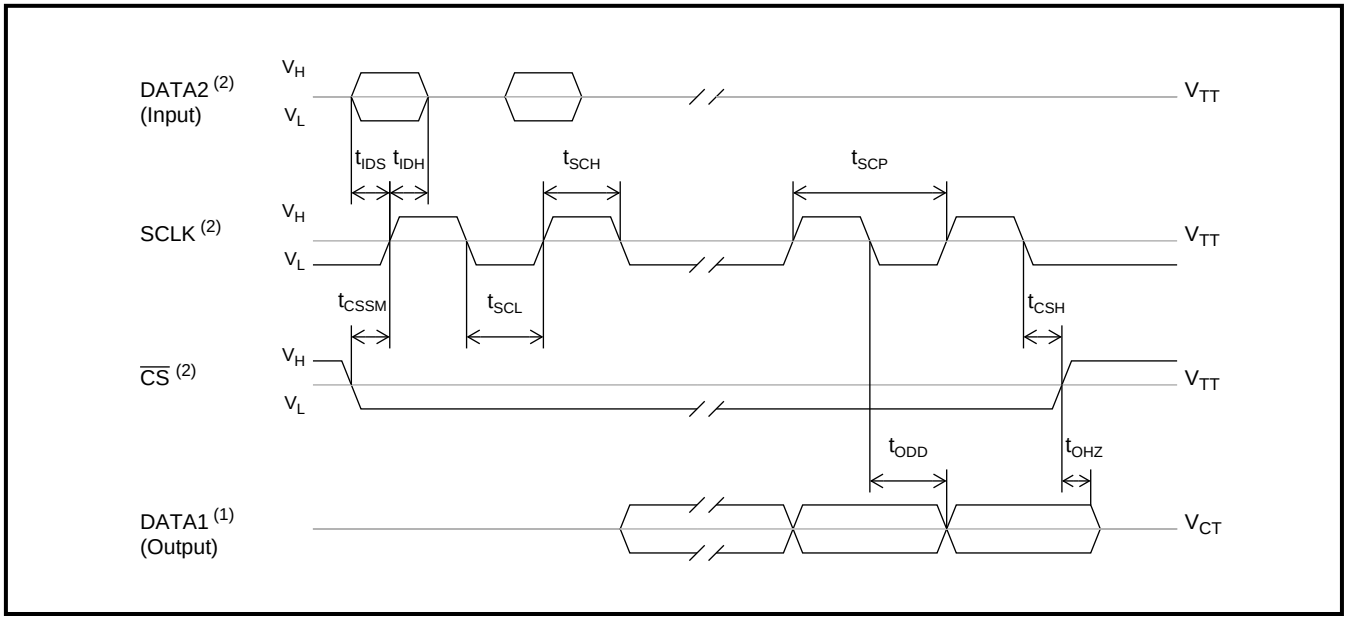


Figure 14 - Motorola Serial Microport Timing

Notes: 1. CMOS output
2. TTL input compatible
3. CMOS input
(see Table 8 for symbol definitions)

Register Summary

Address: 00h R/W	Main Control Register (MC)							
Power Up Reset 00h	7 MSB LIMIT	6 MUTE_R	5 MUTE_S	4 BYPASS	3 NB-	2 AGC-	1 AH-	0 RESET LSB

RESET	When high, the power initialization routine is executed presetting all registers to default values. This bit automatically clears itself to'0' when reset is complete.
AH-	When high, the Howling detector is disabled and when low the Howling detector is enabled.
AGC-	When high, AGC is disabled and when low AGC is enabled
NB-	When high, Narrowband signal detectors in Rin and Sin paths are disabled and when low the signal detectors are enabled
BYPASS	When high, the Send and Receive paths are transparently by-passed from input to output and when low the Send and Receive paths are not bypassed
MUTE_S	When high, the Sin path is muted to quite code (after the NLP) and when low the Sin path is not muted
MUTE_R	When high, the Rin path is muted to quite code (after the NLP) and when low the Rin path is not muted
LIMIT	When high, the 2-bit shift mode is enabled in conjunction with bit 7 of LEC register and when low 2-bit shift mode is disabled

Address: 21h R/W	Acoustic Echo Canceller Control Register (AEC)							
Power Up Reset 00h	7 MSB P-	6 ASC-	5 NLP-	4 INJ-	3 HPF-	2 HCLR	1 ADAPT-	0 ECBY LSB

ECBY	When high, the Echo estimate from the filter is not substracted from the Send path, when low the estimate is substracted
ADAPT-	When high, the Echo canceller adaptation is disabled and when low the adaptation is enabled
HCLR	When high, Adaptive filter coefficients are cleared and when low the filter coefficients are not cleared
HPF-	When high, Offset nulling filter is bypassed in the Sin/Sout path and when low the Offset nulling filter in not bypassed
INJ-	When high, the Noise filtering process is disabled in the NLP and when low the Noise filtering process is enabled
NLP-	When high, the Non Linear Processor is disabled in the Sin/Sout path and when low the NLP is enabled
ASC-	When high, the Internal Adaptation speed control is disabled and when low the Adaptation speed is enabled
P-	When high, the Exponential weighting function for the adaptive filter is disabled and when low the weighting function is enabled

Address: 01h R/W	Line Echo Canceller Control Register (LEC)							
Power Up Reset 00h	7 MSB SHFT	6 ASC-	5 NLP-	4 INJ-	3 HPF-	2 HCLR	1 ADAPT-	0 ECBY LSB

ECBY	When high, the Echo estimate from the filter is not substracted from the Send path, when low the estimate is substracted
ADAPT-	When high, the Echo canceller adaptation is disabled and when low the adaptation is enabled
HCLR	When high, Adaptive filter coefficients are cleared and when low the filter coefficients are not cleared
HPF-	When high, Offset nulling filter is bypassed in the Rin/Rout path and when low the Offset nulling filter in not bypassed
INJ-	When high, the Noise filtering process is disabled in the NLP and when low the Noise filtering process is enabled
NLP-	When high, the Non Linear Processor is disabled in the Rin/Rout path and when low the NLP is enabled
ASC-	When high, the Internal Adaptation speed control is disabled and when low the Adaptation speed is enabled
SHFT	when high the 16-bit linear mode, inputs Sin, Rin, are shift right by 2 and outputs Sout, Rout are shift left by 2. This bit is ignored when 16-bit linear mode is not selected in both ports. This bit is also ignored if bit 7 of MC register is set to zero

Address: 22h Read	Acoustic Echo Canceller Status Register (ASR) (* Do not write to this register)
Power Up Reset 00h	MSB 7 - 6 ACMUND 5 HWLNG 4 - 3 NLPDC 2 DT 1 NB 0 NBS LSB
NBS	When high, the Narrowband signal has been detected in the Sin/Sout path and when low, the Narrowband signal has not been detected in the Sin/Sout path
NB	LOGICAL OR of the status bit NBS + NBR from LSR Register
DT	When high the Double Talk is detected and when low, the Double talk is not detected
NLPDC	When high, the NLP is activated and when low the NLP is not activated
-	RESERVED.
HWLNG	When high, Howling is occurring in the loop and when low, no Howling is detected
ACMUND	When high, No active signal in the Rin/Rout path
-	RESERVED.

Address: 02h Read	Line Echo Canceller Status Register (LSR) (* Do not write to this register)
Power Up Reset 00h	7 - 6 - 5 - 4 - 3 NLPC 2 DT 1 NB 0 NBR LSB
NBR	MSB When high, a narrowband signal has been detected in the Receive (Rin) path. When low no narrowband signal is not detected in the Rin path
NB	This bit indicates a LOGICAL-OR of Stattus bits NBR + NBS (from ASR Register)
DT	When high, double-talk is detected and when low double-talk is not detected
NLPC	When high, NLP is actiivated and when low NLP is not activated
-	RESERVED. .
-	
-	
--	

Address: 20h R/W	Receive Gain Control Register (RGC)
Power Up Reset 6Dh	MSB 7 - 6 - 5 - 4 - 3 G3 2 G2 1 G1 0 GO LSB
G0	User Gain Control on the Rin/Rout path (Tolerance of gains: +/- 0.15 dB). The hexadecimal number represents G3 to G0 value in the table below.
G1	
G2	
G3	
-	RESERVED
-	
-	
-	

Gain Values for Receive Gain Control Register Bit G3 to G0 (RGC)

0h	-24dB	4h	-12dB	8h	0 dB	Ch	+12 dB
1h	-21dB	5h	-9 dB	9h	+ 3 dB	Dh	+ 15 dB
2h	-18dB	6h	-6 dB	Ah	+ 6 dB	Eh	+ 18 dB
3h	-15dB	7h	-3 dB	Bh	+9 dB	Fh	+ 21 dB

Address: 16h Read	Receive (Rin) Peak Detect Register 1 (RIPD1)							
Power Up Reset 00h	7 MSB RIPD$_7$	6 RIPD$_6$	5 RIPD$_5$	4 RIPD$_4$	3 RIPD$_3$	2 RIPD$_2$	1 RIPD$_1$	0 RIPD$_0$ LSB
RIPD$_0$	These peak detector registers allow the user to monitor the receive in signal (Rin) peak level at reference point R1 (see Figure #1). The information is in 16-bit 2's complement linear coded format presented in two 8 bit registers. The high byte is in Register 2 and the low byte is in Register 1.							
RIPD$_1$								
RIPD$_2$								
RIPD$_3$								
RIPD$_4$								
RIPD$_5$								
RIPD$_6$								
RIPD$_7$								

Address: 17h Read	Receive (Rin) Peak Detect Register 2 (RIPD2)							
Power Up Reset 00h	7 MSB RIPD$_{15}$	6 RIPD$_{14}$	5 RIPD$_{13}$	4 RIPD$_{12}$	3 RIPD$_{11}$	2 RIPD$_{10}$	1 RIPD$_9$	0 RIPD$_8$ LSB
RIPD$_8$	See Above Description							
RIPD$_9$								
RIPD$_{10}$								
RIPD$_{11}$								
RIPD$_{12}$								
RIPD$_{13}$								
RIPD$_{14}$								
RIPD$_{15}$								

Address: 18h Read	Receive (Rin) ERROR Peak Detect Register 1 (REPD1)							
Power Up Reset 00h	7 MSB REPD$_7$	6 REPD$_6$	5 REPD$_5$	4 REPD$_4$	3 REPD$_3$	2 REPD$_2$	1 REPD$_1$	0 REPD$_0$ LSB
REPD$_0$	These peak detector registers allow the user to monitor the error signal peak level at reference point R2 (see Figure #1). The information is in 16-bit 2's complement linear coded format presented in two 8 bit registers. The high byte is in Register 2 and the low byte is in Register 1.							
REPD$_1$								
REPD$_2$								
REPD$_3$								
REPD$_4$								
REPD$_5$								
REPD$_6$								
REPD$_7$								

Address: 19h Read	Receive (Rin) ERROR Peak Detect Register 2 (REPD2)							
Power Up Reset 00h	7 MSB $REPD_{15}$	6 $REPD_{14}$	5 $REPD_{13}$	4 $REPD_{12}$	3 $REPD_{11}$	2 $REPD_{10}$	1 $REPD_{9}$	0 $REPD_{8}$ LSB
REPD8	See above description							
REPD9								
REPD10								
REPD11								
REPD12								
REPD13								
REPD14								
REPD15								

Address: 3Ah Read	Receive (Rout) Peak Detect Register 1 (ROPD1)							
Power Up Reset 00h	7 MSB $ROPD_{7}$	6 $ROPD_{6}$	5 $ROPD_{5}$	4 $ROPD_{4}$	3 $ROPD_{3}$	2 $ROPD_{2}$	1 $ROPD_{1}$	0 $ROPD_{0}$ LSB
$ROPD_{0}$	These peak detector registers allow the user to monitor the receive out signal (Rout) peak level at reference point R3 (see Figure #1). The information is in 16-bit 2's complement linear coded format presented in two 8 bit registers. The high byte is in Register 2 and the low byte is in Register 1.							
$ROPD_{1}$								
$ROPD_{2}$								
$ROPD_{3}$								
$ROPD_{4}$								
$ROPD_{5}$								
$ROPD_{6}$								
$ROPD_{7}$								

Address: 3Bh Read	Receive (Rout) Peak Detect Register 2 (ROPD2)							
Power Up Reset 00h	7 MSB $ROPD_{15}$	6 $ROPD_{14}$	5 $ROPD_{13}$	4 $ROPD_{12}$	3 $ROPD_{11}$	2 $ROPD_{10}$	1 $ROPD_{9}$	0 $ROPD_{8}$ LSB
$ROPD_{8}$	See Above description							
$ROPD_{9}$								
$ROPD_{10}$								
$ROPD_{11}$								
$ROPD_{12}$								
$ROPD_{13}$								
$ROPD_{14}$								
$ROPD_{15}$								

Address: 36h Read	Send (Sin) Peak Detect Register 1 (SIPD1)							
Power Up Reset 00h	7 MSB $SIPD_7$	6 $SIPD_6$	5 $SIPD_5$	4 $SIPD_4$	3 $SIPD_3$	2 $SIPD_2$	1 $SIPD_1$	0 $SIPD_0$ LSB
$SIPD_0$	These peak detector registers allow the user to monitor the receive in signal (Sin) peak level at reference point S1 (see Figure #1). The information is in 16-bit 2's complement linear coded format presented in two 8 bit registers. The high byte is in Register 2 and the low byte is in Register 1.							
$SIPD_1$								
$SIPD_2$								
$SIPD_3$								
$SIPD_4$								
$SIPD_5$								
$SIPD_6$								
$SIPD_7$								

Address: 37h Read	Send (Sin) Peak Detect Register 2 (SIPD2)							
Power Up Reset 00h	7 MSB $SIPD_{15}$	6 $SIPD_{14}$	5 $SIPD_{13}$	4 $SIPD_{12}$	3 $SIPD_{11}$	2 $SIPD_{10}$	1 $SIPD_9$	0 $SIPD_8$ LSB
$SIPD_8$	See above description							
$SIPD_9$								
$SIPD_{10}$								
$SIPD_{11}$								
$SIPD_{12}$								
$SIPD_{13}$								
$SIPD_{14}$								
$SIPD_{15}$								

Address: 38h Read	Send ERROR Peak Detect Register 1 (SEPD1)							
Power Up Reset 00h	7 MSB $SEPD_7$	6 $SEPD_6$	5 $SEPD_5$	4 $SEPD_4$	3 $SEPD_3$	2 $SEPD_2$	1 $SEPD_1$	0 $SEPD_0$ LSB
$SEPD_0$	These peak detector registers allow the user to monitor the error signal peak level in the send path at reference point S2 (see Figure #1). The information is in 16-bit 2's complement linear coded format presented in two 8 bit registers. The high byte is in Register 2 and the low byte is in Register 1.							
$SEPD_1$								
$SEPD_2$								
$SEPD_3$								
$SEPD_4$								
$SEPD_5$								
$SEPD_6$								
$SEPD_7$								

Address: 39h Read	Send ERROR Peak Detect Register 2 (SEPD2)							
Power Up Reset 00h	7 MSB $SEPD_{15}$	6 $SEPD_{14}$	5 $SEPD_{13}$	4 $SEPD_{12}$	3 $SEPD_{11}$	2 $SEPD_{10}$	1 $SEPD_9$	0 $SEPD_8$ LSB
SEPD8	See Above description							
SEPD9								
SEPD10								
SEPD11								
SEPD12								
SEPD13								
SEPD14								
SEPD15								

Address: 1Ah Read	Send (Sout) Peak Detect Register 1 (SOPD1)							
Power Up Reset 00h	7 MSB $SOPD_7$	6 $SOPD_6$	5 $SOPD_5$	4 $SOPD_4$	3 $SOPD_3$	2 $SOPD_2$	1 $SOPD_1$	0 $SOPD_0$ LSB
$SOPD_0$	These peak detector registers allow the user to monitor the Send out signal (Sout) peak level at reference point S3 (see Figure #1). The information is in 16-bit 2's complement linear coded format presented in two 8 bit registers. The high byte is in Register 2 and the low byte is in Register 1.							
$SOPD_1$								
$SOPD_2$								
$SOPD_3$								
$SOPD_4$								
$SOPD_5$								
$SOPD_6$								
$SOPD_7$								

Address: 1Bh Read	Send (Sout) Peak Detect Register 2 (SOPD2)							
Power Up Reset 00h	7 MSB $SOPD_{15}$	6 $SOPD_{14}$	5 $SOPD_{13}$	4 $SOPD_{12}$	3 $SOPD_{11}$	2 $SOPD_{10}$	1 $SOPD_9$	0 $SOPD_8$ LSB
$SOPD_8$	See Above description							
$SOPD_9$								
$SOPD_{10}$								
$SOPD_{11}$								
$SOPD_{12}$								
$SOPD_{13}$								
$SOPD_{14}$								
$SOPD_{15}$								

Address: 3Ch R/W	Acoustic Echo Canceller Adaptation Speed Register 1 (A_AS1)							
Power Up Reset 00h	7 MSB	6	5	4	3	2	1	0 LSB
	A_AS_7	A_AS_6	A_AS_5	A_AS_4	A_AS_3	A_AS_2	A_AS_1	A_AS_0
A_AS_0	This register allows the user to program control the adaptation speed of the Acoustic Echo Canceller. This register value changes dynamically when the 'ASC-' bit in the Acoustic Echo Canceller Control Register is low. The 'ASC-' bit must be 1 when this register is under user control. The valid range is from 0000h to 7FFFh. The high byte is in Register 2 and the low byte is in Register 1. Smaller values correspond to slower adaptation speed.							
A_AS_1								
A_AS_2								
A_AS_3								
A_AS_4								
A_AS_5								
A_AS_6								
A_AS_7								

Address: 3Dh R/W	Acoustic Echo Canceller Adaptation Speed Register 2 (A_AS2)							
Power Up Reset 10h	7 MSB	6	5	4	3	2	1	0 LSB
	A_AS_{15}	A_AS_{14}	A_AS_{13}	A_AS_{12}	A_AS_{11}	A_AS_{10}	A_AS_9	A_AS_8
A_AS_8	See Above description							
A_AS_9								
A_AS_{10}								
A_AS_{11}								
A_AS_{12}								
A_AS_{13}								
A_AS_{14}								
A_AS_{15}								

Address: 1Ch R/W	Line Echo Canceller Adaptation Speed Register 1 (L_AS1)							
Power Up Reset 00h	7 MSB	6	5	4	3	2	1	0 LSB
	L_AS_7	L_AS_6	L_AS_5	L_AS_4	L_AS_3	L_AS_2	L_AS_1	L_AS_0
L_AS_0	This register allows the user to program control the adaptation speed of the Line Echo Canceller. This register value changes dynamically when the 'ASC-' bit in the Acoustic Echo Canceller Control Register is low. The 'ASC-' bit must be 1 when this register is under user control. The valid range is from 0000h to 7FFFh. The high byte is in Register 2 and the low byte is in Register 1. Smaller values correspond to slower adaptation speed.							
L_AS_1								
L_AS_2								
L_AS_3								
L_AS_4								
L_AS_5								
L_AS_6								
L_AS_7								

Address: 1Dh R/W	Line Echo Canceller Adaptation Speed Register 2 (L_AS2)							
Power Up Reset 08h	7 MSB	6	5	4	3	2	1	0 LSB
	L_AS_{15}	L_AS_{14}	L_AS_{13}	L_AS_{12}	L_AS_{11}	L_AS_{10}	L_AS_9	L_AS_8
L_AS_8	See Above description							
L_AS_9								
L_AS_{10}								
L_AS_{11}								
L_AS_{12}								
L_AS_{13}								
L_AS_{14}								
L_AS_{15}								

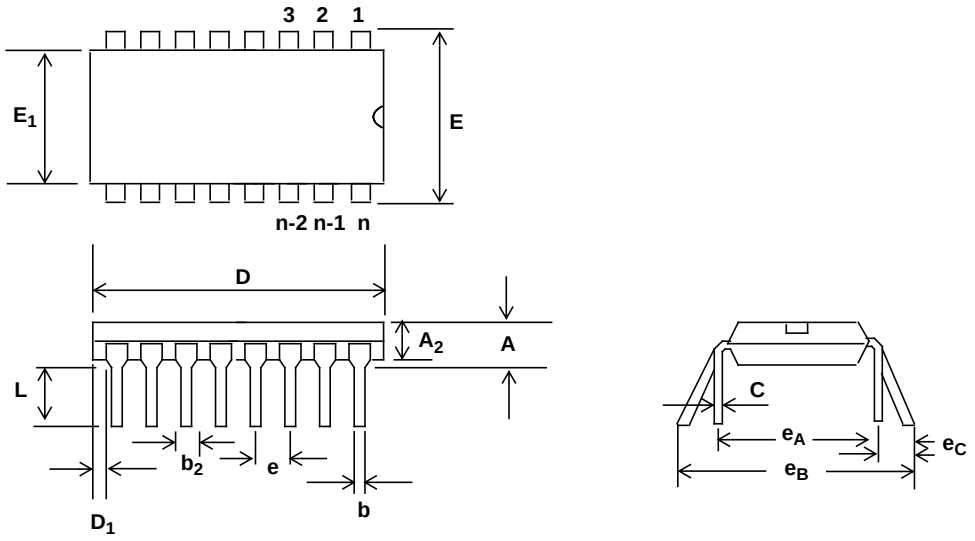
Address: 24h R/W	Rout Limiter Register 1 (RL1)							
Power Up Reset 80h	7 MSB	6	5	4	3	2	1	0 LSB
	L_0	-	-	-	-	-	-	-
-	RESERVED							
-								
-								
-								
-								
-								
-								
L_0	This bit is used in conjunction with Rout Limiter Register 2. (See description below.)							

Address: 25h R/W	Rout Limiter Register 2 (RL2)							
Power Up Reset 3Eh	7 MSB	6	5	4	3	2	1	0 LSB
	L_8	L_7	L_6	L_5	L_4	L_3	L_2	L_1
L_1	In conjunction with bit 7 (L_0) of the above (RL1) register, this register (RL2) allows the user to program the output Limiter threshold value in the Rout path. Default value is (1f40)h which is equal to 3.14dBmo Maximum value is (7FC0)h = 15 dBmo Minimum value is (0040)h = -38 dBmo							
L_2								
L_3								
L_4								
L_5								
L_6								
L_7								
L_8								

Address: 26h R/W	Sout Limiter Register (SL)							
Power Up Reset 3Dh	7 MSB	6	5	4	3	2	1	0 LSB
	L_4	L_3	L_2	L_1	L_0	-	-	-
-	RESERVED							
-								
-								
L_0	This register allows the user to program the output Limiter threshold value in the Rout path							
L_1								
L_2	Default value is (1f40)h which is equal to 3.14dBmo							
L_3	Maximum value is (7F40)h							
L_4								

Address: 03h Read	Device Revision Code Register (DRC)							
Power Up Reset 40h	7 MSB	6	5	4	3	2	1	0 LSB
	DRC_2	DRC_1	DRC_0	-	-	-	-	-
-	RESERVED							
-								
-								
-								
DRC_0	Revision code of the device (=02).							
DRC_1								
DRC_2								

Package Outlines



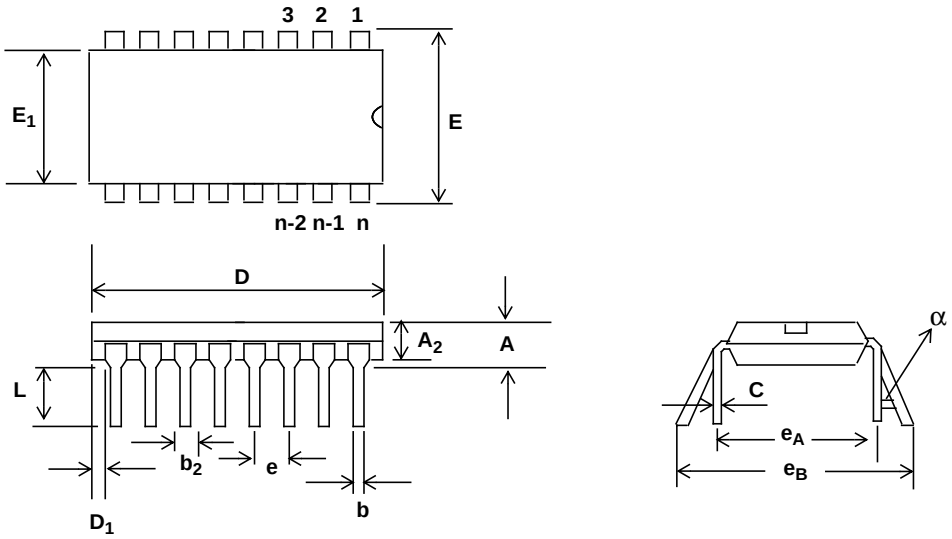
Notes:
1) Not to scale
2) Dimensions in inches
3) (Dimensions in millimeters)

Plastic Dual-In-Line Packages (PDIP) - E Suffix

DIM	8-Pin		16-Pin		18-Pin		20-Pin	
	Plastic		Plastic		Plastic		Plastic	
	Min	Max	Min	Max	Min	Max	Min	Max
A		0.210 (5.33)		0.210 (5.33)		0.210 (5.33)		0.210 (5.33)
A_2	0.115 (2.92)	0.195 (4.95)	0.115 (2.92)	0.195 (4.95)	0.115 (2.92)	0.195 (4.95)	0.115 (2.92)	0.195 (4.95)
b	0.014 (0.356)	0.022 (0.558)	0.014 (0.356)	0.022 (0.558)	0.014 (0.356)	0.022 (0.558)	0.014 (0.356)	0.022 (0.558)
b_2	0.045 (1.14)	0.070 (1.77)	0.045 (1.14)	0.070 (1.77)	0.045 (1.14)	0.070 (1.77)	0.045 (1.14)	0.070 (1.77)
C	0.008 (0.203)	0.014 (0.356)	0.008 (0.203)	0.014(0.356)	0.008 (0.203)	0.014 (0.356)	0.008 (0.203)	0.014 (0.356)
D	0.355 (9.02)	0.400 (10.16)	0.780 (19.81)	0.800 (20.32)	0.880 (22.35)	0.920 (23.37)	0.980 (24.89)	1.060 (26.9)
D_1	0.005 (0.13)		0.005 (0.13)		0.005 (0.13)		0.005 (0.13)	
E	0.300 (7.62)	0.325 (8.26)	0.300 (7.62)	0.325 (8.26)	0.300 (7.62)	0.325 (8.26)	0.300 (7.62)	0.325 (8.26)
E_1	0.240 (6.10)	0.280 (7.11)	0.240 (6.10)	0.280 (7.11)	0.240 (6.10)	0.280 (7.11)	0.240 (6.10)	0.280 (7.11)
e	0.100 BSC (2.54)		0.100 BSC (2.54)		0.100 BSC (2.54)		0.100 BSC (2.54)	
e_A	0.300 BSC (7.62)		0.300 BSC (7.62)		0.300 BSC (7.62)		0.300 BSC (7.62)	
L	0.115 (2.92)	0.150 (3.81)	0.115 (2.92)	0.150 (3.81)	0.115 (2.92)	0.150 (3.81)	0.115 (2.92)	0.150 (3.81)
e_B		0.430 (10.92)		0.430 (10.92)		0.430 (10.92)		0.430 (10.92)
e_C	0	0.060 (1.52)	0	0.060 (1.52)	0	0.060 (1.52)	0	0.060 (1.52)

NOTE: Controlling dimensions in parenthesis ( ) are in millimeters.

Package Outlines



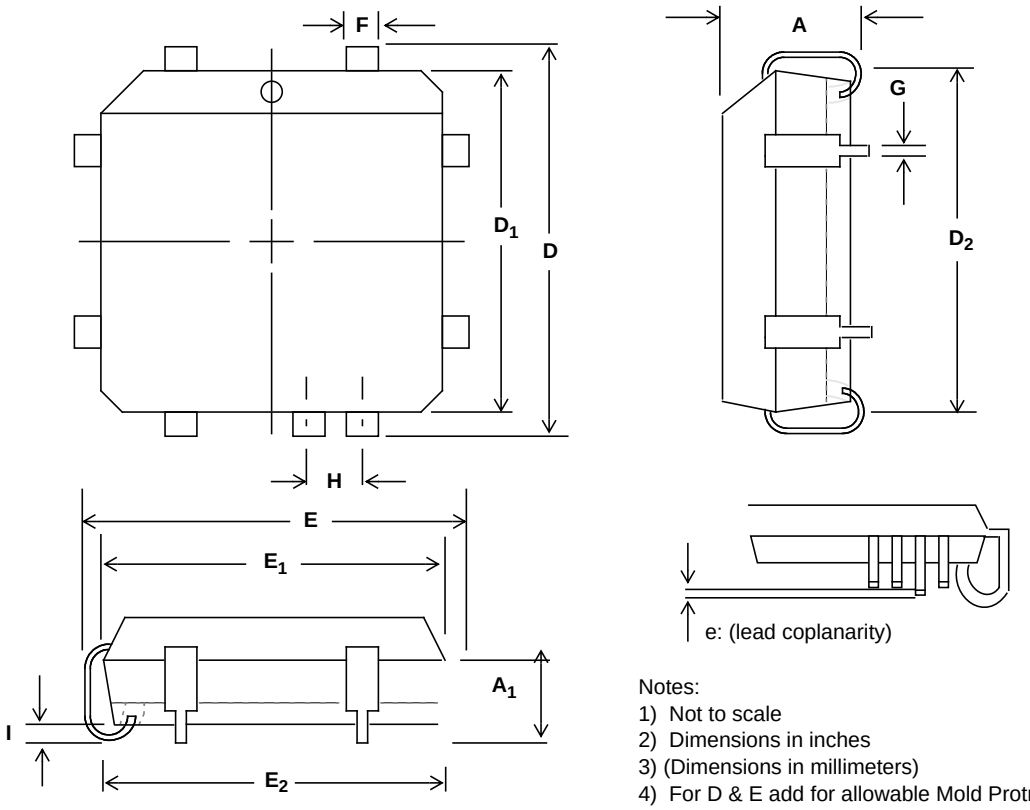
Notes:
1) Not to scale
2) Dimensions in inches
3) (Dimensions in millimeters)

Plastic Dual-In-Line Packages (PDIP) - E Suffix

DIM	22-Pin		24-Pin		28-Pin		40-Pin	
	Plastic		Plastic		Plastic		Plastic	
	Min	Max	Min	Max	Min	Max	Min	Max
A		0.210 (5.33)		0.250 (6.35)		0.250 (6.35)		0.250 (6.35)
A_2	0.125 (3.18)	0.195 (4.95)	0.125 (3.18)	0.195 (4.95)	0.125 (3.18)	0.195 (4.95)	0.125 (3.18)	0.195 (4.95)
b	0.014 (0.356)	0.022 (0.558)	0.014 (0.356)	0.022 (0.558)	0.014 (0.356)	0.022 (0.558)	0.014 (0.356)	0.022 (0.558)
b_2	0.045 (1.15)	0.070 (1.77)	0.030 (0.77)	0.070 (1.77)	0.030 (0.77)	0.070 (1.77)	0.030 (0.77)	0.070 (1.77)
C	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.015 (0.381)
D	1.050 (26.67)	1.120 (28.44)	1.150 (29.3)	1.290 (32.7)	1.380 (35.1)	1.565 (39.7)	1.980 (50.3)	2.095 (53.2)
D_1	0.005 (0.13)		0.005 (0.13)		0.005 (0.13)		0.005 (0.13)	
E	0.390 (9.91)	0.430 (10.92)	0.600 (15.24)	0.670 (17.02)	0.600 (15.24)	0.670 (17.02)	0.600 (15.24)	0.670 (17.02)
E			0.290 (7.37)	.330 (8.38)				
E_1	0.330 (8.39)	0.380 (9.65)	0.485 (12.32)	0.580 (14.73)	0.485 (12.32)	0.580 (14.73)	0.485 (12.32)	0.580 (14.73)
E_1			0.246 (6.25)	0.254 (6.45)				
e	0.100 BSC (2.54)		0.100 BSC (2.54)		0.100 BSC (2.54)		0.100 BSC (2.54)	
e_A	0.400 BSC (10.16)		0.600 BSC (15.24)		0.600 BSC (15.24)		0.600 BSC (15.24)	
e_A			0.300 BSC (7.62)					
e_B				0.430 (10.92)				
L	0.115 (2.93)	0.160 (4.06)	0.115 (2.93)	0.200 (5.08)	0.115 (2.93)	0.200 (5.08)	0.115 (2.93)	0.200 (5.08)
α		15°		15°		15°		15°

Shaded areas for 300 Mil Body Width 24 PDIP only

Package Outlines



Notes:
1) Not to scale
2) Dimensions in inches
3) (Dimensions in millimeters)
4) For D & E add for allowable Mold Protrusion 0.010"

Dim	20-Pin		28-Pin		44-Pin		68-Pin		84-Pin	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	0.165 (4.20)	0.180 (4.57)	0.165 (4.20)	0.180 (4.57)	0.165 (4.20)	0.180 (4.57)	0.165 (4.20)	0.200 (5.08)	0.165 (4.20)	0.200 (5.08)
A_1	0.090 (2.29)	0.120 (3.04)	0.090 (2.29)	0.120 (3.04)	0.090 (2.29)	0.120 (3.04)	0.090 (2.29)	0.130 (3.30)	0.090 (2.29)	0.130 (3.30)
D/E	0.385 (9.78)	0.395 (10.03)	0.485 (12.32)	0.495 (12.57)	0.685 (17.40)	0.695 (17.65)	0.985 (25.02)	0.995 (25.27)	1.185 (30.10)	1.195 (30.35)
D_1/E_1	0.350 (8.890)	0.356 (9.042)	0.450 (11.430)	0.456 (11.582)	0.650 (16.510)	0.656 (16.662)	0.950 (24.130)	0.958 (24.333)	1.150 (29.210)	1.158 (29.413)
D_2/E_2	0.290 (7.37)	0.330 (8.38)	0.390 (9.91)	0.430 (10.92)	0.590 (14.99)	0.630 (16.00)	0.890 (22.61)	0.930 (23.62)	1.090 (27.69)	1.130 (28.70)
e	0	0.004	0	0.004	0	0.004	0	0.004	0	0.004
F	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)
G	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)
H	0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)	
I	0.020 (0.51)		0.020 (0.51)		0.020 (0.51)		0.020 (0.51)		0.020 (0.51)	

Plastic J-Lead Chip Carrier - P-Suffix

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