# 128Mb BURST CellularRAM™ 1.5

## MT45W8MW16BGX

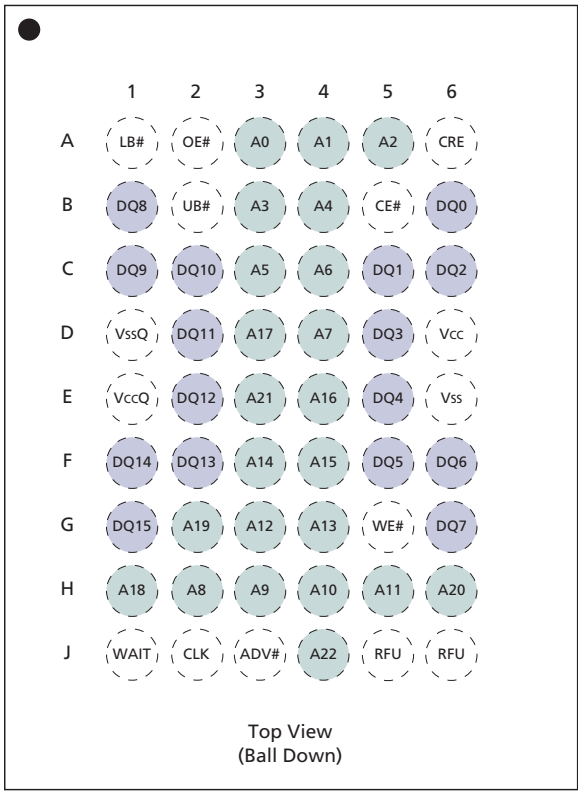
### Features

- Single device supports asynchronous, page, and burst operations
- Vcc, VccQ Voltages
  1.7V–1.95V Vcc
  1.7V–1.95V VccQ
- Random Access Time: 70ns
- Burst Mode READ and WRITE Access
  4, 8, 16, or 32 words, or continuous burst
  Burst wrap or sequential
  MAX clock rate: 104 MHz ($^{t}$CLK = 9.62ns)
  Burst initial latency: 39ns (4 clocks) @ 104 MHz
  $^{t}$ACLK: 7ns @ 104 MHz
- Page Mode Read Access
  Sixteen-word page size
  Interpage read access: 70ns
  Intrapage read access: 20ns
- Low Power Consumption
  Asynchronous READ: < 30mA
  Intrapage Read: < 15mA
  Initial access, burst READ:
  (39ns [4 clocks] @ 104 MHz) < 40mA
  Continuous burst READ: < 25mA
  Standby: < 40µA (TYP at 25°C)
  Deep power-down: < 3µA (TYP)
- Low-Power Features
  On-chip Temperature Compensated Refresh (TCR)
  Partial Array Refresh (PAR)
  Deep Power-Down (DPD) Mode

### Options

| Options | Designator |
|---|---|
| • Configuration: | MT45**W8MW16**B |
| 8 Meg x 16 | |
| VCC Core Voltage Supply: 1.8V | |
| VCCQ I/O Voltage Supply: 1.8V | |
| • Package | |
| 54-ball VFBGA—"green" | GX |
| • Timing | |
| 70ns access | -70 |
| 85ns access | -85 |

### Figure 1: Ball Assignment 54-Ball VFBGA




| Options (continued) | Designator |
|---|---|
| • Frequency | |
| 66 MHz | 6 |
| 80 MHz | 8 |
| 104 MHz | 1 |
| • Standby Power at 85°C | |
| Standard: 200µA (MAX) | None |
| Low-power: 160µA (MAX) | L |
| • Operating Temperature Range | |
| Wireless (-30°C to +85°C) | WT |
| Industrial (-40°C to +85°C) | IT |

*Part Number Example:*
**MT45W8MW16BGX-701LWT**

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## General Description

Micron® CellularRAM™ products are high-speed, CMOS pseudo-static random access memories developed for low-power, portable applications. The MT45W8MW16BGX device has a 128Mb DRAM core, organized as 8 Meg x 16 bits. These devices include an industry-standard burst mode Flash interface that dramatically increases read/write bandwidth compared with other low-power SRAM or Pseudo SRAM offerings.

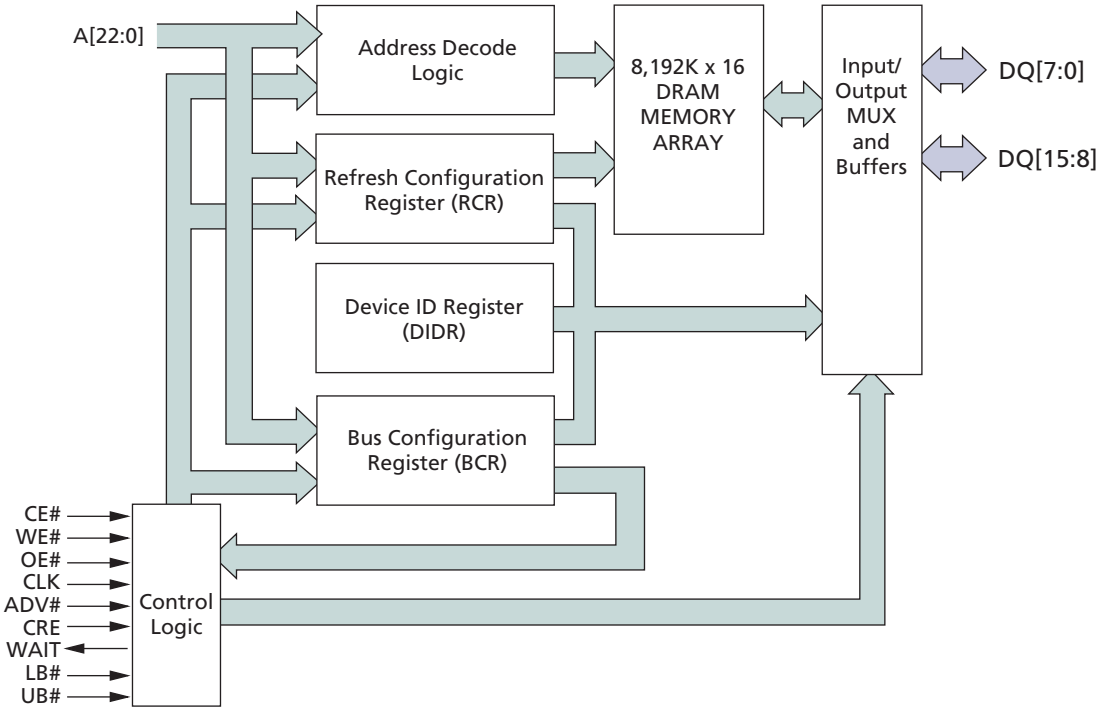
To operate seamlessly on a burst Flash bus, CellularRAM products incorporate a transparent self refresh mechanism. The hidden refresh requires no additional support from the system memory controller and has no significant impact on device read/write performance.

Two user-accessible control registers define device operation. The bus configuration register (BCR) defines how the CellularRAM device interacts with the system memory bus and is nearly identical to its counterpart on burst mode Flash devices. The refresh configuration register (RCR) is used to control how refresh is performed on the DRAM array. These registers are automatically loaded with default settings during power-up and can be updated anytime during normal operation.

Special attention has been focused on standby current consumption during self refresh. CellularRAM products include three mechanisms to minimize standby current. Partial array refresh (PAR) enables the system to limit refresh to only that part of the DRAM array that contains essential data. Temperature compensated refresh (TCR) uses an on-chip sensor to adjust the refresh rate to match the device temperature—the refresh rate decreases at lower temperatures to minimize current consumption during standby. Deep power-down (DPD) enables the system to halt the refresh operation altogether when no vital information is stored in the device. The system configurable refresh mechanisms are accessed through the RCR.

This CellularRAM device is compliant with the industry-standard CellularRAM 1.5 feature set established by the CellularRAM Workgroup. It includes support for both variable and fixed latency, with three output-device drive-strength settings, additional wrap options, and a device ID register (DIDR).

**Figure 2: Functional Block Diagram—8 Meg x 16**




NOTE:

Functional block diagrams illustrate simplified device operation. See ball descriptions (Table 1); bus operations tables (Tables 2 and 3); and timing diagrams for detailed information.

## Table 1: VFBGA Ball Descriptions

| VFBGA ASSIGNMENT | SYMBOL | TYPE | DESCRIPTION |
|---|---|---|---|
| A3, A4, A5, B3, B4, C3, C4, D4, H2, H3, H4, H5, G3, G4, F3, F4, E4, D3, H1, G2, H6, E3, J4 | A[22:0] | Input | Address Inputs: Inputs for addresses during READ and WRITE operations. Addresses are internally latched during READ and WRITE cycles. The address lines are also used to define the value to be loaded into the BCR or the RCR. |
| J2 | CLK | Input | Clock: Synchronizes the memory to the system operating frequency during synchronous operations. When configured for synchronous operation, the address is latched on the first rising CLK edge when ADV# is active. CLK is static LOW during asynchronous access READ and WRITE operations and during PAGE READ ACCESS operations. |
| J3 | ADV# | Input | Address Valid: Indicates that a valid address is present on the address inputs. Addresses can be latched on the rising edge of ADV# during asynchronous READ and WRITE operations. ADV# can be held LOW during asynchronous READ and WRITE operations. |
| A6 | CRE | Input | Control Register Enable: When CRE is HIGH, WRITE operations load the RCR or BCR, and READ operations access the RCR, BCR, or DIDR. |
| B5 | CE# | Input | Chip Enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby or deep power-down mode. |
| A2 | OE# | Input | Output Enable: Enables the output buffers when LOW. When OE# is HIGH, the output buffers are disabled. |
| G5 | WE# | Input | Write Enable: Determines if a given cycle is a WRITE cycle. If WE# is LOW, the cycle is a WRITE to either a configuration register or to the memory array. |
| A1 | LB# | Input | Lower Byte Enable. DQ[7:0] |
| B2 | UB# | Input | Upper Byte Enable. DQ[15:8] |
| B6, C5, C6, D5, E5, F5, F6, G6, B1, C1, C2, D2, E2, F2, F1, G1 | DQ[15:0] | Input/ Output | Data Inputs/Outputs. |
| J1 | WAIT | Output | Wait: Provides data-valid feedback during burst READ and WRITE operations. The signal is gated by CE#. WAIT is used to arbitrate collisions between refresh and READ/WRITE operations. WAIT is asserted when a burst crosses a row boundary. WAIT is also used to mask the delay associated with opening a new internal page. WAIT is asserted and should be ignored during asynchronous and page mode operations. WAIT is High-Z when CE# is HIGH. |
| J5, J6 | RFU | — | Reserved for future use. |
| D6 | VCC | Supply | Device Power Supply: (1.70V–1.95V) Power supply for device core operation. |
| E1 | VCCQ | Supply | I/O Power Supply: (1.70V–1.95V) Power supply for input/output buffers. |
| E6 | VSS | Supply | VSS must be connected to ground. |
| D1 | VSSQ | Supply | VSSQ must be connected to ground. |

NOTE:

The CLK and ADV# inputs can be tied to VSS if the device is always operating in asynchronous or page mode. WAIT will be asserted but should be ignored during asynchronous and page mode operations.

## Table 2: Bus Operations—Asynchronous Mode

| MODE | POWER | CLK[1] | ADV# | CE# | OE# | WE# | CRE | LB#/ UB# | WAIT[2] | DQ[15:0][3] | NOTES |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Read | Active | L | L | L | L | H | L | L | Low-Z | Data-Out | 4 |
| Write | Active | L | L | L | X | L | L | L | Low-Z | Data-In | 4 |
| Standby | Standby | L | X | H | X | X | L | X | High-Z | High-Z | 5, 6 |
| No Operation | Idle | L | X | L | X | X | L | X | Low-Z | X | 4, 6 |
| Configuration Register Write | Active | L | L | L | H | L | H | X | Low-Z | High-Z | |
| Configuration Register Read | Active | L | L | L | L | H | H | L | Low-Z | Config. Reg. Out | |
| DPD | Deep Power-Down | L | X | H | X | X | X | X | High-Z | High-Z | 7 |

## Table 3: Bus Operations—Burst Mode

| MODE | POWER | CLK[1] | ADV# | CE# | OE# | WE# | CRE | LB#/ UB# | WAIT[2] | DQ[15:0][3] | NOTES |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Async Read | Active | L | L | L | L | H | L | L | Low-Z | Data-Out | 4 |
| Async Write | Active | L | L | L | X | L | L | L | Low-Z | Data-In | 4 |
| Standby | Standby | L | X | H | X | X | L | X | High-Z | High-Z | 5, 6 |
| No Operation | Idle | L | X | L | X | X | L | X | Low-Z | X | 4, 6 |
| Initial Burst Read | Active |  | L | L | X | H | L | L | Low-Z | Data-Out | 4, 8 |
| Initial Burst Write | Active |  | L | L | H | L | L | X | Low-Z | Data-In | 4, 8 |
| Burst Continue | Active |  | H | L | X | X | X | L | Low-Z | Data-In or Data-Out | 4, 8 |
| Burst Suspend | Active | X | X | L | H | X | X | X | Low-Z | High-Z | 4, 8 |
| Configuration Register Write | Active |  | L | L | H | L | H | X | Low-Z | High-Z | 8, 9 |
| Configuration Register Read | Active |  | L | L | L | H | H | L | Low-Z | Config. Reg. Out | 8, 9 |
| DPD | Deep Power-Down | L | X | H | X | X | X | X | High-Z | High-Z | 7 |

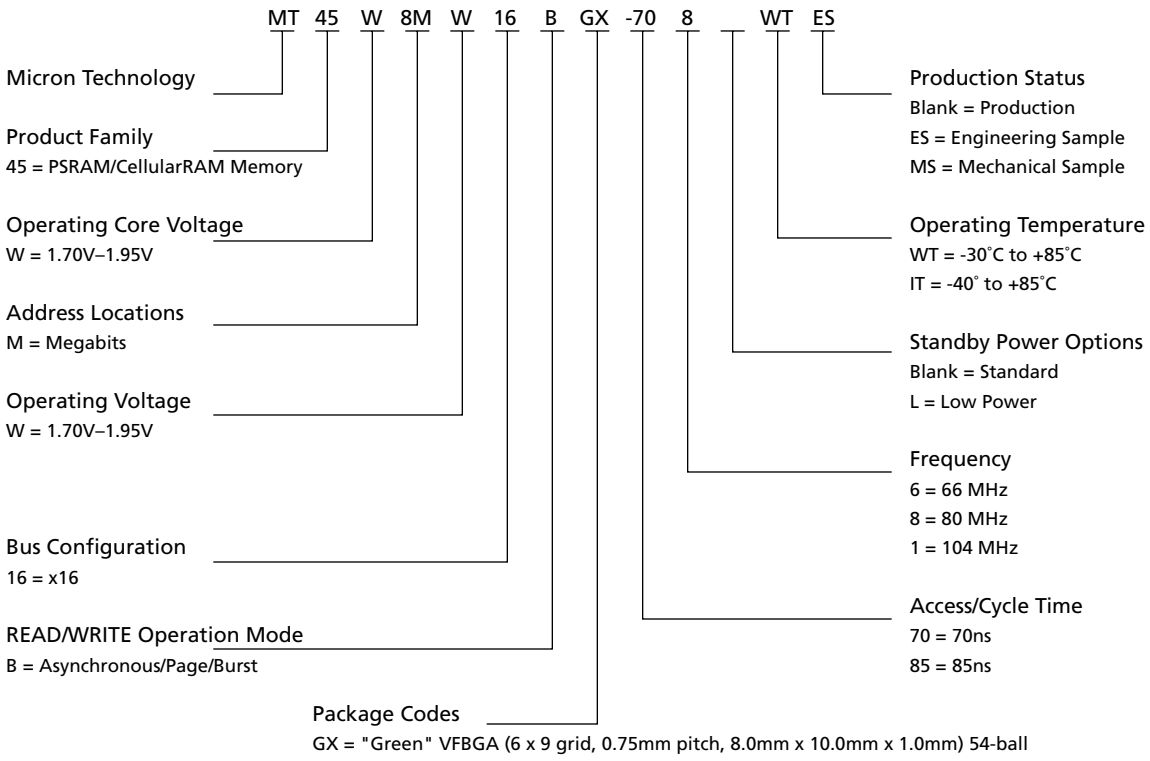
NOTE:

1. CLK must be LOW during async read and async write modes; and to achieve standby power during standby and DPD modes. CLK must be static (HIGH or LOW) during burst suspend.
2. The WAIT polarity is configured through the bus configuration register (BCR[10]).
3. When LB# and UB# are in select mode (LOW), DQ[15:0] are affected. When only LB# is in select mode, DQ[7:0] are affected. When only UB# is in the select mode, DQ[15:8] are affected.
4. The device will consume active power in this mode whenever addresses are changed.
5. When the device is in standby mode, address inputs and data inputs/outputs are internally isolated from any external influence.
6. $V_{IN}$ = $V_{CC}Q$ or 0V; all device balls must be static (unswitched) in order to achieve standby current.
7. DPD is initiated when CE# transitions from LOW to HIGH after writing RCR[4] to 0. DPD is maintained until CE# transitions from HIGH to LOW.
8. Burst mode operation is initialized through the bus configuration register (BCR[15]).
9. Initial cycle. Following cycles are the same as BURST CONTINUE. CE# must stay LOW for the equivalent of a single-word burst (as indicated by WAIT).

## Part-Numbering Information

Micron CellularRAM devices are available in several different configurations and densities (see Figure 3).

**Figure 3: Part Number Chart**




### *Valid Part Number Combinations*

After building the part number from the part numbering chart above, please go to the Micron Part Marking Decoder Web site at http://www.micron.com/partsearch to verify that the part number is offered and valid. If the device required is not on this list, please contact the factory.

### *Device Marking*

Due to the size of the package, the Micron standard part number is not printed on the top of the device. Instead, an abbreviated device mark comprised of a five-digit alphanumeric code is used. The abbreviated device marks are cross-referenced to the Micron part numbers at http://www.micron.com/partsearch. To view the location of the abbreviated mark on the device, please refer to customer service note, CSN-11, "Product Mark/Label," at http://www.micron.com/csn.

## Functional Description

In general, the MT45W8MW16BGX device is a high-density alternative to SRAM and Pseudo SRAM products, popular in low-power, portable applications.

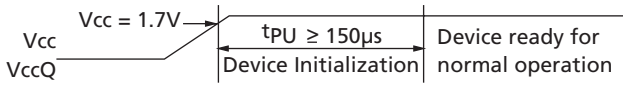
MT45W8MW16BGX contains a 134,217,728-bit DRAM core, organized as 8,388,608 addresses by 16 bits. The device implements the same high-speed bus interface found on burst mode Flash products.

The CellularRAM bus interface supports both asynchronous and burst mode transfers. Page mode accesses are also included as a bandwidth-enhancing extension to the asynchronous read protocol.

### *Power-Up Initialization*

CellularRAM products include an on-chip voltage sensor used to launch the power-up initialization process. Initialization will configure the BCR and the RCR with their default settings (see Table 18 on page 20 and Table 24 on page 26). VCC and VCCQ must be applied simultaneously. When they reach a stable level at or above 1.7V, the device will require 150µs to complete its self-initialization process. During the initialization period, CE# should remain HIGH. When initialization is complete, the device is ready for normal operation.

**Figure 4: Power-Up Initialization Timing**




## Bus Operating Modes

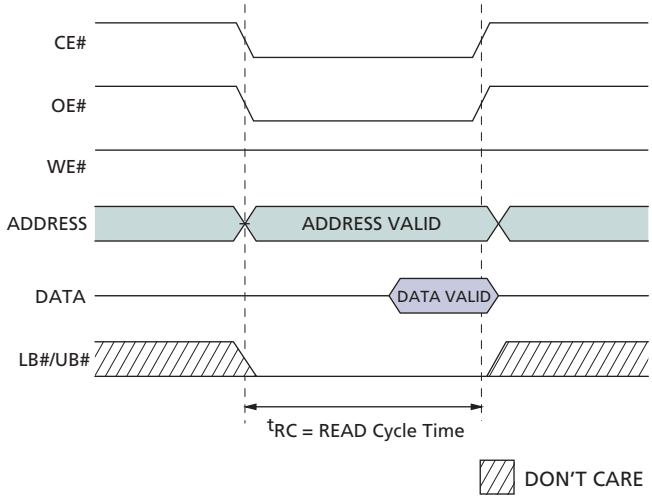
The MT45W8MW16BGX CellularRAM product incorporates a burst mode interface found on Flash products targeting low-power, wireless applications. This bus interface supports asynchronous, page mode, and burst mode read and write transfers. The specific interface supported is defined by the value loaded into the BCR. Page mode is controlled by the refresh configuration register (RCR[7]).

### *Asynchronous Mode*

CellularRAM products power up in the asynchronous operating mode. This mode uses the industry-standard SRAM control bus (CE#, OE#, WE#, LB#/UB#). READ operations (Figure 5) are initiated by bringing CE#, OE#, and LB#/UB# LOW while keeping WE# HIGH. Valid data will be driven out of the I/Os after the specified access time has elapsed. WRITE operations (Figure 6) occur when CE#, WE#, and LB#/UB# are driven LOW. During asynchronous WRITE operations, the OE# level is a "Don't Care," and WE# will override OE#. The data to be written is latched on the rising edge of CE#, WE#, or LB#/UB# (whichever occurs first). Asynchronous operations (page mode disabled) can either use the ADV input to latch the address, or ADV can be driven LOW during the entire READ/WRITE operation.

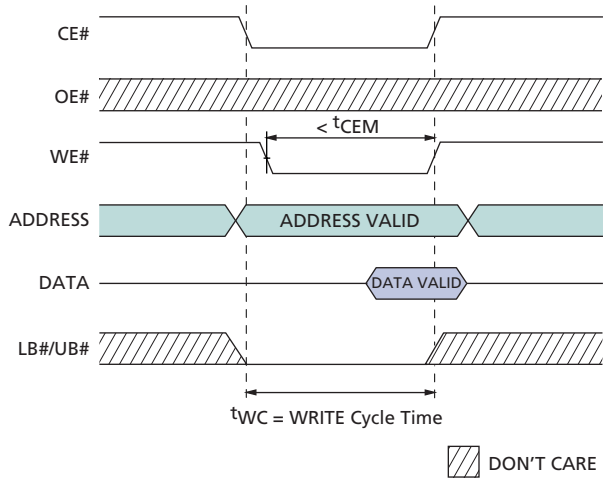
During asynchronous operation, the CLK input must be held static LOW. WAIT will be driven while the device is enabled and its state should be ignored. WE# LOW time must be limited to tCEM.

**Figure 5: READ Operation (ADV# LOW)**




NOTE:
ADV must remain LOW for page mode operation.

**Figure 6: WRITE Operation (ADV# LOW)**



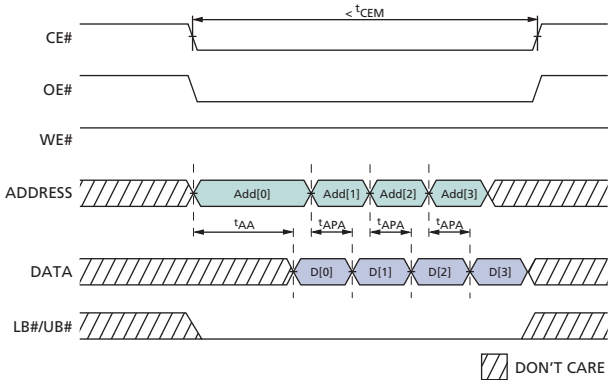
## Page Mode READ Operation

Page mode is a performance-enhancing extension to the legacy asynchronous READ operation. In page-mode-capable products, an initial asynchronous read access is performed, then adjacent addresses can be read quickly by simply changing the low-order address. Addresses A[3:0] are used to determine the members of the 16-address CellularRAM page. Any change in addresses A[4] or higher will initiate a new $^{t}$AA access time. Figure 7 shows the timing for a page mode access. Page mode takes advantage of the fact that adjacent addresses can be read in a shorter period of time than random addresses. WRITE operations do not include comparable page mode functionality.

During asynchronous page mode operation, the CLK input must be held LOW. CE# must be driven HIGH upon completion of a page mode access. WAIT will be driven while the device is enabled and its state should be ignored. Page mode is enabled by setting RCR[7] to HIGH. ADV must be driven LOW during all page mode read accesses.

Due to refresh considerations, CE# must not be LOW longer than $^{t}$CEM.

**Figure 7: Page Mode READ Operation (ADV# LOW)**




## Burst Mode Operation

Burst mode operations enable high-speed synchronous READ and WRITE operations. Burst operations consist of a multi-clock sequence that must be performed in an ordered fashion. After CE# goes LOW, the address to access is latched on the rising edge of the next clock that ADV# is LOW. During this first clock rising edge, WE# indicates whether the operation is going to be a READ (WE# = HIGH, Figure 8 on page 12) or WRITE (WE# = LOW, Figure 9 on page 12).

The size of a burst can be specified in the BCR either as a fixed length or continuous. Fixed-length bursts consist of four, eight, sixteen, or thirty-two words. Continuous bursts have the ability to start at a specified address and burst through the entire memory.

The latency count stored in the BCR defines the number of clock cycles that elapse before the initial data value is transferred between the processor and CellularRAM device. The initial latency for READ operations can be configured as fixed or variable (WRITE operations always use fixed latency). Variable latency allows the CellularRAM to be configured for minimum latency at high clock frequencies, but the controller must monitor WAIT to detect any conflict with refresh cycles.

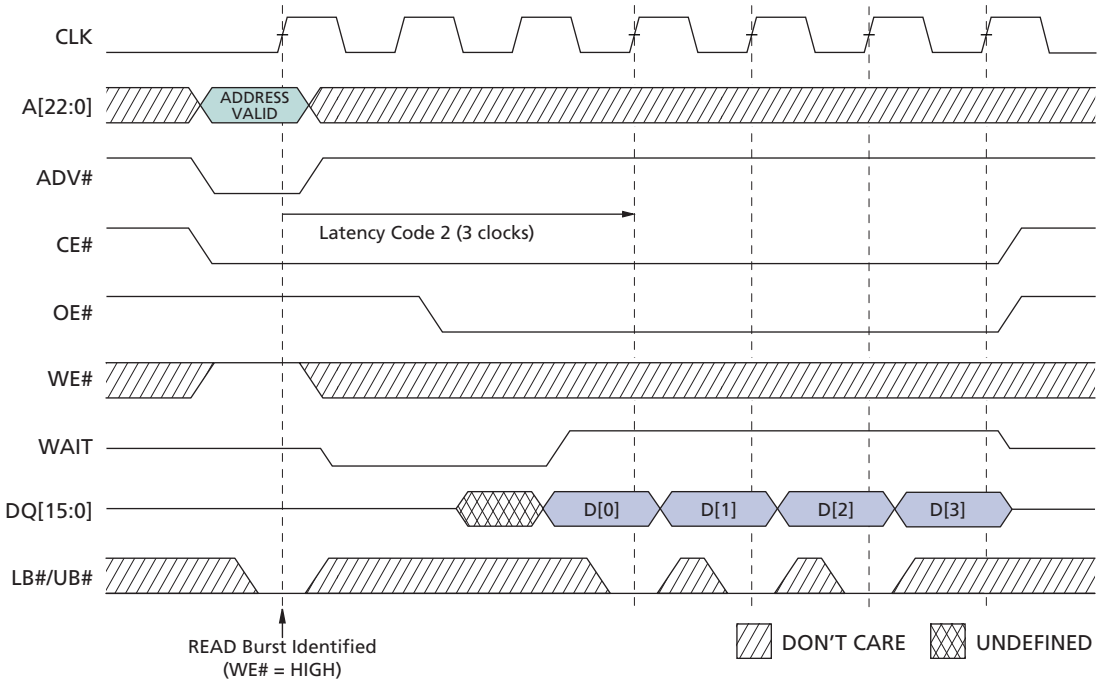
Fixed latency outputs the first data word after the worst-case access delay, including allowance for refresh collisions. The initial latency time and clock speed determine the latency count setting. The boundaries of 128-word rows should not be crossed in fixed latency mode. Fixed latency is used when the controller cannot monitor WAIT. Fixed latency also provides improved performance at lower clock frequencies.

The WAIT output asserts as soon as CE# goes LOW, and de-asserts to indicate when data is to be transferred into (or out of) the memory. WAIT will again be asserted if the burst crosses a row boundary (variable latency only—do not cross row boundaries when using fixed latency). Once the CellularRAM device has restored the previous row's data and accessed the next row, WAIT will be de-asserted and the burst can continue (see Figure 38 on page 45).

To access other devices on the same bus without the timing penalty of the initial latency for a new burst, burst mode can be suspended. Bursts are suspended by stopping CLK. CLK can be stopped HIGH or LOW. If another device will use the data bus while the burst is suspended, OE# should be taken HIGH to disable the CellularRAM outputs; otherwise, OE# can remain LOW. Note that the WAIT output will continue to be active, and as a result no other devices should directly share the WAIT connection to the controller. To continue the burst sequence, OE# is taken LOW, then CLK is restarted after valid data is available on the bus.

The CE# LOW time is limited by refresh considerations. CE# must not stay LOW longer than $^{t}$CEM. If a burst suspension will cause CE# to remain LOW for longer than $^{t}$CEM, CE# should be taken HIGH and the burst restarted with a new CE# LOW/ADV# LOW cycle.

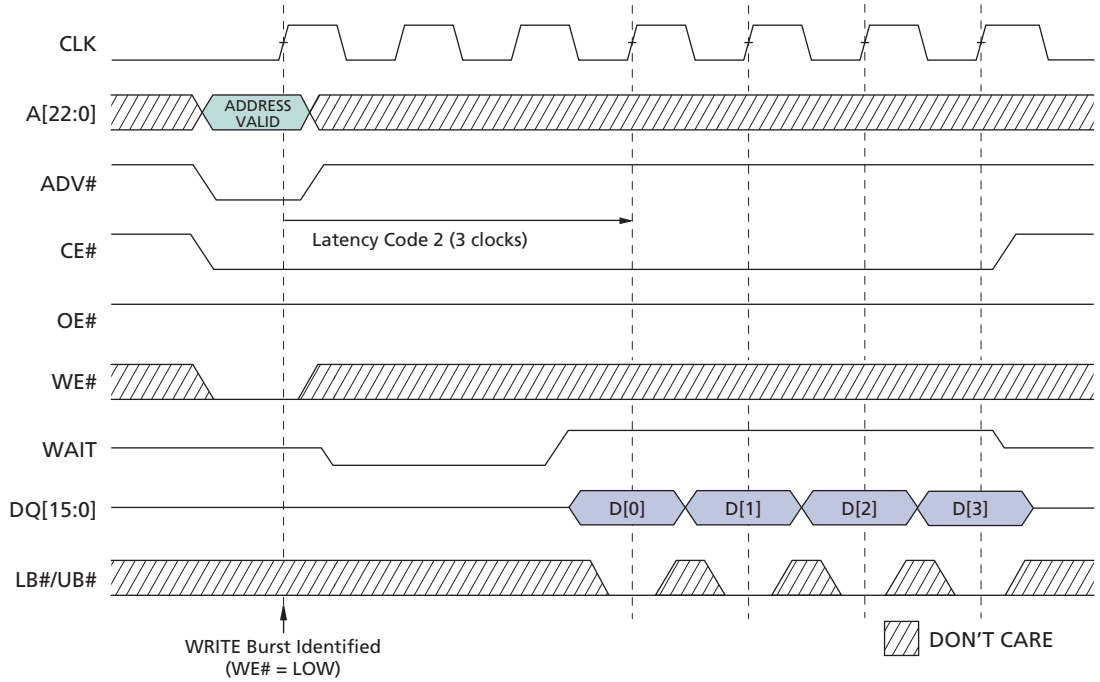
## Figure 8: Burst Mode READ (4-word burst)




NOTE:

Non-default BCR settings for burst mode READ (4-word burst): Fixed or variable latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay. Diagram above is representative of variable latency with no refresh collision or fixed-latency access.

## Figure 9: Burst Mode WRITE (4-word burst)




NOTE:

Non-default BCR settings for burst mode WRITE (4-word burst): Fixed or variable latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.

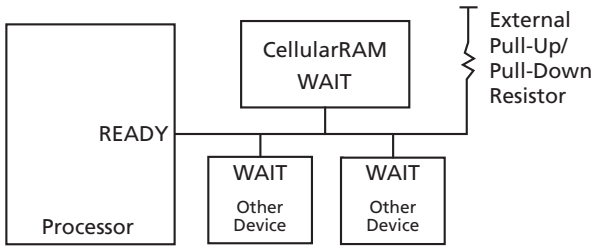
## Mixed-Mode Operation

The device supports a combination of synchronous READ and asynchronous READ and WRITE operations when the BCR is configured for synchronous operation. The asynchronous READ and WRITE operations require that the clock (CLK) remain LOW during the entire sequence. The ADV# signal can be used to latch the target address, or it can remain LOW during the entire WRITE operation. CE# can remain LOW when transitioning between mixed-mode operations with fixed latency enabled; however, the CE# LOW time must not exceed $^{t}$CEM. Mixed-mode operation facilitates a seamless interface to legacy burst mode Flash memory controllers. See Figure 50 on page 57 for the "Asynchronous WRITE Followed by Burst READ" timing diagram.

## WAIT Operation

The WAIT output on a CellularRAM device is typically connected to a shared, system-level WAIT signal (see Figure 10). The shared WAIT signal is used by the processor to coordinate transactions with multiple memories on the synchronous bus.

**Figure 10: Wired or WAIT Configuration**




Once a READ or WRITE operation has been initiated, WAIT goes active to indicate that the CellularRAM device requires additional time before data can be transferred. For READ operations, WAIT will remain active until valid data is output from the device. For WRITE operations, WAIT will indicate to the memory controller when data will be accepted into the CellularRAM device. When WAIT transitions to an inactive state, the data burst will progress on successive clock edges.

CE# must remain asserted during WAIT cycles (WAIT asserted and WAIT configuration BCR[8] = 1). Bringing CE# HIGH during WAIT cycles may cause data corruption. (Note that for BCR[8] = 0, the actual WAIT cycles end one cycle after WAIT de-asserts, and for row boundary crossings, start one cycle after the WAIT signal asserts.)

When using variable initial access latency (BCR[14] = 0), the WAIT output performs an arbitration role for READ operations launched while an on-chip refresh is in progress. If a collision occurs, WAIT is asserted for additional clock cycles until the refresh has completed (see Figures 11 on page 14). When the refresh operation has completed, the READ operation will continue normally.

WAIT is also asserted when a continuous READ or WRITE burst crosses the boundary between 128-word rows. The WAIT assertion allows time for the new row to be accessed, and permits any pending refresh operations to be performed.

WAIT will be asserted but should be ignored during asynchronous READ and WRITE, and page READ operations.

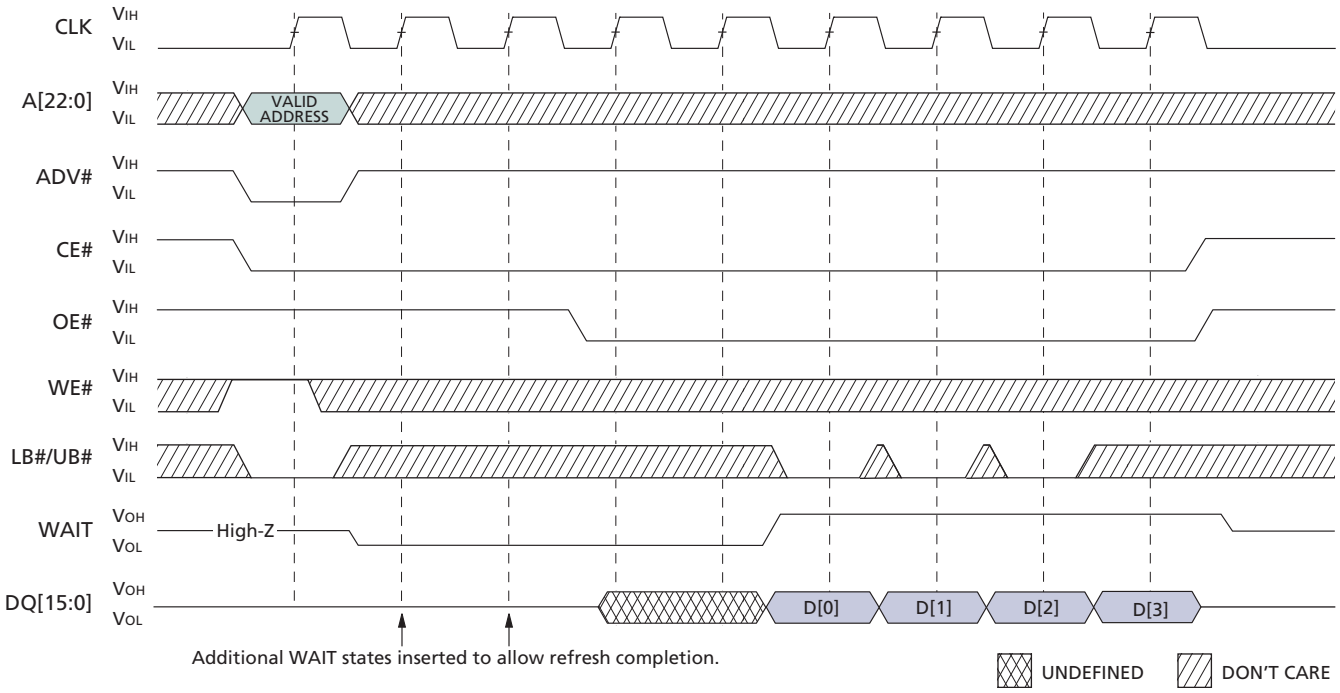
By using fixed initial latency (BCR[14] = 1), this CellularRAM device can be used in burst mode without monitoring the WAIT signal. However, WAIT can still be used to determine when valid data is available at the start of the burst and at row-boundary crossings. If WAIT is not monitored, the controller must stop burst accesses at row boundaries and restart the burst to access the next row.

## LB#/UB# Operation

The LB# enable and UB# enable signals support byte-wide data transfers. During READ operations, the enabled byte(s) are driven onto the DQs. The DQs associated with a disabled byte are put into a High-Z state during a READ operation. During WRITE operations, any disabled bytes will not be transferred to the RAM array and the internal value will remain unchanged. During an asynchronous WRITE cycle, the data to be written is latched on the rising edge of CE#, WE#, LB#, or UB#, whichever occurs first.

When both the LB# and UB# are disabled (HIGH) during an operation, the device will disable the data bus from receiving or transmitting data. Although the device will seem to be deselected, it remains in an active mode as long as CE# remains LOW.

## Figure 11: Refresh Collision During Variable-Latency READ Operation




NOTE:

Non-default BCR settings for refresh collision during variable-latency READ operation: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.

## Low-Power Operation

### Standby Mode Operation

During standby, the device current consumption is reduced to the level necessary to perform the DRAM refresh operation. Standby operation occurs when CE# is HIGH.

The device will enter a reduced power state upon completion of a READ or WRITE operation, or when the address and control inputs remain static for an extended period of time. This mode will continue until a change occurs to the address or control inputs.

### Temperature Compensated Refresh

Temperature compensated refresh (TCR) allows for adequate refresh at different temperatures. This CellularRAM device includes an on-chip temperature sensor that automatically adjusts the refresh rate according to the operating temperature. The device continually adjusts the refresh rate to match that temperature.

### Partial Array Refresh

Partial array refresh (PAR) restricts refresh operation to a portion of the total memory array. This feature enables the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, one-eighth array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map (see Table 8 on page 27). READ and WRITE operations to address ranges receiving refresh will not be affected. Data stored in addresses not receiving refresh will become corrupted. When re-enabling additional portions of the array, the new portions are available immediately upon writing to the RCR.

### Deep Power-Down Operation

Deep power-down (DPD) operation disables all refresh-related activity. This mode is used if the system does not require the storage provided by the CellularRAM device. Any stored data will become corrupted when DPD is enabled. When refresh activity has been re-enabled by rewriting the RCR, the CellularRAM device will require 150µs to perform an initialization procedure before normal operations can resume. During this 150µs period, the current consumption will be higher than the specified standby levels, but considerably lower than the active current specification.

DPD can be enabled by writing to the RCR using CRE or the software access sequence; DPD starts when CE# goes HIGH. DPD is disabled the next time CE# goes LOW.

## Registers

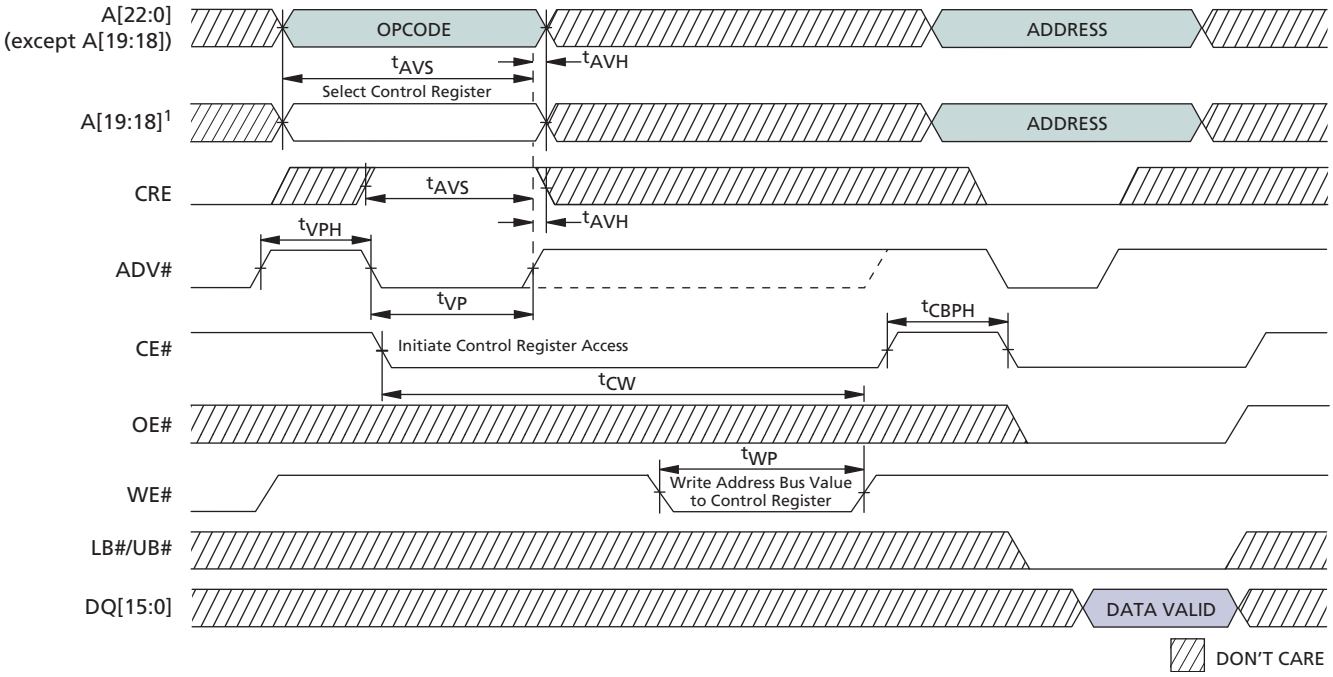
Two user-accessible configuration registers define the device operation. The bus configuration register (BCR) defines how the CellularRAM interacts with the system memory bus and is nearly identical to its counterpart on burst mode Flash devices. The refresh configuration register (RCR) is used to control how refresh is performed on the DRAM array. These registers are automatically loaded with default settings during power-up, and can be updated any time the devices are operating in a standby state.

A DIDR provides information on the device manufacturer, CellularRAM generation, and the specific device configuration. The DIDR is read-only.

### Access Using CRE

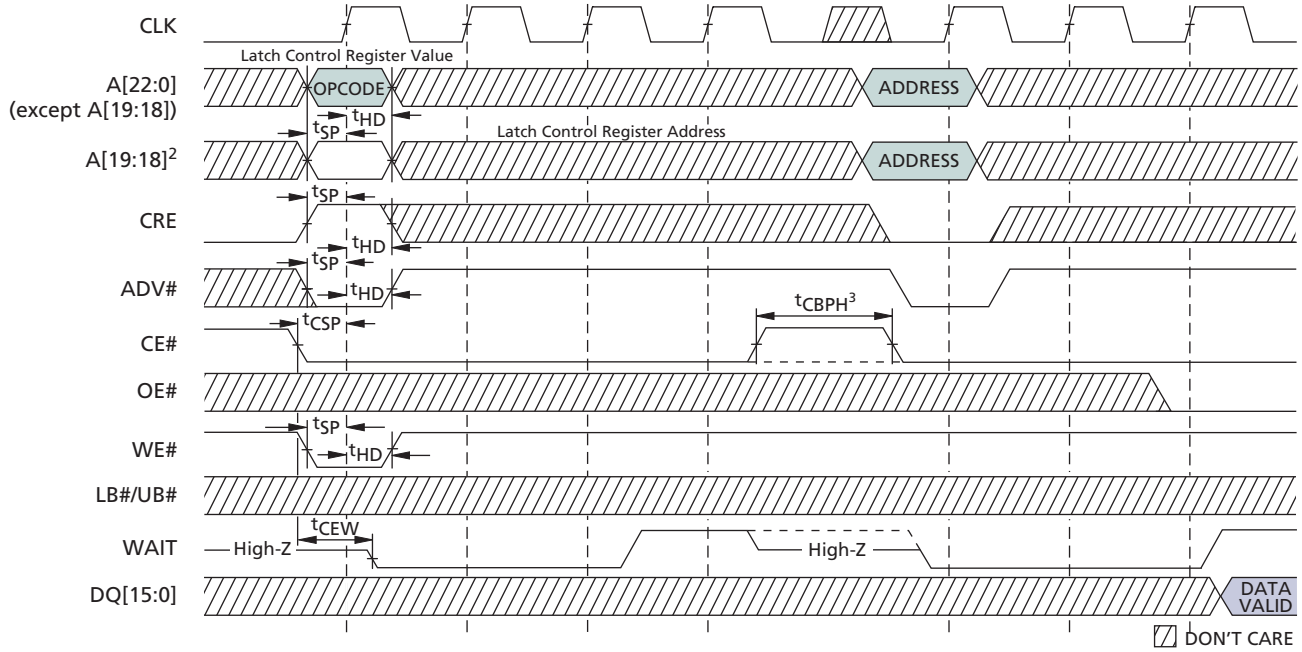
The registers can be accessed using either a synchronous or an asynchronous operation when the control register enable (CRE) input is HIGH (see Figures 12 through 15 on pages 16 through 18). When CRE is LOW, a READ or WRITE operation will access the memory array. The configuration register values are written via addresses A[22:0]. In an asynchronous WRITE, the values are latched into the configuration register on the rising edge of ADV#, CE#, or WE#, whichever occurs first; LB# and UB# are “Don’t Care.” The BCR is accessed when A[19:18] are 10b; the RCR is accessed when A[19:18] are 00b. The DIDR is read when A[19:18] are 01b. For reads, address inputs other than A[19:18] are “Don’t Care,” and register bits 15:0 are output on DQ[15:0].

## Figure 12: Configuration Register WRITE, Asynchronous Mode Followed by READ ARRAY Operation



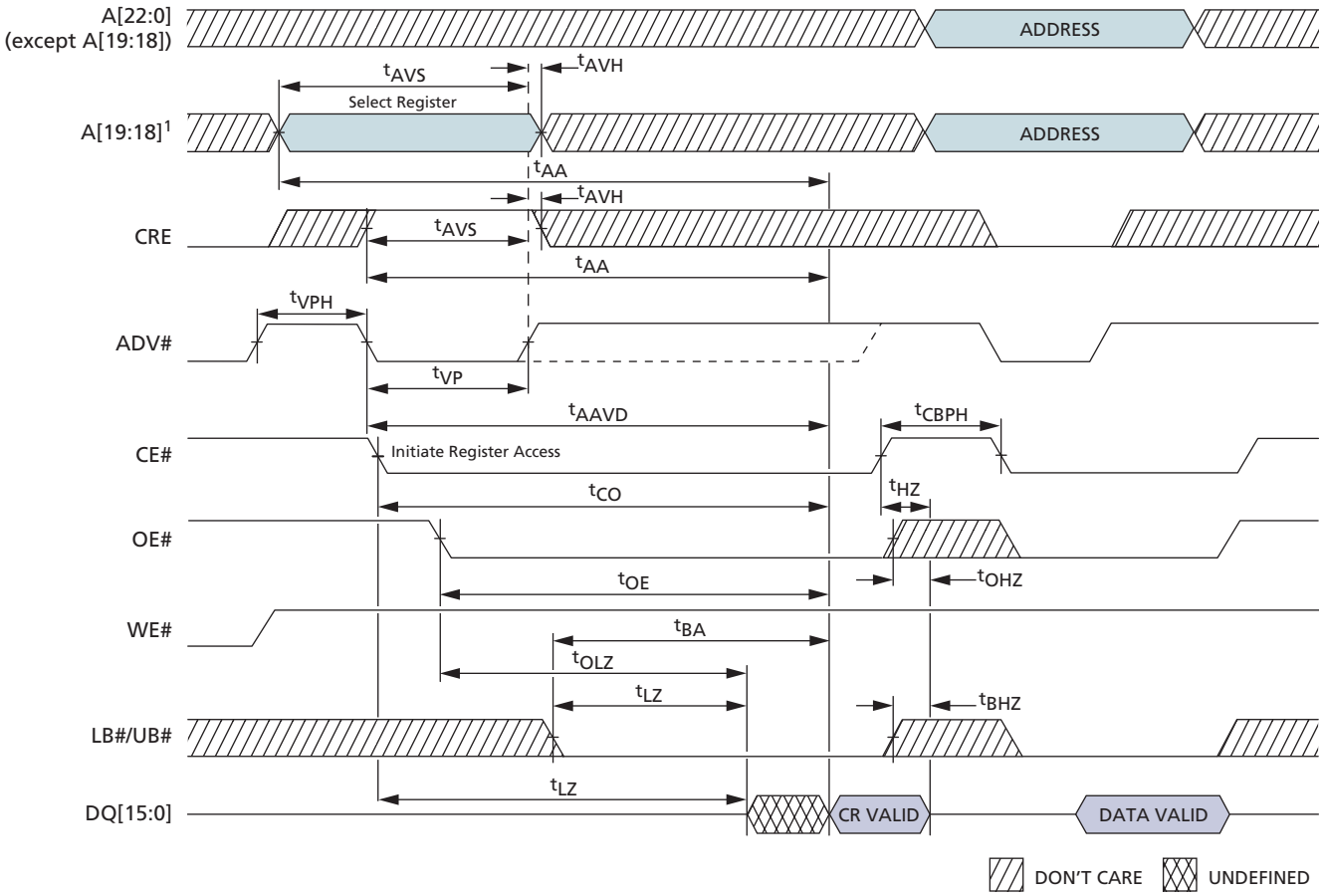

NOTE: 1. A[19:18] = 00b to load RCR, and 10b to load BCR.

## Figure 13: Configuration Register WRITE, Synchronous Mode Followed by READ ARRAY Operation




NOTE:
1. Non-default BCR settings for synchronous mode configuration register WRITE followed by READ ARRAY operation: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. A[19:18] = 00b to load RCR, and 10b to load BCR.
3. CE# must remain LOW to complete a burst-of-one WRITE. WAIT must be monitored—additional WAIT cycles caused by refresh collisions require a corresponding number of additional CE# LOW cycles.

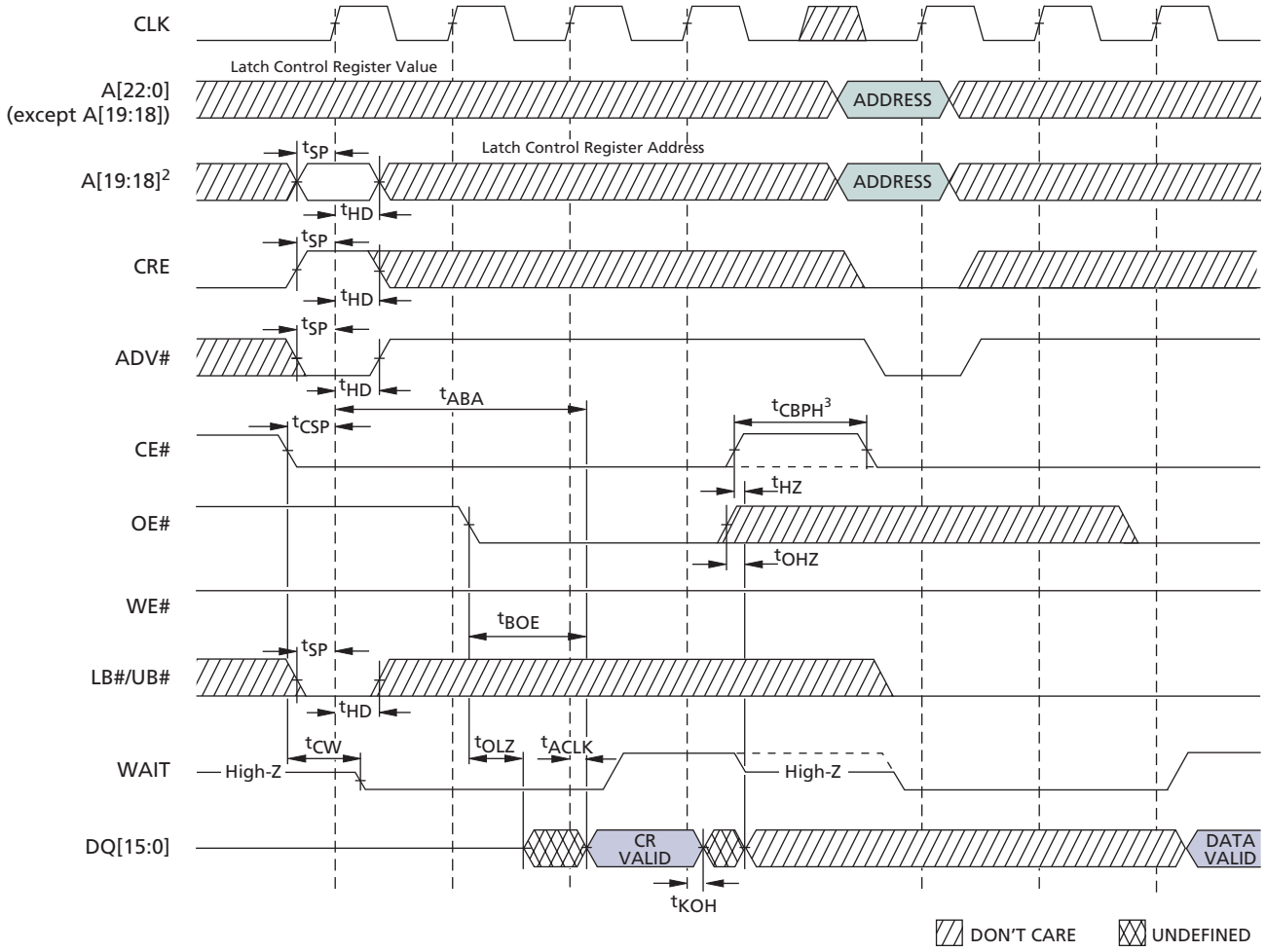
## Figure 14: Register READ, Asynchronous Mode Followed by READ ARRAY Operation




NOTE:

A[19:18] = 00b to read RCR, 10b to read BCR, and 01b to read DIDR.

## Figure 15: Register READ, Synchronous Mode Followed by READ ARRAY Operation




NOTE:

1. Non-default BCR settings for synchronous mode register READ followed by READ ARRAY operation: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. A[19:18] = 00b to read RCR, 10b to read BCR, and 01b to read DIDR.
3. CE# must remain LOW to complete a burst-of-one WRITE. WAIT must be monitored—additional WAIT cycles caused by refresh collisions require a corresponding number of additional CE# LOW cycles.

### Software Access

Software access of the registers uses a sequence of asynchronous READ and asynchronous WRITE operations. The contents of the configuration registers can be modified and all registers can be read using the software sequence.

The configuration registers are loaded using a four-step sequence consisting of two asynchronous READ operations followed by two asynchronous WRITE operations (see Figure 16). The read sequence is virtually identical except that an asynchronous READ is performed during the fourth operation (see Figure 17). The address used during all READ and WRITE operations is the highest address of the CellularRAM device being accessed (7FFFFFh for 128Mb); the contents of this address are not changed by using this sequence.

The data value presented during the third operation (WRITE) in the sequence defines whether the BCR, RCR, or the DIDR is to be accessed. If the data is 0000h, the sequence will access the RCR; if the data is 0001h, the sequence will access the BCR; if the data is 0002h, the sequence will access the DIDR. During the fourth operation, DQ[15:0] transfer data in to or out of bits 15–0 of the registers.

The use of the software sequence does not affect the ability to perform the standard (CRE-controlled) method of loading the configuration registers. However, the software nature of this access mechanism eliminates the need for CRE. If the software mechanism is used, CRE can simply be tied to Vss. The port line often used for CRE control purposes is no longer required.

**Figure 16: Load Configuration Register**

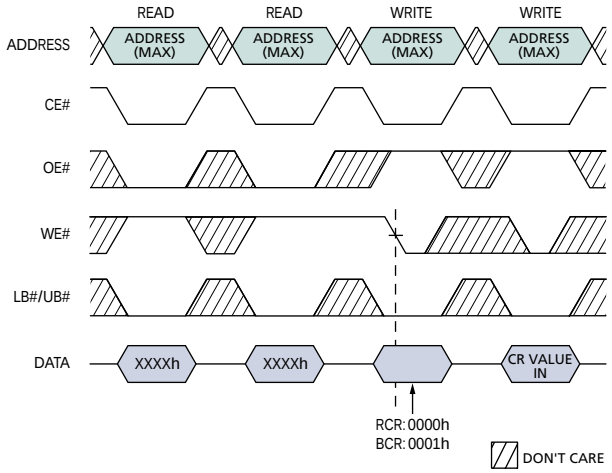
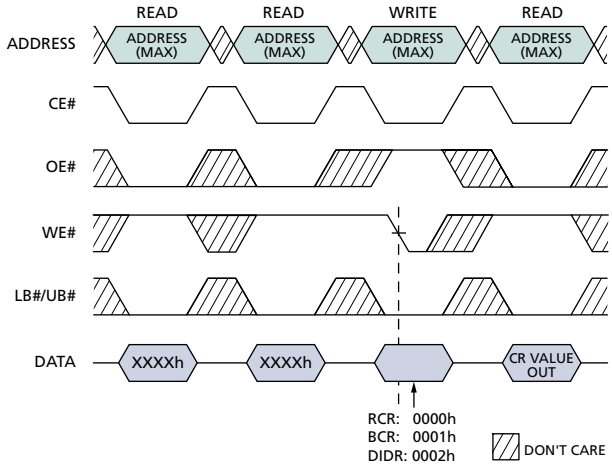



**Figure 17: Read Configuration Register**

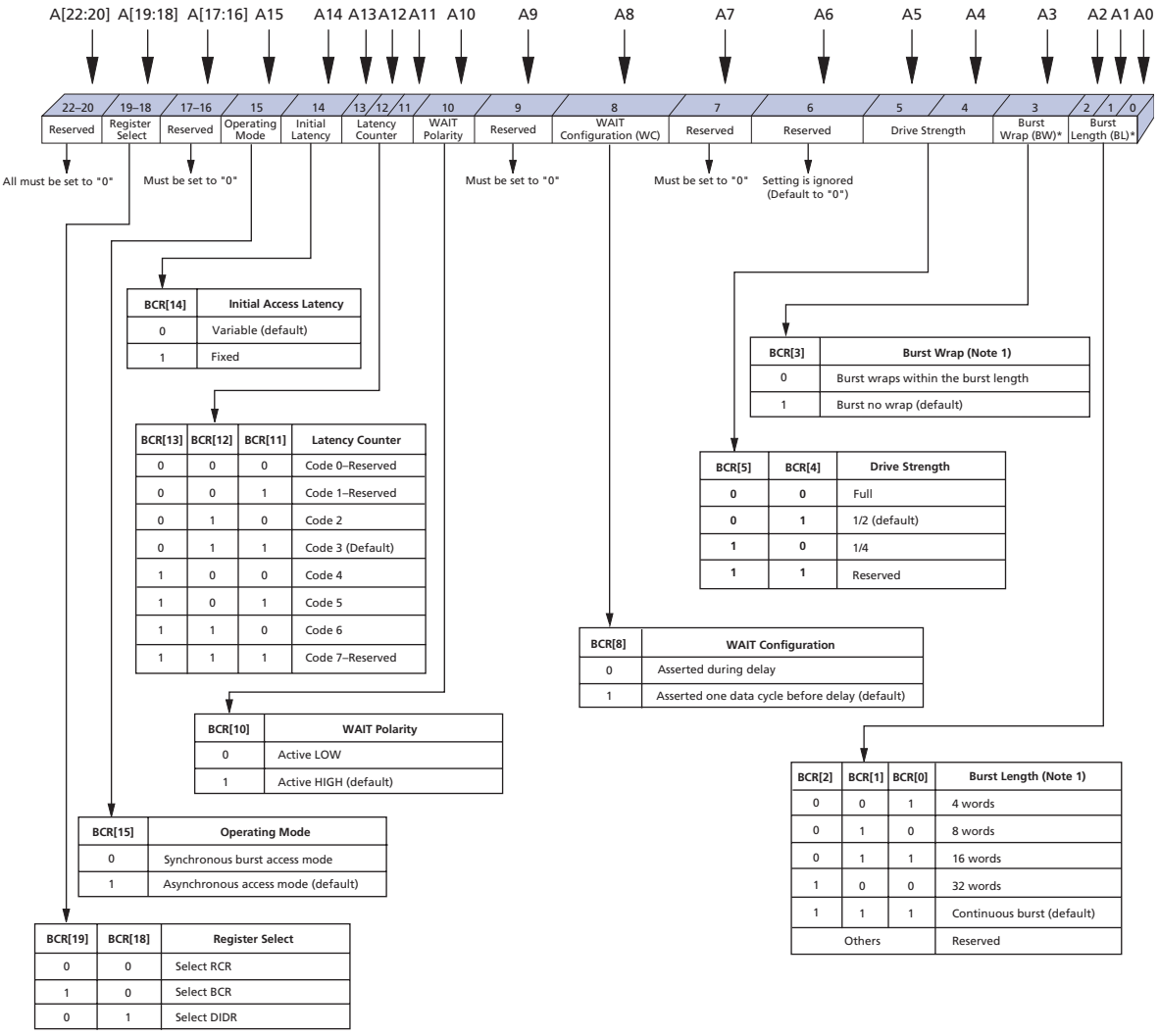


## Bus Configuration Register

The BCR defines how the CellularRAM device interacts with the system memory bus. Page mode operation is enabled by a bit contained in the RCR. Figure 18 describes the control bits in the BCR. At power-up, the BCR is set to 9D1Fh.

The BCR is accessed with CRE HIGH and A[19:18] = 10b, or through the register access software sequence with DQ = 0001h on the third cycle.

**Figure 18: Bus Configuration Register Definition**




NOTE:

1. Burst wrap and length apply to both READ and WRITE operations.

## Table 4: Sequence and Burst Length

| BURST WRAP | | STARTING ADDRESS | 4-WORD BURST LENGTH | 8-WORD BURST LENGTH | 16-WORD BURST LENGTH | 32-WORD BURST LENGTH | CONTINUOUS BURST |
|---|---|---|---|---|---|---|---|
| BCR[3] | WRAP | (DECIMAL) | LINEAR | LINEAR | LINEAR | LINEAR | LINEAR |
| 0 | Yes | 0 | 0-1-2-3 | 0-1-2-3-4-5-6-7 | 0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15 | 0-1-2-...-29-30-31 | 0-1-2-3-4-5-6-... |
| | | 1 | 1-2-3-0 | 1-2-3-4-5-6-7-0 | 1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-0 | 1-2-3-...-30-31-0 | 1-2-3-4-5-6-7-... |
| | | 2 | 2-3-0-1 | 2-3-4-5-6-7-0-1 | 2-3-4-5-6-7-8-9-10-11-12-13-14-15-0-1 | 2-3-4-...-31-0-1 | 2-3-4-5-6-7-8-... |
| | | 3 | 3-0-1-2 | 3-4-5-6-7-0-1-2 | 3-4-5-6-7-8-9-10-11-12-13-14-15-0-1-2 | 3-4-5-...-0-1-2 | 3-4-5-6-7-8-9-... |
| | | 4 | | 4-5-6-7-0-1-2-3 | 4-5-6-7-8-9-10-11-12-13-14-15-0-1-2-3 | 4-5-6-...-1-2-3 | 4-5-6-7-8-9-10-... |
| | | 5 | | 5-6-7-0-1-2-3-4 | 5-6-7-8-9-10-11-12-13-14-15-0-1-2-3-4 | 5-6-7-...-2-3-4 | 5-6-7-8-9-10-11-... |
| | | 6 | | 6-7-0-1-2-3-4-5 | 6-7-8-9-10-11-12-13-14-15-0-1-2-3-4-5 | 6-7-8-...-3-4-5 | 6-7-8-9-10-11-12- |
| | | 7 | | 7-0-1-2-3-4-5-6 | 7-8-9-10-11-12-13-14-15-0-1-2-3-4-5-6 | 7-8-9-...-4-5-6 | 7-8-9-10-11-12-13-... |
| | | ... | | | ... | ... | ... |
| | | 14 | | | 14-15-0-1-2-3-4-5-6-7-8-9-10-11-12-13 | 14-15-16-...-11-12-13 | 14-15-16-17-18-19-20-... |
| | | 15 | | | 15-0-1-2-3-4-5-6-7-8-9-10-11-12-13-14 | 15-16-17-...-12-13-14 | 15-16-17-18-19-20-21-... |
| | | ... | | | | ... | ... |
| | | 30 | | | | 30-31-0-...-27-28-29 | 30-31-32-33-34-... |
| | | 31 | | | | 31-0-1-...-28-29-30 | 31-32-33-34-35-... |
| 1 | No | 0 | 0-1-2-3 | 0-1-2-3-4-5-6-7 | 0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15 | 0-1-2...--29-30-31 | 0-1-2-3-4-5-6-... |
| | | 1 | 1-2-3-4 | 1-2-3-4-5-6-7-8 | 1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-16 | 1-2-3-...-30-31-32 | 1-2-3-4-5-6-7-... |
| | | 2 | 2-3-4-5 | 2-3-4-5-6-7-8-9 | 2-3-4-5-6-7-8-9-10-11-12-13-14-15-16-17 | 2-3-4-...-31-32-33 | 2-3-4-5-6-7-8-... |
| | | 3 | 3-4-5-6 | 3-4-5-6-7-8-9-10 | 3-4-5-6-7-8-9-10-11-12-13-14-15-16-17-18 | 3-4-5-...-32-33-34 | 3-4-5-6-7-8-9-... |
| | | 4 | | 4-5-6-7-8-9-10-11 | 4-5-6-7-8-9-10-11-12-13-14-15-16-17-18-19 | 4-5-6-...-33-34-35 | 4-5-6-7-8-9-10-... |
| | | 5 | | 5-6-7-8-9-10-11-12 | 5-6-7-8-9-10-11-12-13-...-15-16-17-18-19-20 | 5-6-7-...-34-35-36 | 5-6-7-8-9-10-11... |
| | | 6 | | 6-7-8-9-10-11-12-13 | 6-7-8-9-10-11-12-13-14-...-16-17-18-19-20-21 | 6-7-8-...-35-36-37 | 6-7-8-9-10-11-12... |
| | | 7 | | 7-8-9-10-11-12-13-14 | 7-8-9-10-11-12-13-14-...-17-18-19-20-21-22 | 7-8-9-...-36-37-38 | 7-8-9-10-11-12-13... |
| | | ... | | | ... | ... | ... |
| | | 14 | | | 14-15-16-17-18-19-...-23-24-25-26-27-28-29 | 14-15-16-...-43-44-45 | 14-15-16-17-18-19-20-... |
| | | 15 | | | 15-16-17-18-19-20-...-24-25-26-27-28-29-30 | 15-16-17-...-44-45-46 | 15-16-17-18-19-20-21-... |
| | | ... | | | | ... | ... |
| | | 30 | | | | 30-31-32-...-59-60-61 | 30-31-32-33-34-35-36-... |
| | | 31 | | | | 31-32-33-...-60-61-62 | 31-32-33-34-35-36-37-... |

### Burst Length (BCR[2:0])
### Default = Continuous Burst

Burst lengths define the number of words the device outputs during burst READ and WRITE operations. The device supports a burst length of 4, 8, 16, or 32 words. The device can also be set in continuous burst mode where data is accessed sequentially without regard to address boundaries; the internal address wraps to 000000h if the burst goes past the last address.

### Burst Wrap (BCR[3]) Default = No Wrap

The burst-wrap option determines if a 4-, 8-, 16-, or 32-word READ or WRITE burst wraps within the burst length, or steps through sequential addresses. If the wrap option is not enabled, the device accesses data from sequential addresses without regard to burst boundaries; the internal address wraps to 000000h if the burst goes past the last address.

### Drive Strength (BCR[5:4])
### Default = Outputs Use Half-Drive Strength

The output driver strength can be altered to full, one-half, or one-quarter strength to adjust for different data bus loading scenarios. The reduced-strength options are intended for stacked chip (Flash + CellularRAM) environments when there is a dedicated memory bus. The reduced-drive-strength option minimizes the noise generated on the data bus during READ operations. Full output drive strength should be selected when using a discrete CellularRAM device in a more heavily loaded data bus environment. Outputs are configured at half-drive strength during testing. See Table 5 for additional information.

## Table 5: Drive Strength

| BCR[5] | BCR[4] | DRIVE STRENGTH | IMPEDANCE TYP (Ω) | USE RECOMMENDATION |
|---|---|---|---|---|
| 0 | 0 | Full | 25–30 | $C_L$ = 30pF to 50pF |
| 0 | 1 | 1/2 (default) | 50 | $C_L$ = 15pF to 30pF<br>104 MHz at light load |
| 1 | 0 | 1/4 | 100 | $C_L$ = 15pF or lower |
| 1 | 1 | Reserved | | |

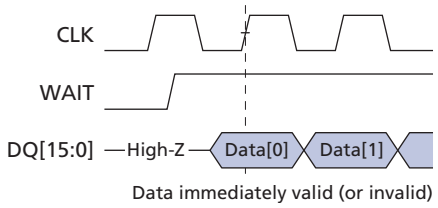
### WAIT Configuration (BCR[8])
### Default = WAIT Transitions One Clock Before Data Valid/Invalid

The WAIT configuration bit is used to determine when WAIT transitions between the asserted and the de-asserted state with respect to valid data presented on the data bus. The memory controller will use the WAIT signal to coordinate data transfer during synchronous READ and WRITE operations. When BCR[8] = 0, data will be valid or invalid on the clock edge immediately after WAIT transitions to the de-asserted or asserted state, respectively (Figures 19 and 21). When A8 = 1, the WAIT signal transitions one clock period prior to the data bus going valid or invalid (Figures 20 and 21).

### WAIT Polarity (BCR[10])
### Default = WAIT Active HIGH

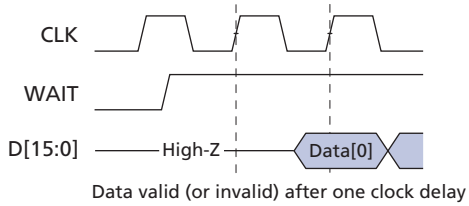
The WAIT polarity bit indicates whether an asserted WAIT output should be HIGH or LOW. This bit will determine whether the WAIT signal requires a pull-up or pull-down resistor to maintain the de-asserted state.

## Figure 19: WAIT Configuration (BCR[8] = 0)



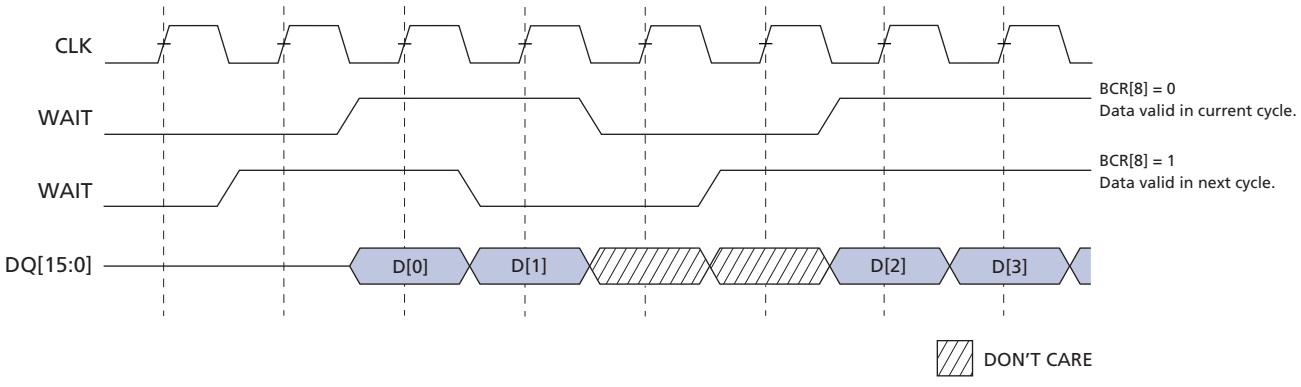

NOTE:
Data valid/invalid immediately after WAIT transitions (BCR[8] = 0). See Figure 21.

## Figure 20: WAIT Configuration (BCR[8] = 1)




NOTE:
Valid/invalid data delayed for one clock after WAIT transitions (BCR[8] = 1). See Figure 21.

## Figure 21: WAIT Configuration During Burst Operation




NOTE:
Non-default BCR setting: WAIT active LOW.

### Latency Counter (BCR[13:11])
### Default = Three Clock Latency

The latency counter bits determine how many clocks occur between the beginning of a READ or WRITE operation and the first data value transferred. For allowable latency codes, see Tables 6 and 7 and Figures 22 and 23).

### Initial Access Latency (BRC[14])
### Default = Variable

Variable initial access latency outputs data after the number of clocks set by the latency counter. However, WAIT must be monitored to detect delays caused by collisions with refresh operations.

Fixed initial access latency outputs the first data at a consistent time that allows for worst-case refresh collisions. The latency counter must be configured to match the initial latency and the clock frequency. It is not necessary to monitor WAIT with fixed initial latency. The burst begins after the number of clock cycles configured by the latency counter. The burst will pause (and WAIT will be asserted) at the boundary of a 128-word row. (See Table 7 and Figure 23 on page 25.)

### Operating Mode (BCR[15])
### Default = Asynchronous Operation

The operating mode bit selects either synchronous burst operation or the default asynchronous mode of operation.

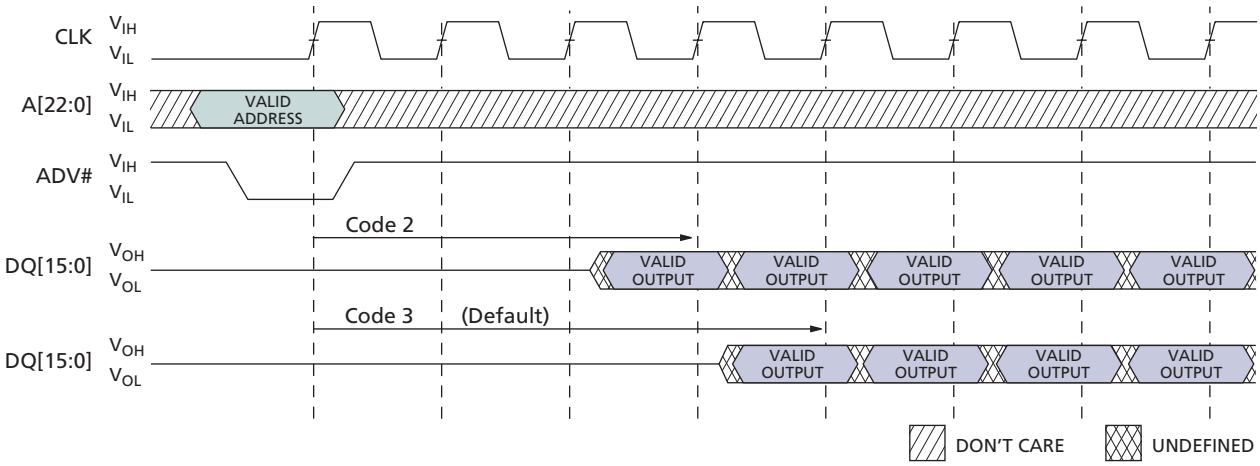
## Table 6: Variable Latency Configuration Codes

| BCR[13:11] | LATENCY CONFIGURATION CODE | LATENCY[1] | | MAX INPUT CLK FREQUENCY (MHz) | | |
|---|---|---|---|---|---|---|
| | | NORMAL | REFRESH COLLISION | -701 | -708 | -856 |
| 010 | 2 (3 clocks) | 2 | 4 | 66 (15ns) | 54 (18.5ns) | 40 (25ns) |
| 011 | 3 (4 clocks)—default | 3 | 6 | 104 (9.62ns) | 80 (12.5ns) | 66 (15ns) |
| Others | Reserved | — | — | — | — | — |

NOTE:

1. Latency is the number of clock cycles from the initiation of a burst operation until data appears. Data is transferred on the next clock cycle.

## Figure 22: Latency Counter (Variable Initial Latency, No Refresh Collision)

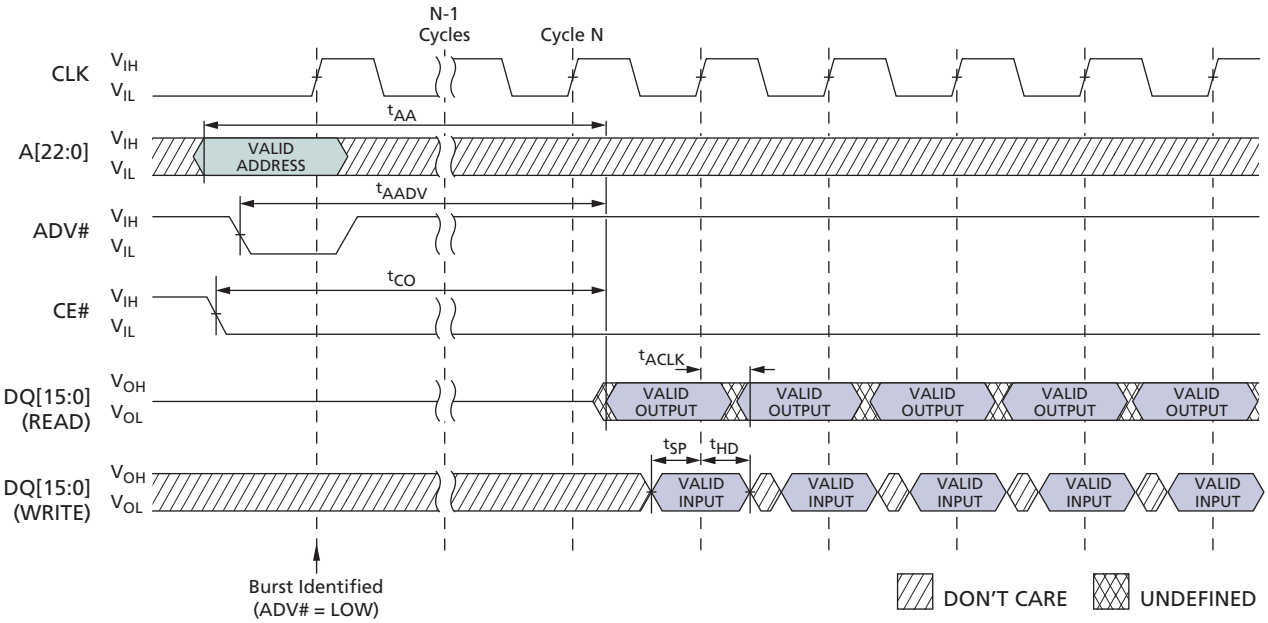


## Table 7: Fixed Latency Configuration Codes

| BCR[13:11] | LATENCY CONFIGURATION CODE | LATENCY COUNT (N) | MAX INPUT CLK FREQUENCY (MHz) | | |
|---|---|---|---|---|---|
| | | | -701 | -708 | -856 |
| 010 | 2 (3 clocks) | 2 | 33 (30ns) | 33 (30ns) | 20 (50ns) |
| 011 | 3 (4 clocks)—default | 3 | 52 (19.2ns) | 52 (19.2ns) | 33 (30ns) |
| 100 | 4 (5 clocks) | 4 | 66 (15ns) | 66 (15ns) | 40 (25ns) |
| 101 | 5 (6 clocks) | 5 | 75 (13.3ns) | 75 (13.3ns) | 52 (19.2ns) |
| 110 | 6 (7 clocks) | 6 | 104 (9.62ns)[1] | 80 (12.5ns) | 66 (15ns) |
| Others | Reserved | — | — | — | — |

NOTE:
1. Fixed latency > 80 MHz available only with Vcc/VccQ from 1.8V–1.95V.

## Figure 23: Latency Counter (Fixed Latency)



## Refresh Configuration Register

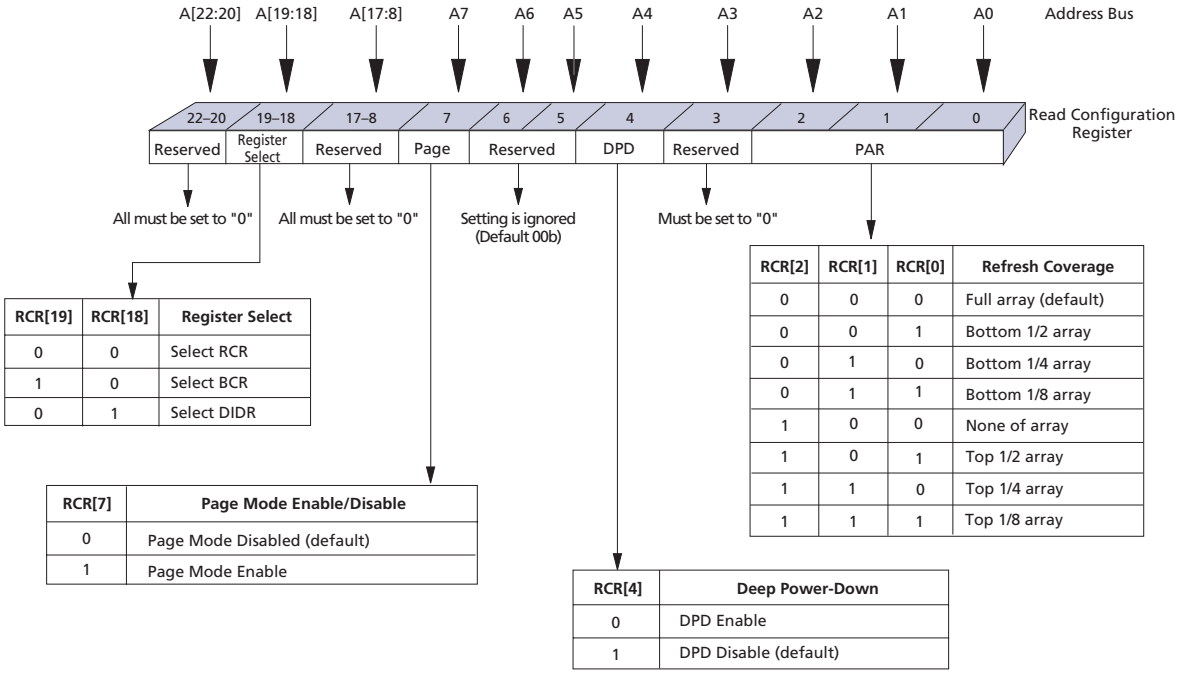
The refresh configuration register (RCR) defines how the CellularRAM device performs its transparent self refresh. Altering the refresh parameters can dramatically reduce current consumption during standby mode. Page mode control is also embedded into the RCR. Figure 24 describes the control bits used in the RCR. At power-up, the RCR is set to 0010h.

The RCR is accessed with CRE HIGH and A[19:18] = 00b; or through the register access software sequence with DQ = 0000h on the third cycle (see "Registers" on page 15.)

### Partial Array Refresh (RCR[2:0]
### Default = Full Array Refresh

The PAR bits restrict refresh operation to a portion of the total memory array. This feature allows the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, one-eighth array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map (see Table 8 on page 27).

**Figure 24: Refresh Configuration Register Mapping**




| RCR[19] | RCR[18] | Register Select |
|---|---|---|
| 0 | 0 | Select RCR |
| 1 | 0 | Select BCR |
| 0 | 1 | Select DIDR |

| RCR[2] | RCR[1] | RCR[0] | Refresh Coverage |
|---|---|---|---|
| 0 | 0 | 0 | Full array (default) |
| 0 | 0 | 1 | Bottom 1/2 array |
| 0 | 1 | 0 | Bottom 1/4 array |
| 0 | 1 | 1 | Bottom 1/8 array |
| 1 | 0 | 0 | None of array |
| 1 | 0 | 1 | Top 1/2 array |
| 1 | 1 | 0 | Top 1/4 array |
| 1 | 1 | 1 | Top 1/8 array |

| RCR[7] | Page Mode Enable/Disable |
|---|---|
| 0 | Page Mode Disabled (default) |
| 1 | Page Mode Enable |

| RCR[4] | Deep Power-Down |
|---|---|
| 0 | DPD Enable |
| 1 | DPD Disable (default) |

## Table 8: 128Mb Address Patterns for PAR (RCR[4] = 1)

| RCR[2] | RCR[1] | RCR[0] | ACTIVE SECTION | ADDRESS SPACE | SIZE | DENSITY |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | Full die | 000000h–7FFFFFh | 8 Meg x 16 | 128Mb |
| 0 | 0 | 1 | One-half of die | 000000h–3FFFFFh | 4 Meg x 16 | 64Mb |
| 0 | 1 | 0 | One-quarter of die | 000000h–1FFFFFh | 2 Meg x 16 | 32Mb |
| 0 | 1 | 1 | One-eighth of die | 000000h–0FFFFFh | 1 Meg x 16 | 16Mb |
| 1 | 0 | 0 | None of die | 0 | 0 Meg x 16 | 0Mb |
| 1 | 0 | 1 | One-half of die | 400000h–7FFFFFh | 4 Meg x 16 | 64Mb |
| 1 | 1 | 0 | One-quarter of die | 600000h–7FFFFFh | 2 Meg x 16 | 32Mb |
| 1 | 1 | 1 | One-eighth of die | 700000h–7FFFFFh | 1 Meg x 16 | 16Mb |

### Deep Power-Down (RCR[4])
### Default = DPD Disabled

The deep power-down bit enables and disables all refresh-related activity. This mode is used if the system does not require the storage provided by the CellularRAM device. Any stored data will become corrupted when DPD is enabled. When refresh activity has been re-enabled, the CellularRAM device will require 150µs to perform an initialization procedure before normal operations can resume.

Deep power-down is enabled by setting RCR[4] = 0 and taking CE# HIGH. Taking CE# LOW disables DPD and sets RCR[4] = 1; it is not necessary to write to the RCR to disable DPD. DPD can be enabled using CRE or the software sequence to access the RCR.

### Page Mode Operation (RCR[7])
### Default = Disabled

The page mode operation bit determines whether page mode is enabled for asynchronous READ operations. In the power-up default state, page mode is disabled.

## *Device Identification Register*

The DIDR provides information on the device manufacturer, CellularRAM generation, and the specific device configuration. Table 9 describes the bit fields in the DIDR. This register is read-only, and is set to 0343h (see Table 9).

The DIDR is accessed with CRE HIGH and A[19:18] = 01b, or through the register access software sequence with DQ = 0002h on the third cycle.

## Table 9: Device Identification Register Mapping

| BIT FIELD | DIDR[15] | DIDR[14:11] | | DIDR[10:8] | DIDR[7:5] | DIDR[4:0] |
|---|---|---|---|---|---|---|
| Field Name | Reserved | Device Version | | Device Density | CellularRAM Generation | Vendor ID |
| | | Bit Setting | Version | | | |
| Bit Setting | 0b | 0000b | 1st | 011b | 010b | 00011b |
| | | 0001b | 2nd | | | |
| | | ⋮ | ⋮ | | | |
| Meaning | — | | | 128Mb | CellularRAM 1.5 | Micron |

## Absolute Maximum Ratings

Voltage to Any Ball Except VCC, VCCQ Relative to VSS
0.50V to (4.0V or VCCQ + 0.3V, whichever is less)
Voltage on VCC Supply Relative to VSS. . -0.2V to +2.45V
Voltage on VCCQ Supply Relative to VSS -0.2V to +2.45V
Storage Temperature (plastic). . . . . -55ºC to +150ºC
Operating Temperature (case)
Wireless. . . . . -30ºC to +85ºC
Industrial . . . . . -40ºC to +85ºC
Soldering Temperature and Time
10s (solder ball only) . . . . . +260ºC

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Table 10: Electrical Characteristics and Operating Conditions

Wireless Temperature (-30°C < $T_C$ < +85°C); Industrial Temperature (-40°C < $T_C$ < +85°C)

| DESCRIPTION | CONDITIONS | SYMBOL | | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Supply Voltage | | VCC | | 1.7 | 1.95 | V | |
| I/O Supply Voltage | | VCCQ | W: 1.8V | 1.7 | 1.95 | V | |
| Input High Voltage | | VIH | | VCCQ - 0.4 | VCCQ + 0.2 | V | 1 |
| Input Low Voltage | | VIL | | -0.20 | 0.4 | V | 2 |
| Output High Voltage | IOH = -0.2mA | VOH | | 0.80 VCCQ | | V | 3 |
| Output Low Voltage | IOL = +0.2mA | VOL | | | 0.20 VCCQ | V | 3 |
| Input Leakage Current | VIN = 0 to VCCQ | ILI | | | 1 | µA | |
| Output Leakage Current | OE# = VIH or Chip Disabled | ILO | | | 1 | µA | |
| Operating Current | | | | | | | |
| Asynchronous Random READ/WRITE | VIN = VCCQ or 0V Chip Enabled, IOUT = 0 | ICC1 | -70 | | 30 | mA | 4 |
| | | | -85 | | 25 | | |
| Asynchronous Page READ | | ICC1P | -70 | | 15 | mA | 4 |
| | | | -85 | | 12 | | |
| Initial Access, Burst READ/WRITE | | ICC2 | 104 MHz | | 40 | mA | 4 |
| | | | 80 MHz | | 35 | | |
| | | | 66 MHz | | 30 | | |
| Continuous Burst READ | | ICC3R | 104 MHz | | 25 | mA | 4 |
| | | | 80 MHz | | 20 | | |
| | | | 66 MHz | | 18 | | |
| Continuous Burst WRITE | | ICC3W | 104 MHz | | 40 | mA | 4 |
| | | | 80 MHz | | 35 | | |
| | | | 66 MHz | | 30 | | |
| Standby Current | VIN = VCCQ or 0V CE# = VCCQ | ISB | Standard | | 200 | µA | 5 |
| | | | Low-Power (L) | | 160 | | |

NOTE:

1. Input signals may overshoot to VccQ + 1.0V for periods less than 2ns during transitions.
2. Input signals may undershoot to Vss - 1.0V for periods less than 2ns during transitions.
3. BCR[5:4] = 01b (default setting of one-half drive strength).
4. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add the current required to drive output capacitance expected in the actual system.
5. ISB (MAX) values measured with PAR set to FULL ARRAY and at +85°C. In order to achieve low standby current, all inputs must be driven to either VCCQ or VSS. ISB might be slightly higher for up to 500ms after power-up, or after changes to the PAR array partition.

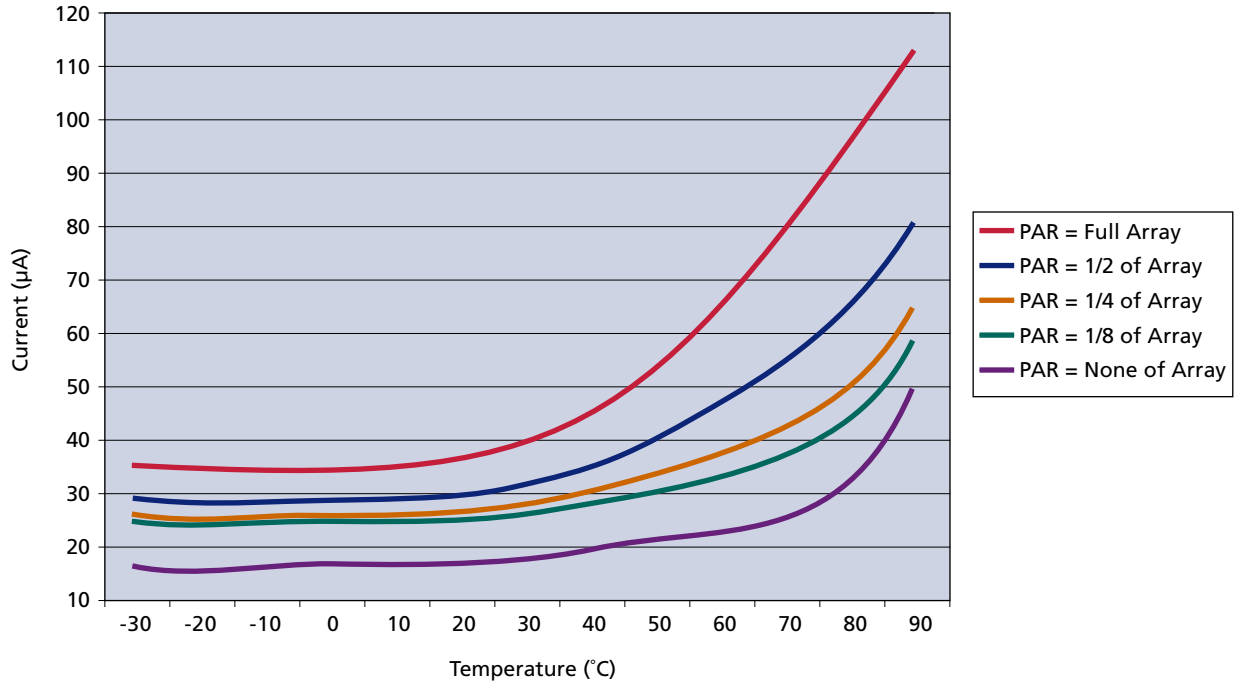
## Table 11: Partial Array Refresh Specifications and Conditions

| DESCRIPTION | CONDITIONS | SYMBOL | | ARRAY PARTITION | MAX | UNITS |
|---|---|---|---|---|---|---|
| Partial Array Refresh Standby Current | $V_{IN}$ = $V_{CCQ}$ or 0V, CE# = $V_{CCQ}$ | $I_{PAR}$ | Standard Power (no desig.) | Full | 200 | µA |
| | | | | 1/2 | 170 | |
| | | | | 1/4 | 155 | |
| | | | | 1/8 | 150 | |
| | | | | 0 | 140 | |
| | | | Low-Power Option (L) | Full | 160 | µA |
| | | | | 1/2 | 130 | |
| | | | | 1/4 | 115 | |
| | | | | 1/8 | 110 | |
| | | | | 0 | 100 | |

NOTE:

$I_{PAR}$ (MAX) values measured at 85°C. $I_{PAR}$ might be slightly higher for up to 500ms after changes to the PAR array partition.

## Figure 25: Typical Refresh Current vs. Temperature ($I_{TCR}$)




## Table 12: Deep Power-Down Specifications

| DESCRIPTION | CONDITIONS | SYMBOL | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Deep Power-Down | $V_{IN}$ = $V_{CCQ}$ or 0V; $V_{CC}$, $V_{CCQ}$ = 1.95V; +85°C | $I_{ZZ}$ | 3 | 25 | µA |

NOTE:

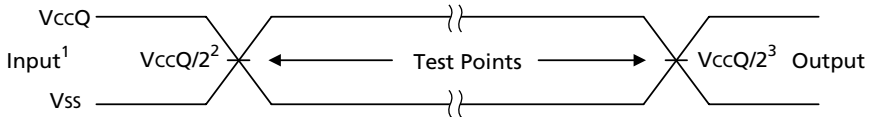
Typical (TYP) $I_{ZZ}$ value applies across all operating temperatures and voltages.

## Table 13: Capacitance

| DESCRIPTION | CONDITIONS | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Capacitance | $T_C$ = +25°C; f = 1 MHz; | $C_{IN}$ | 2.0 | 6 | pF | 1 |
| Input/Output Capacitance (DQ) | $V_{IN}$ = 0V | $C_{IO}$ | 3.5 | 6 | pF | 1 |

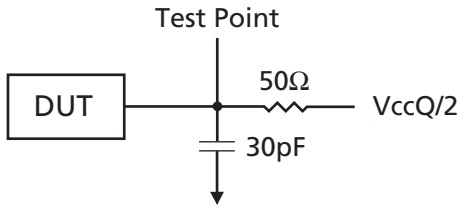
NOTE:
1. These parameters are verified in device characterization and are not 100% tested.

## Figure 26: AC Input/Output Reference Waveform




NOTE:
1. AC test inputs are driven at VccQ for a logic 1 and Vss for a logic 0. Input rise and fall times (10% to 90%) < 1.6ns.
2. Input timing begins at VccQ/2.
3. Output timing ends at VccQ/2.

## Figure 27: AC Output Load Circuit




NOTE:
All tests are performed with the outputs configured for default setting of half drive strength (BCR[5:4] = 01b).

## Table 14: Asynchronous READ Cycle Timing Requirements

All tests are performed with the outputs configured for default setting of half drive strength (BCR[5:4] = 01b).

| PARAMETER | SYMBOL | -701/708 | | -856 | | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | | |
| Address Access Time | $^tAA$ | | 70 | | 85 | ns | |
| ADV# Access Time | $^tAADV$ | | 70 | | 85 | ns | |
| Page Access Time | $^tAPA$ | | 20 | | 25 | ns | |
| Address Hold from ADV# HIGH | $^tAVH$ | 2 | | 2 | | ns | |
| Address Setup to ADV# HIGH | $^tAVS$ | 5 | | 5 | | ns | |
| LB#/UB# Access Time | $^tBA$ | | 70 | | 85 | ns | |
| LB#/UB# Disable to DQ High-Z Output | $^tBHZ$ | | 8 | | 8 | ns | 1 |
| LB#/UB# Enable to Low-Z Output | $^tBLZ$ | 10 | | 10 | | ns | 2 |
| Maximum CE# Pulse Width | $^tCEM$ | | 4 | | 4 | µs | 3 |
| CE# LOW to WAIT Valid | $^tCEW$ | 1 | 7.5 | 1 | 7.5 | ns | |
| Chip Select Access Time | $^tCO$ | | 70 | | 85 | ns | |
| CE# LOW to ADV# HIGH | $^tCVS$ | 7 | | 7 | | ns | |
| Chip Disable to DQ and WAIT High-Z Output | $^tHZ$ | | 8 | | 8 | ns | 1 |
| Chip Enable to Low-Z Output | $^tLZ$ | 10 | | 10 | | ns | 2 |
| Output Enable to Valid Output | $^tOE$ | | 20 | | 20 | ns | |
| Output Hold from Address Change | $^tOH$ | 5 | | 5 | | ns | |
| Output Disable to DQ High-Z Output | $^tOHZ$ | | 8 | | 8 | ns | 1 |
| Output Enable to Low-Z Output | $^tOLZ$ | 3 | | 3 | | ns | 2 |
| Page Cycle Time | $^tPC$ | 20 | | 25 | | ns | |
| READ Cycle Time | $^tRC$ | 70 | | 85 | | ns | |
| ADV# Pulse Width LOW | $^tVP$ | 5 | | 7 | | ns | |
| ADV# Pulse Width HIGH | $^tVPH$ | 10 | | 10 | | ns | |

NOTE:

1. Low-Z to High-Z timings are tested with the circuit shown in Figure 27 on page 30. The High-Z timings measure a 100mV transition from either $V_{OH}$ or $V_{OL}$ toward $V_{CCQ}/2$.
2. High-Z to Low-Z timings are tested with the circuit shown in Figure 27 on page 30. The Low-Z timings measure a 100mV transition away from the High-Z ($V_{CCQ}/2$) level toward either $V_{OH}$ or $V_{OL}$.
3. Page mode enabled only.

## Table 15: Burst READ Cycle Timing Requirements

All tests are performed with the outputs configured for default setting of half drive strength (BCR[5:4] = 01b).

| PARAMETER | SYMBOL | -701 | | -708 | | -856 | | UNITS | NOTES |
|---|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| Address Access Time (Fixed Latency) | $^{t}AA$ | | 70 | | 70 | | 85 | ns | |
| ADV# Access Time (Fixed Latency) | $^{t}AADV$ | | 70 | | 70 | | 85 | ns | |
| Burst to READ Access Time (Variable Latency) | $^{t}ABA$ | | 35 | | 46 | | 55 | ns | |
| CLK to Output Delay | $^{t}ACLK$ | | 7 | | 9 | | 11 | ns | |
| Address Hold from ADV# HIGH (Fixed Latency) | $^{t}AVH$ | 2 | | 2 | | 2 | | ns | |
| Burst OE# LOW to Output Delay | $^{t}BOE$ | | 20 | | 20 | | 20 | ns | |
| CE# HIGH between Subsequent Burst or Mixed-Mode Operations | $^{t}CBPH$ | 5 | | 6 | | 8 | | ns | 1 |
| Maximum CE# Pulse Width | $^{t}CEM$ | | 4 | | 4 | | 4 | µs | 1 |
| CE# LOW to WAIT Valid | $^{t}CEW$ | 1 | 7.5 | 1 | 7.5 | 1 | 7.5 | ns | |
| CLK Period | $^{t}CLK$ | 9.62 | | 12.5 | | 15 | | ns | |
| Chip Select Access Time (Fixed Latency) | $^{t}CO$ | | 70 | | 70 | | 85 | ns | |
| CE# Setup Time to Active CLK Edge | $^{t}CSP$ | 3 | | 4 | | 5 | | ns | |
| Hold Time from Active CLK Edge | $^{t}HD$ | 2 | | 2 | | 2 | | ns | |
| Chip Disable to DQ and WAIT High-Z Output | $^{t}HZ$ | | 8 | | 8 | | 8 | ns | 2 |
| CLK Rise or Fall Time | $^{t}KHKL$ | | 1.6 | | 1.8 | | 2.0 | ns | |
| CLK to WAIT Valid | $^{t}KHTL$ | | 7 | | 9 | | 11 | ns | |
| CLK to DQ High-Z Output | $^{t}KHZ$ | 3 | 8 | 3 | 8 | 3 | 8 | ns | |
| CLK to Low-Z Output | $^{t}KLZ$ | 2 | 5 | 2 | 5 | 2 | 5 | ns | |
| Output HOLD from CLK | $^{t}KOH$ | 2 | | 2 | | 2 | | ns | |
| CLK HIGH or LOW Time | $^{t}KP$ | 3 | | 4 | | 5 | | ns | |
| Output Disable to DQ High-Z Output | $^{t}OHZ$ | | 8 | | 8 | | 8 | ns | 2 |
| Output Enable to Low-Z Output | $^{t}OLZ$ | 3 | | 3 | | 3 | | ns | 3 |
| Setup Time to Active CLK Edge | $^{t}SP$ | 3 | | 3 | | 3 | | ns | |

NOTE:

1. A refresh opportunity must be provided every $^{t}CEM$. A refresh opportunity is satisfied by either of the following two conditions: a) clocked CE# HIGH, or b) CE# HIGH for longer than 15ns.
2. Low-Z to High-Z timings are tested with the circuit shown in Figure 27 on page 30. The High-Z timings measure a 100mV transition from either $V_{OH}$ or $V_{OL}$ toward $V_{CC}Q/2$.
3. High-Z to Low-Z timings are tested with the circuit shown in Figure 27 on page 30. The Low-Z timings measure a 100mV transition away from the High-Z ($V_{CC}Q/2$) level toward either $V_{OH}$ or $V_{OL}$.

## Table 16: Asynchronous WRITE Cycle Timing Requirements

| PARAMETER | SYMBOL | -701/708 | | -856 | | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | | |
| Address and ADV# LOW Setup Time | $^{t}AS$ | 0 | | 0 | | ns | |
| Address Hold from ADV# Going HIGH | $^{t}AVH$ | 2 | | 2 | | ns | |
| Address Setup to ADV# Going HIGH | $^{t}AVS$ | 5 | | 5 | | ns | |
| Address Valid to End of WRITE | $^{t}AW$ | 70 | | 85 | | ns | |
| LB#/UB# Select to End of WRITE | $^{t}BW$ | 70 | | 85 | | ns | |
| CE# LOW to WAIT Valid | $^{t}CEW$ | 1 | 7.5 | 1 | 7.5 | ns | |
| CE# HIGH between Subsequent Async Operations | $^{t}CPH$ | 5 | | 5 | | ns | |
| CE# LOW to ADV# HIGH | $^{t}CVS$ | 7 | | 7 | | ns | |
| Chip Enable to End of WRITE | $^{t}CW$ | 70 | | 85 | | ns | |
| Data Hold from WRITE Time | $^{t}DH$ | 0 | | 0 | | ns | |
| Data WRITE Setup Time | $^{t}DW$ | 20 | | 20 | | ns | |
| Chip Disable to WAIT High-Z Output | $^{t}HZ$ | | 8 | | 8 | ns | 1 |
| Chip Enable to Low-Z Output | $^{t}LZ$ | 10 | | 10 | | ns | 2 |
| End WRITE to Low-Z Output | $^{t}OW$ | 5 | | 5 | | ns | 2 |
| ADV# Pulse Width | $^{t}VP$ | 5 | | 7 | | ns | |
| ADV# Pulse Width HIGH | $^{t}VPH$ | 10 | | 10 | | ns | |
| ADV# Setup to End of WRITE | $^{t}VS$ | 70 | | 85 | | ns | |
| WRITE Cycle Time | $^{t}WC$ | 70 | | 85 | | ns | |
| WRITE to DQ High-Z Output | $^{t}WHZ$ | | 8 | | 8 | ns | 1 |
| WRITE Pulse Width | $^{t}WP$ | 45 | | 55 | | ns | 3 |
| WRITE Pulse Width HIGH | $^{t}WPH$ | 10 | | 10 | | ns | |
| WRITE Recovery Time | $^{t}WR$ | 0 | | 0 | | ns | |

NOTE:

1. Low-Z to High-Z timings are tested with the circuit shown in Figure 27 on page 30. The High-Z timings measure a 100mV transition from either $V_{OH}$ or $V_{OL}$ toward $V_{CCQ}/2$.
2. High-Z to Low-Z timings are tested with the circuit shown in Figure 27 on page 30. The Low-Z timings measure a 100mV transition away from the High-Z ($V_{CCQ}/2$) level toward either $V_{OH}$ or $V_{OL}$.
3. WE# LOW time must be limited to $^{t}CEM$ (4µs).

## Table 17: Burst WRITE Cycle Timing Requirements

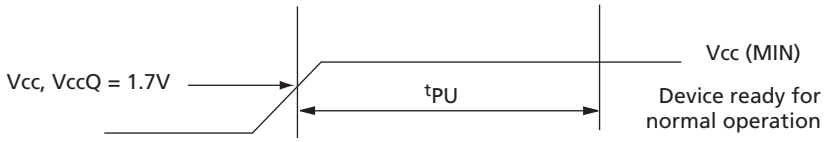
| PARAMETER | SYMBOL | -701 | | -708 | | -856 | | UNITS | NOTES |
|---|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| Address and ADV# LOW setup time | $^tAS$ | 0 | | 0 | | 0 | | ns | 1 |
| Address Hold from ADV# HIGH (Fixed Latency) | $^tAVH$ | 2 | | 2 | | 2 | | ns | |
| CE# HIGH between Subsequent Burst or Mixed-Mode Operations | $^tCBPH$ | 5 | | 6 | | 8 | | ns | 2 |
| Maximum CE# Pulse Width | $^tCEM$ | | 4 | | 4 | | 4 | µs | 2 |
| CE# LOW to WAIT Valid | $^tCEW$ | 1 | 7.5 | 1 | 7.5 | 1 | 7.5 | ns | |
| Clock Period | $^tCLK$ | 9.62 | | 12.5 | | 15 | | ns | |
| CE# Setup to CLK Active Edge | $^tCSP$ | 3 | | 4 | | 5 | | ns | |
| Hold Time from Active CLK Edge | $^tHD$ | 2 | | 2 | | 2 | | ns | |
| Chip Disable to WAIT High-Z Output | $^tHZ$ | | 8 | | 8 | | 8 | ns | 3 |
| Last Clock to ADV# LOW | $^tKADV$ | 4 | | 6 | | 6 | | ns | |
| CLK Rise or Fall Time | $^tKHKL$ | | 1.6 | | 1.8 | | 2.0 | ns | |
| Clock to WAIT Valid | $^tKHTL$ | | 7 | | 9 | | 11 | ns | |
| CLK HIGH or LOW Time | $^tKP$ | 3 | | 4 | | 5 | | ns | |
| Setup Time to Activate CLK Edge | $^tSP$ | 3 | | 3 | | 3 | | ns | |

NOTE:

1. $^tAS$ required if $^tCSP$ > 20ns.
2. A refresh opportunity must be provided every $^tCEM$. A refresh opportunity is satisfied by either of the following two conditions: a) clocked CE# HIGH, or b) CE# HIGH for longer than 15ns.
3. Low-Z to High-Z timings are tested with the circuit shown in Figure 27 on page 30. The High-Z timings measure a 100mV transition from either $V_{OH}$ or $V_{OL}$ toward $V_{CC}Q/2$.

## Timing Diagrams

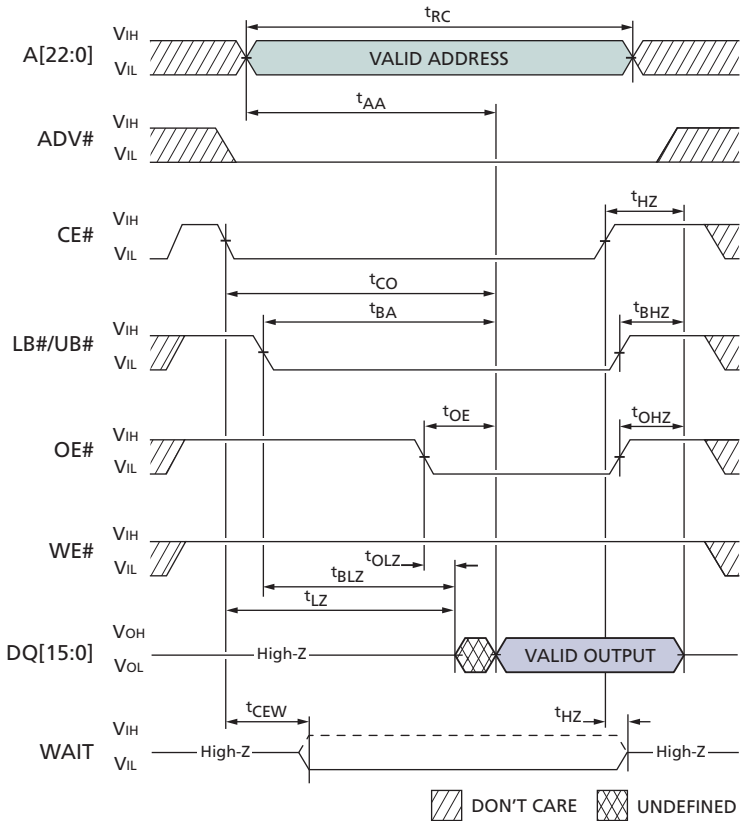
### Figure 28: Initialization Period




### Table 18: Initialization Timing Parameters

| PARAMETER | SYMBOL | -701/708 | | -856 | | UNITS | NOTE |
|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | | |
| Initialization Period (required before normal operations) | $t_{PU}$ | | 150 | | 150 | µs | |

## Figure 29: Asynchronous READ

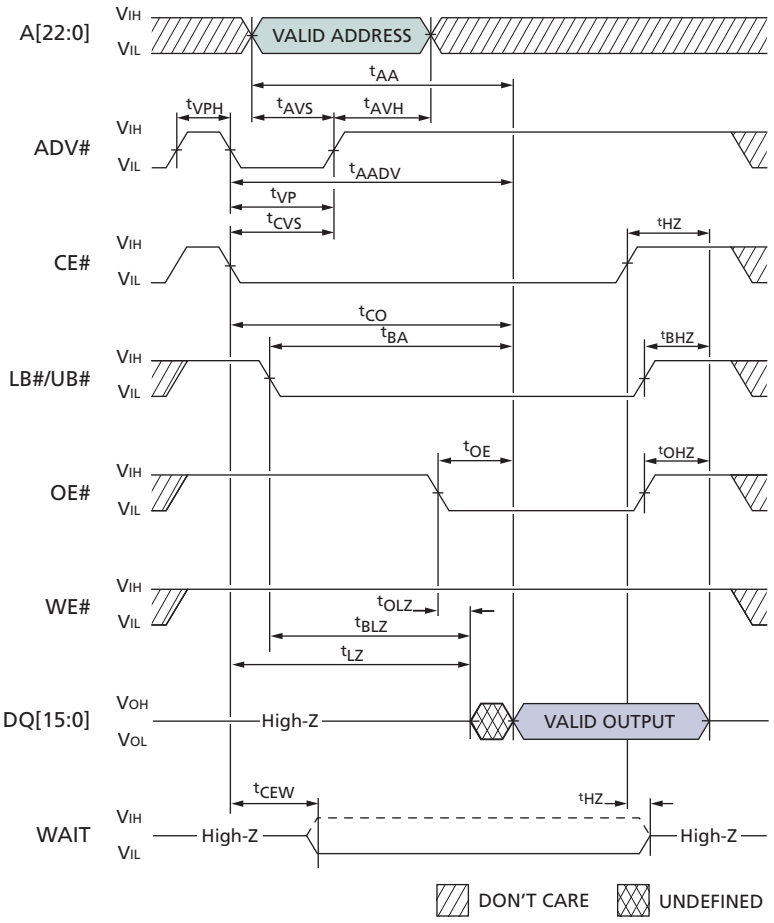



## Table 19: Asynchronous READ Timing Parameters

| SYMBOL | -701/708 MIN | -701/708 MAX | -856 MIN | -856 MAX | UNITS |
|---|---|---|---|---|---|
| $^{t}AA$ | | 70 | | 85 | ns |
| $^{t}BA$ | | 70 | | 85 | ns |
| $^{t}BHZ$ | | 8 | | 8 | ns |
| $^{t}BLZ$ | 10 | | 10 | | ns |
| $^{t}CEW$ | 1 | 7.5 | 1 | 7.5 | ns |
| $^{t}CO$ | | 70 | | 85 | ns |

| SYMBOL | -701/708 MIN | -701/708 MAX | -856 MIN | -856 MAX | UNITS |
|---|---|---|---|---|---|
| $^{t}HZ$ | | 8 | | 8 | ns |
| $^{t}LZ$ | 10 | | 10 | | ns |
| $^{t}OE$ | | 20 | | 20 | ns |
| $^{t}OHZ$ | | 8 | | 8 | ns |
| $^{t}OLZ$ | 3 | | 3 | | ns |
| $^{t}RC$ | 70 | | 85 | | ns |

## Figure 30: Asynchronous READ Using ADV#

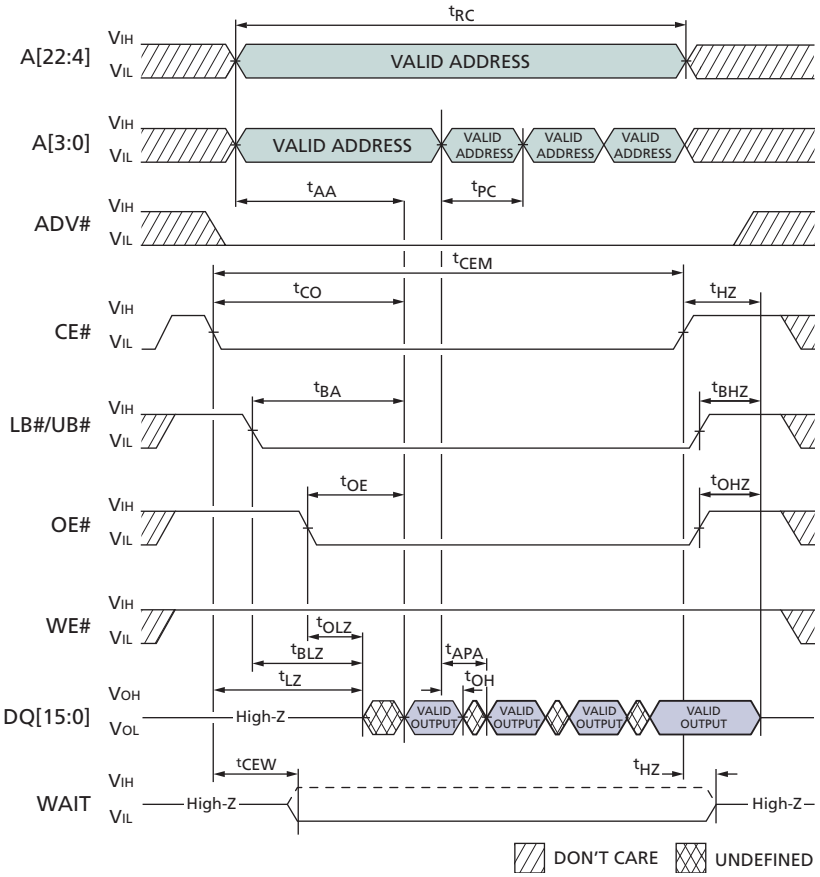



## Table 20: Asynchronous READ Timing Parameters Using ADV#

| SYMBOL | -701/708 MIN | -701/708 MAX | -856 MIN | -856 MAX | UNITS |
|---|---|---|---|---|---|
| $t_{AA}$ | | 70 | | 85 | ns |
| $t_{AADV}$ | | 70 | | 85 | ns |
| $t_{AVH}$ | 2 | | 2 | | ns |
| $t_{AVS}$ | 5 | | 5 | | ns |
| $t_{BA}$ | | 70 | | 85 | ns |
| $t_{BHZ}$ | | 8 | | 8 | ns |
| $t_{BLZ}$ | 10 | | 10 | | ns |
| $t_{CEW}$ | 1 | 7.5 | 1 | 7.5 | ns |
| $t_{CO}$ | | 70 | | 85 | ns |

| SYMBOL | -701/708 MIN | -701/708 MAX | -856 MIN | -856 MAX | UNITS |
|---|---|---|---|---|---|
| $t_{CVS}$ | 7 | | 7 | | ns |
| $t_{HZ}$ | | 8 | | 8 | ns |
| $t_{LZ}$ | 10 | | 10 | | ns |
| $t_{OE}$ | | 20 | | 20 | ns |
| $t_{OHZ}$ | | 8 | | 8 | ns |
| $t_{OLZ}$ | 3 | | 3 | | ns |
| $t_{VP}$ | 5 | | 7 | | ns |
| $t_{VPH}$ | 10 | | 10 | | ns |

## Figure 31: Page Mode READ

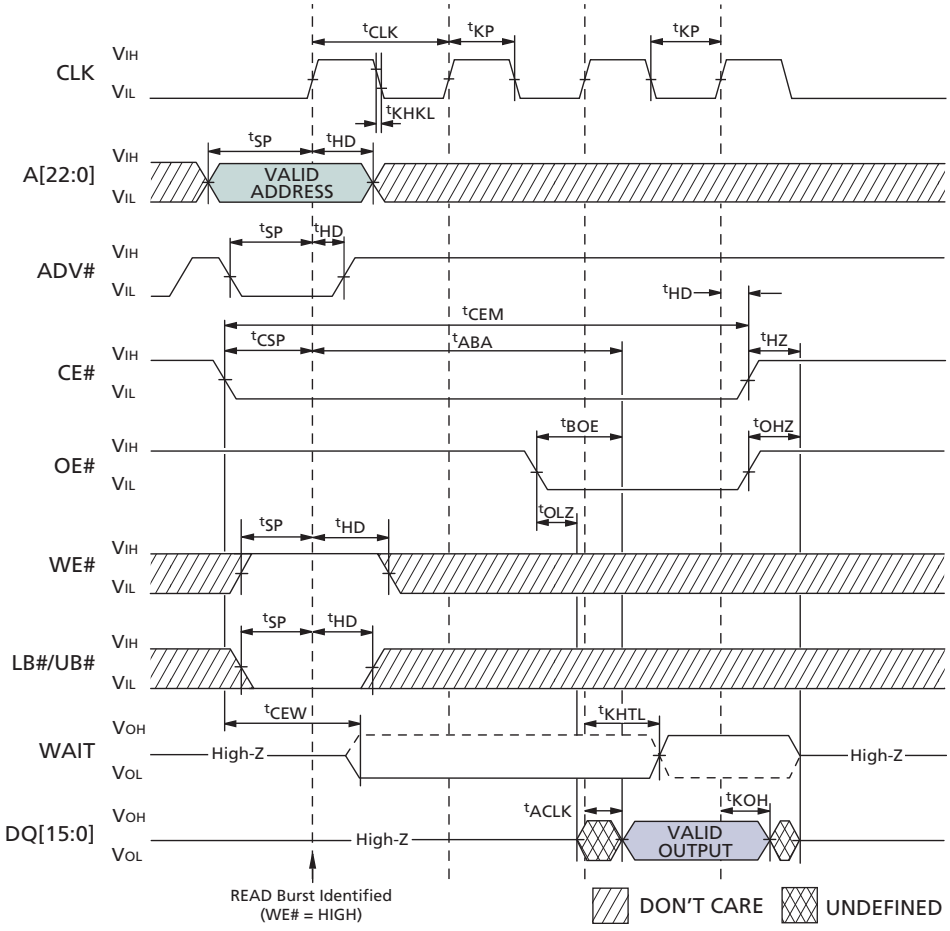



## Table 21: Asynchronous READ Timing Parameters—Page Mode Operation

| SYMBOL | -701/708 MIN | -701/708 MAX | -856 MIN | -856 MAX | UNITS |
|---|---|---|---|---|---|
| tAA | | 70 | | 85 | ns |
| tAPA | | 20 | | 25 | ns |
| tBA | | 70 | | 85 | ns |
| tBHZ | | 8 | | 8 | ns |
| tBLZ | 10 | | 10 | | ns |
| tCEM | | 4 | | 4 | µs |
| tCEW | 1 | 7.5 | 1 | 7.5 | ns |
| tCO | | 70 | | 85 | ns |

| SYMBOL | -701/708 MIN | -701/708 MAX | -856 MIN | -856 MAX | UNITS |
|---|---|---|---|---|---|
| tHZ | | 8 | | 8 | ns |
| tLZ | 10 | | 10 | | ns |
| tOE | | 20 | | 20 | ns |
| tOH | 5 | | 5 | | ns |
| tOHZ | | 8 | | 8 | ns |
| tOLZ | 3 | | 3 | | ns |
| tPC | 20 | | 25 | | ns |
| tRC | 70 | | 85 | | ns |

## Figure 32: Single-Access Burst READ Operation—Variable Latency



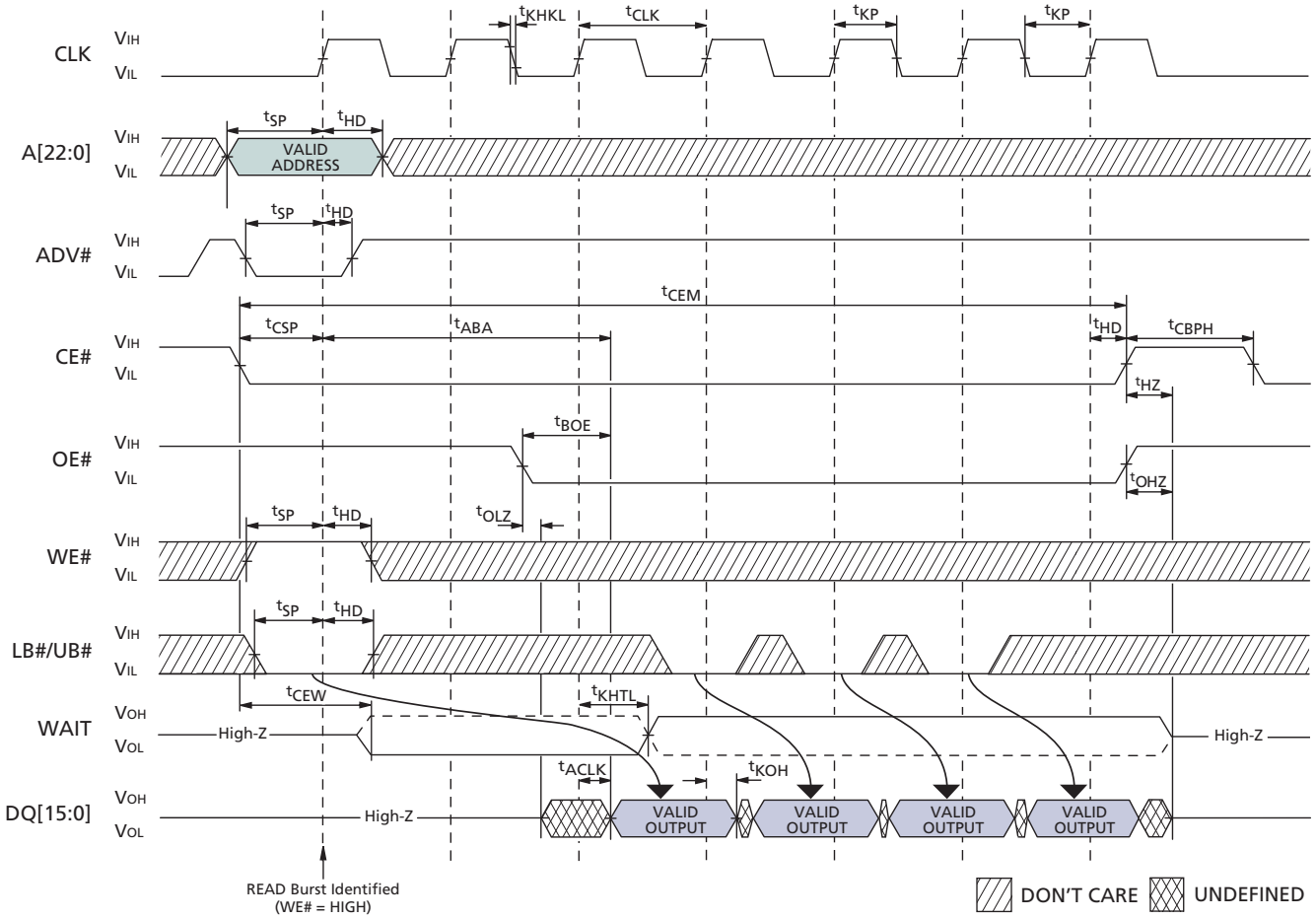

NOTE:
Non-default BCR settings: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.

## Table 22: Burst READ Timing Parameters—Single Access, Variable Latency

| | -701 | | -708 | | -856 | | |
|---|---|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | MIN | MAX | UNITS |
| tABA | | 35 | | 46 | | 55 | ns |
| tACLK | | 7 | | 9 | | 11 | ns |
| tBOE | | 20 | | 20 | | 20 | ns |
| tCEM | | 4 | | 4 | | 4 | µs |
| tCEW | 1 | 7.5 | 1 | 7.5 | 1 | 7.5 | ns |
| tCLK | 9.62 | | 12.5 | | 15 | | ns |
| tCSP | 3 | | 4 | | 5 | | ns |
| tHD | 2 | | 2 | | 2 | | ns |

| | -701 | | -708 | | -856 | | |
|---|---|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | MIN | MAX | UNITS |
| tHZ | | 8 | | 8 | | 8 | ns |
| tKHKL | | 1.6 | | 1.8 | | 2.0 | ns |
| tKHTL | | 7 | | 9 | | 11 | ns |
| tKOH | 2 | | 2 | | 2 | | ns |
| tKP | 3 | | 4 | | 5 | | ns |
| tOHZ | | 8 | | 8 | | 8 | ns |
| tOLZ | 3 | | 3 | | 3 | | ns |
| tSP | 3 | | 3 | | 3 | | ns |

## Figure 33: 4-Word Burst READ Operation—Variable Latency



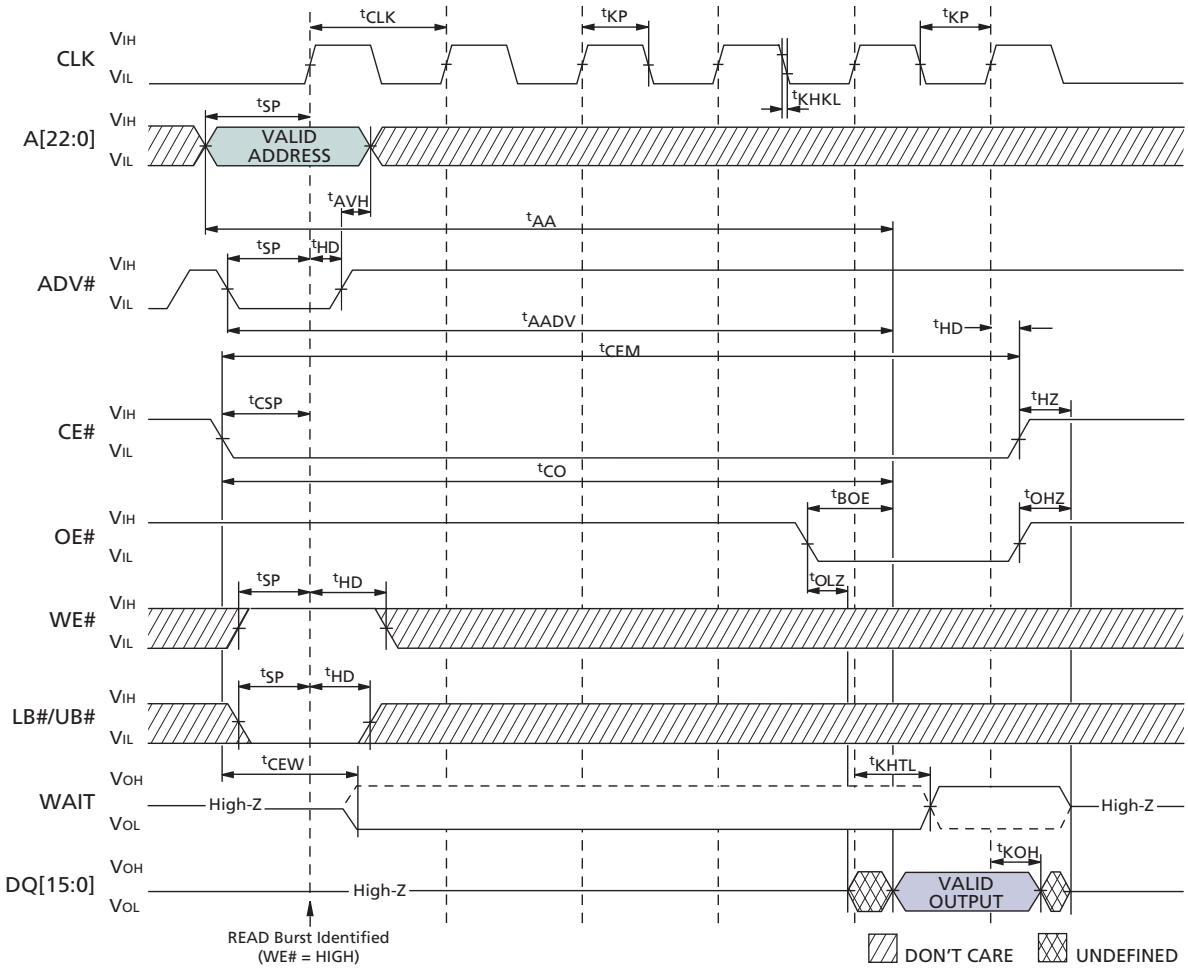

NOTE:
Non-default BCR settings: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.

## Table 23: Burst READ Timing Parameters—4-Word Burst

| SYMBOL | -701 MIN | -701 MAX | -708 MIN | -708 MAX | -856 MIN | -856 MAX | UNITS |
|---|---|---|---|---|---|---|---|
| tABA | | 35 | | 46 | | 55 | ns |
| tACLK | | 7 | | 9 | | 11 | ns |
| tBOE | | 20 | | 20 | | 20 | ns |
| tCBPH | 5 | | 6 | | 8 | | ns |
| tCEM | | 4 | | 4 | | 4 | µs |
| tCEW | 1 | 7.5 | 1 | 7.5 | 1 | 7.5 | ns |
| tCLK | 9.62 | | 12.5 | | 15 | | ns |
| tCSP | 3 | | 4 | | 5 | | ns |
| tHD | 2 | | 2 | | 2 | | ns |

| SYMBOL | -701 MIN | -701 MAX | -708 MIN | -708 MAX | -856 MIN | -856 MAX | UNITS |
|---|---|---|---|---|---|---|---|
| tHZ | | 8 | | 8 | | 8 | ns |
| tKHKL | | 1.6 | | 1.8 | | 2.0 | ns |
| tKHTL | | 7 | | 9 | | 11 | ns |
| tKOH | 2 | | 2 | | 2 | | ns |
| tKP | 3 | | 4 | | 5 | | ns |
| tOHZ | | 8 | | 8 | | 8 | ns |
| tOLZ | 3 | | 3 | | 3 | | ns |
| tSP | 3 | | 3 | | 3 | | ns |

## Figure 34: Single-Access Burst READ Operation—Fixed Latency




NOTE:

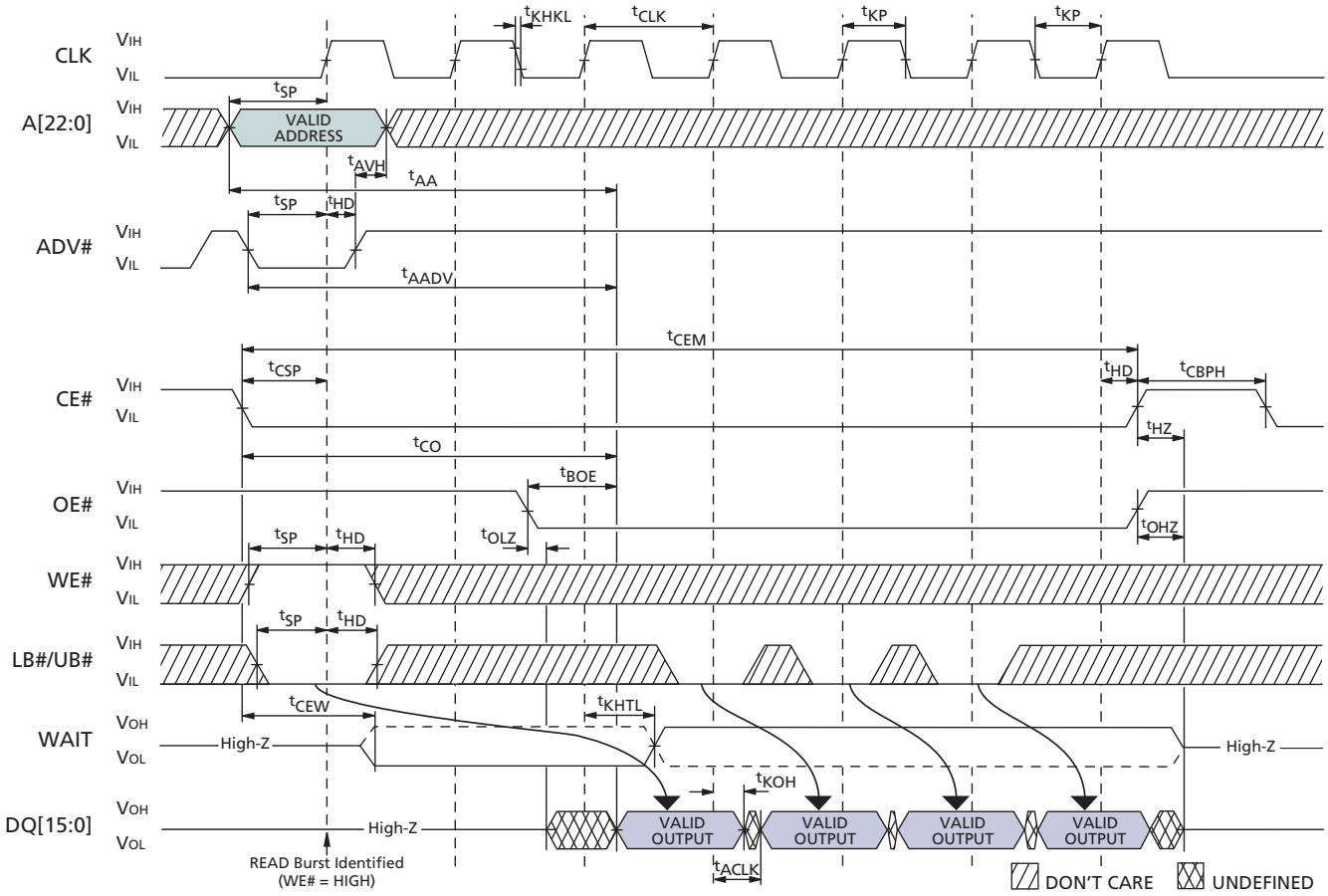
Non-default BCR settings: Fixed latency; latency code four (five clocks); WAIT active LOW; WAIT asserted during delay.

## Table 24: Burst READ Timing Parameters—Single Access, Fixed Latency

| SYMBOL | -701 MIN | -701 MAX | -708 MIN | -708 MAX | -856 MIN | -856 MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $t_{AA}$ | | 70 | | 70 | | 85 | ns |
| $t_{AADV}$ | | 70 | | 70 | | 85 | ns |
| $t_{AVH}$ | 2 | | 2 | | 2 | | ns |
| $t_{BOE}$ | | 20 | | 20 | | 20 | ns |
| $t_{CEM}$ | | 4 | | 4 | | 4 | µs |
| $t_{CEW}$ | 1 | 7.5 | 1 | 7.5 | 1 | 7.5 | ns |
| $t_{CLK}$ | 9.62 | | 12.5 | | 15 | | ns |
| $t_{CO}$ | | 70 | | 70 | | 85 | ns |
| $t_{CSP}$ | 3 | | 4 | | 5 | | ns |

| SYMBOL | -701 MIN | -701 MAX | -708 MIN | -708 MAX | -856 MIN | -856 MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $t_{HD}$ | 2 | | 2 | | 2 | | ns |
| $t_{HZ}$ | | 8 | | 8 | | 8 | ns |
| $t_{KHKL}$ | | 1.6 | | 1.8 | | 2.0 | ns |
| $t_{KHTL}$ | | 7 | | 9 | | 11 | ns |
| $t_{KOH}$ | 2 | | 2 | | 2 | | ns |
| $t_{KP}$ | 3 | | 4 | | 5 | | ns |
| $t_{OHZ}$ | | 8 | | 8 | | 8 | ns |
| $t_{OLZ}$ | 3 | | 3 | | 3 | | ns |
| $t_{SP}$ | 3 | | 3 | | 3 | | ns |

## Figure 35: 4-Word Burst READ Operation—Fixed Latency




NOTE:

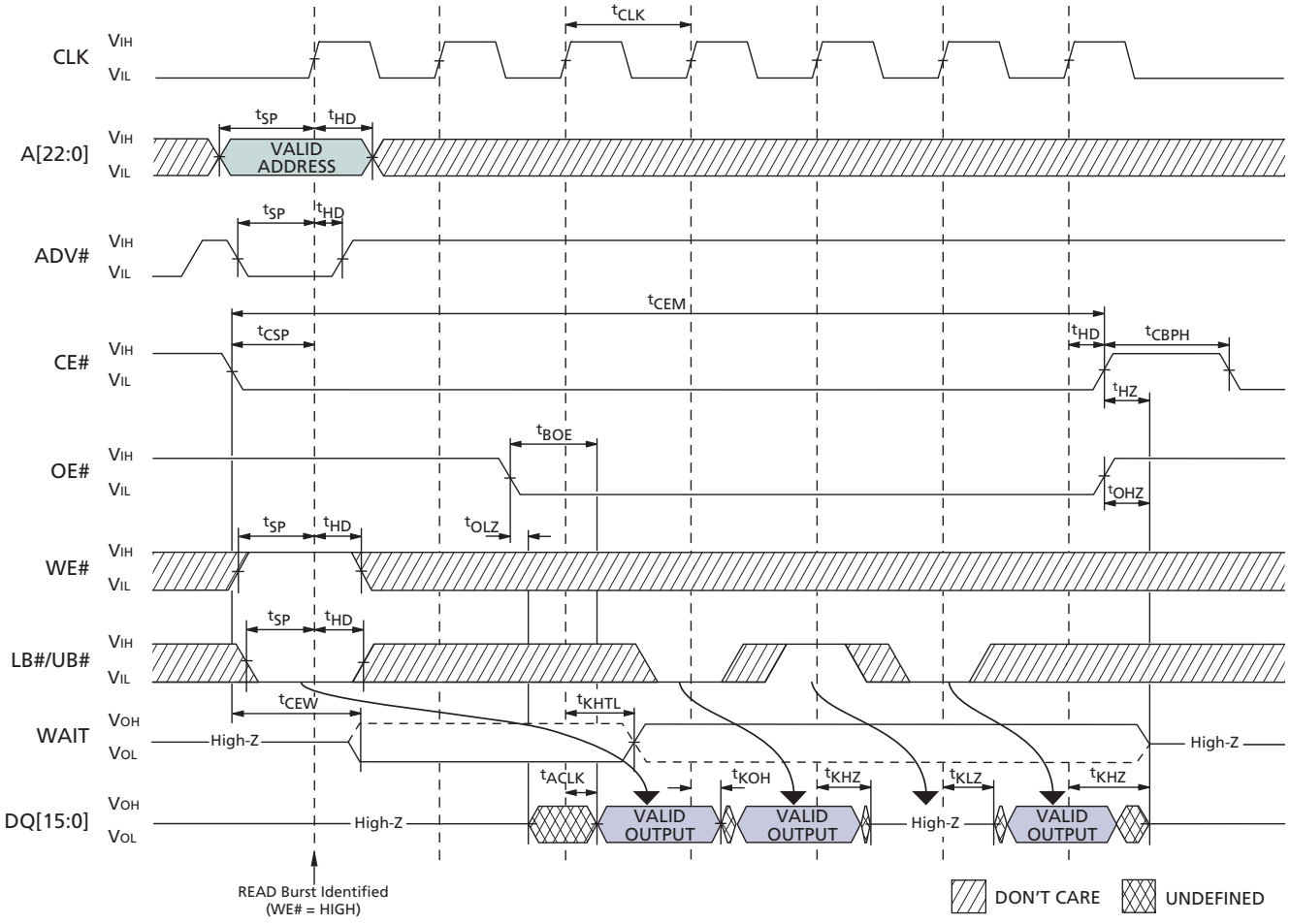
Non-default BCR settings: Fixed latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.

## Table 25: Burst READ Timing Parameters—4-Word Burst, Fixed Latency

| SYMBOL | -701 MIN | -701 MAX | -708 MIN | -708 MAX | -856 MIN | -856 MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $t_{AA}$ | | 70 | | 70 | | 85 | ns |
| $t_{AADV}$ | | 70 | | 70 | | 85 | ns |
| $t_{ACLK}$ | | 7 | | 9 | | 11 | ns |
| $t_{AVH}$ | 2 | | 2 | | 2 | | ns |
| $t_{BOE}$ | | 20 | | 20 | | 20 | ns |
| $t_{CBPH}$ | 5 | | 6 | | 8 | | ns |
| $t_{CEM}$ | | 4 | | 4 | | 4 | µs |
| $t_{CEW}$ | 1 | 7.5 | 1 | 7.5 | 1 | 7.5 | ns |
| $t_{CLK}$ | 9.62 | | 12.5 | | 15 | | ns |
| $t_{CO}$ | | 70 | | 70 | | 85 | ns |

| SYMBOL | -701 MIN | -701 MAX | -708 MIN | -708 MAX | -856 MIN | -856 MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $t_{CSP}$ | 3 | | 4 | | 5 | | ns |
| $t_{HD}$ | 2 | | 2 | | 2 | | ns |
| $t_{HZ}$ | | 8 | | 8 | | 8 | ns |
| $t_{KHKL}$ | | 1.6 | | 1.8 | | 2.0 | ns |
| $t_{KHTL}$ | | 7 | | 9 | | 11 | ns |
| $t_{KOH}$ | 2 | | 2 | | 2 | | ns |
| $t_{KP}$ | 3 | | 4 | | 5 | | ns |
| $t_{OHZ}$ | | 8 | | 8 | | 8 | ns |
| $t_{OLZ}$ | 3 | | 3 | | 3 | | ns |
| $t_{SP}$ | 3 | | 3 | | 3 | | ns |

## Figure 36: 4-Word Burst READ Operation (with LB#/UB#)




NOTE:

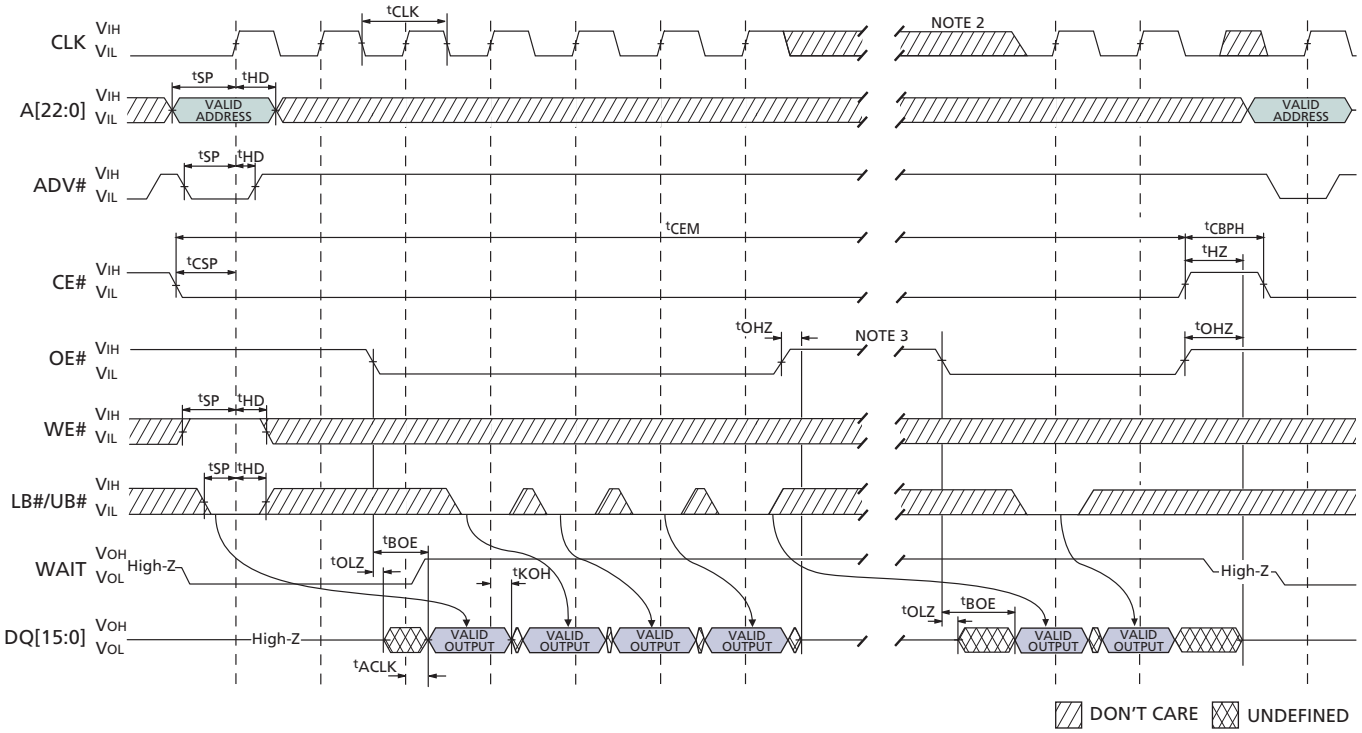
Non-default BCR settings: Fixed or variable latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay; burst length four.

## Table 26: Burst READ Timing Parameters—4-Word Burst with LB#/UB#

| SYMBOL | -701 MIN | -701 MAX | -708 MIN | -708 MAX | -856 MIN | -856 MAX | UNITS |
|---|---|---|---|---|---|---|---|
| tACLK | | 7 | | 9 | | 11 | ns |
| tBOE | | 20 | | 20 | | 20 | ns |
| tCBPH | 5 | | 6 | | 8 | | ns |
| tCEM | | 4 | | 4 | | 4 | µs |
| tCEW | 1 | 7.5 | 1 | 7.5 | 1 | 7.5 | ns |
| tCLK | 9.62 | | 12.5 | | 15 | | ns |
| tCSP | 3 | | 4 | | 5 | | ns |
| tHD | 2 | | 2 | | 2 | | ns |

| SYMBOL | -701 MIN | -701 MAX | -708 MIN | -708 MAX | -856 MIN | -856 MAX | UNITS |
|---|---|---|---|---|---|---|---|
| tHZ | | 8 | | 8 | | 8 | ns |
| tKHTL | | 7 | | 9 | | 11 | ns |
| tKHZ | 3 | 8 | 3 | 8 | 3 | 8 | ns |
| tKLZ | 2 | 5 | 2 | 5 | 2 | 5 | ns |
| tKOH | 2 | | 2 | | 2 | | ns |
| tOHZ | | 8 | | 8 | | 8 | ns |
| tOLZ | 3 | | 3 | | 3 | | ns |
| tSP | 3 | | 3 | | 3 | | ns |

## Figure 37: READ Burst Suspend




NOTE:

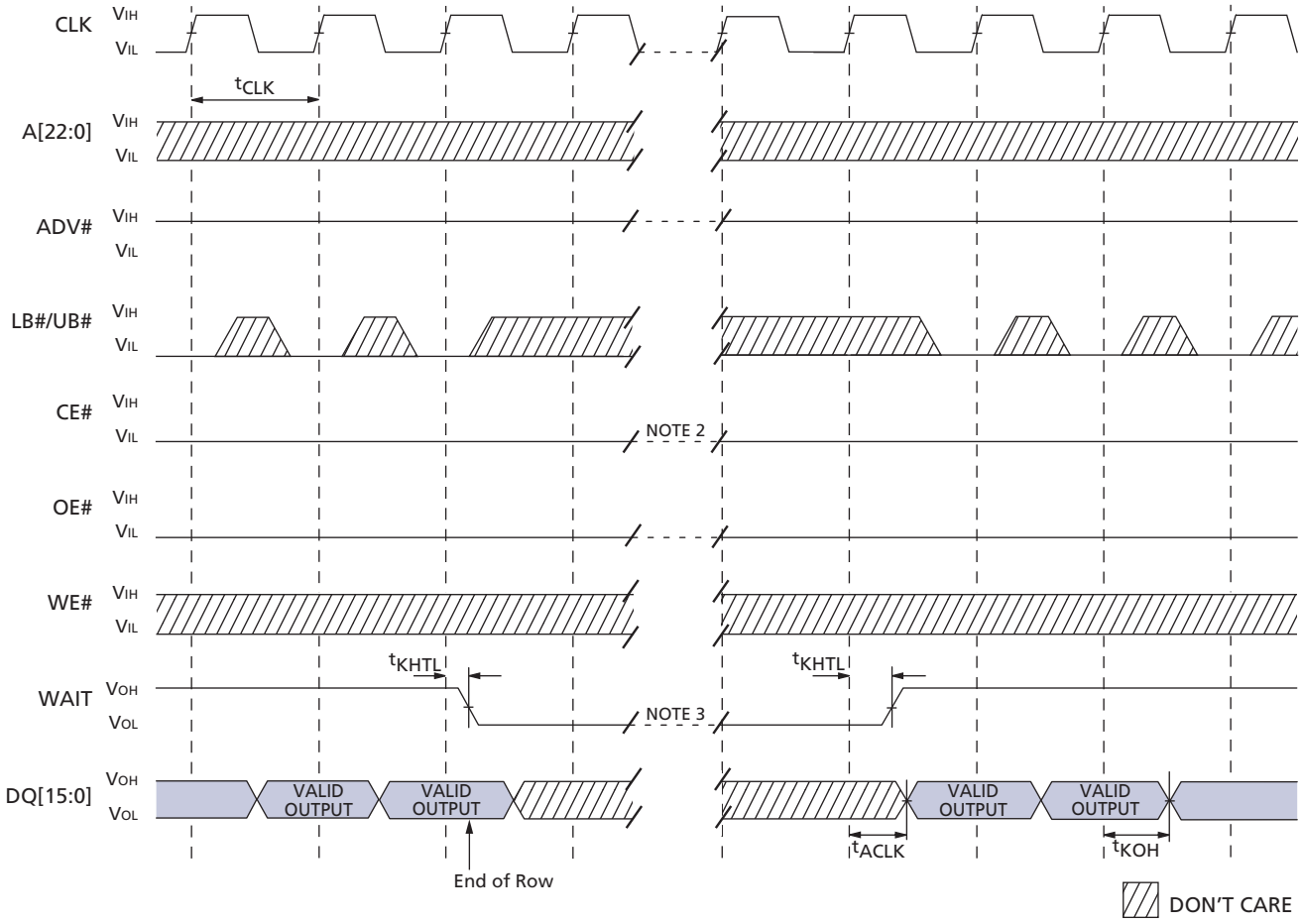
1. Non-default BCR settings for READ burst suspend: Fixed or variable latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. CLK can be stopped LOW or HIGH, but must be static, with no LOW-to-HIGH transitions during burst suspend.
3. OE# can stay LOW during burst suspend. If OE# is LOW, DQ[15:0] will continue to output valid data.

## Table 27: Burst READ Timing Parameters—Burst Suspend

| SYMBOL | -701 | | -708 | | -856 | | UNITS |
|---|---|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | MIN | MAX | |
| $^{t}$ACLK | | 7 | | 9 | | 11 | ns |
| $^{t}$BOE | | 20 | | 20 | | 20 | ns |
| $^{t}$CBPH | 5 | | 6 | | 8 | | ns |
| $^{t}$CEM | | 4 | | 4 | | 4 | µs |
| $^{t}$CLK | 9.62 | | 12.5 | | 15 | | ns |
| $^{t}$CSP | 3 | | 4 | | 5 | | ns |

| SYMBOL | -701 | | -708 | | -856 | | UNITS |
|---|---|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | MIN | MAX | |
| $^{t}$HD | 2 | | 2 | | 2 | | ns |
| $^{t}$HZ | | 8 | | 8 | | 8 | ns |
| $^{t}$KOH | 2 | | 2 | | 2 | | ns |
| $^{t}$OHZ | | 8 | | 8 | | 8 | ns |
| $^{t}$OLZ | 3 | | 3 | | 3 | | ns |
| $^{t}$SP | 3 | | 3 | | 3 | | ns |

## Figure 38: Continuous Burst READ Showing an Output Delay with BCR[8] = 0 for Variable Latency End-of-Row Condition




NOTE:

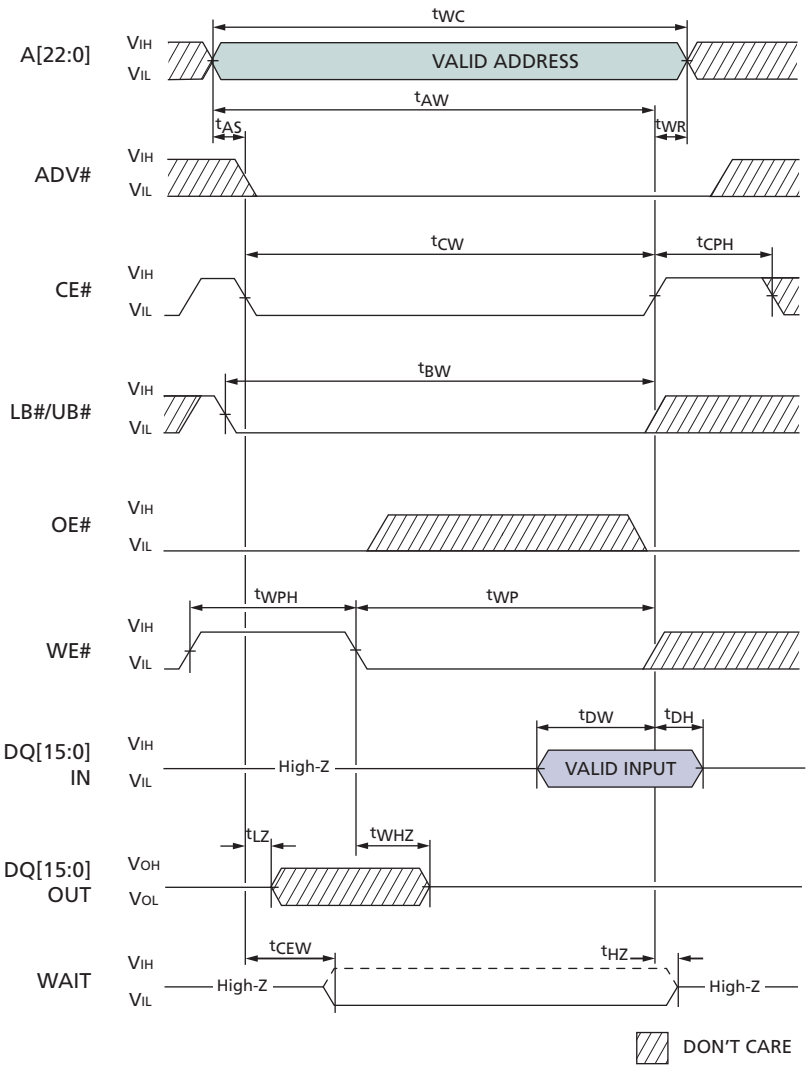
1. Non-default BCR settings for continuous burst READ, BCR[8] = 0: WAIT active LOW; WAIT asserted during delay. Do not cross row boundaries with fixed latency.
2. CE# must not remain LOW longer than $^{t}$CEM.
3. WAIT asserts for anywhere from LC to 2LC cycles. LC = Latency Code (BCR[13:11]).

## Table 28: Burst READ Timing Parameters—BCR[8] = 0

| SYMBOL | -701 | | -708 | | -856 | | UNITS |
|---|---|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | MIN | MAX | |
| $^{t}$ACLK | | 7 | | 9 | | 11 | ns |
| $^{t}$CLK | 9.62 | | 12.5 | | 15 | | ns |

| SYMBOL | -701 | | -708 | | -856 | | UNITS |
|---|---|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | MIN | MAX | |
| $^{t}$KHTL | | 7 | | 9 | | 11 | ns |
| $^{t}$KOH | 2 | | 2 | | 2 | | ns |

## Figure 39: CE#-Controlled Asynchronous WRITE

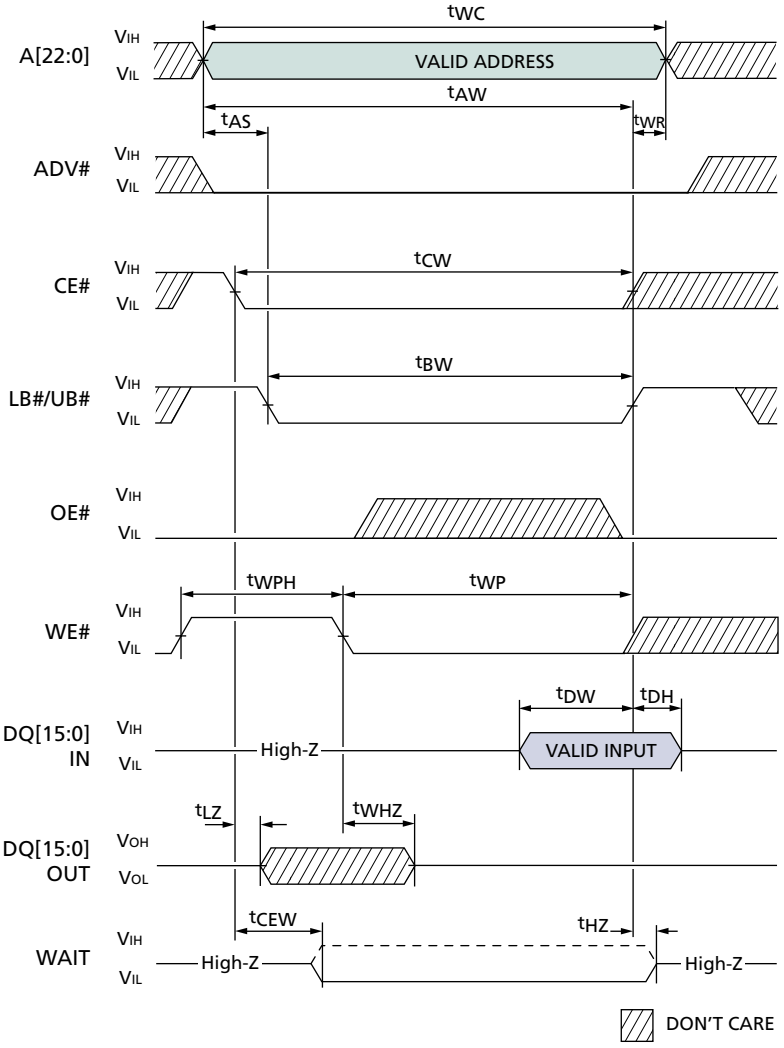



## Table 29: Asynchronous WRITE Timing Parameters—CE#-Controlled

| SYMBOL | -701/708 MIN | -701/708 MAX | -856 MIN | -856 MAX | UNITS |
|---|---|---|---|---|---|
| $t_{AS}$ | 0 | | 0 | | ns |
| $t_{AW}$ | 70 | | 85 | | ns |
| $t_{BW}$ | 70 | | 85 | | ns |
| $t_{CEW}$ | 1 | 7.5 | 1 | 7.5 | ns |
| $t_{CPH}$ | 5 | | 5 | | ns |
| $t_{CW}$ | 70 | | 85 | | ns |
| $t_{DH}$ | 0 | | 0 | | ns |
| $t_{DW}$ | 20 | | 20 | | ns |

| SYMBOL | -701/708 MIN | -701/708 MAX | -856 MIN | -856 MAX | UNITS |
|---|---|---|---|---|---|
| $t_{HZ}$ | | 8 | | 8 | ns |
| $t_{LZ}$ | 10 | | 10 | | ns |
| $t_{WC}$ | 70 | | 85 | | ns |
| $t_{WHZ}$ | | 8 | | 8 | ns |
| $t_{WP}$ | 45 | | 55 | | ns |
| $t_{WPH}$ | 10 | | 10 | | ns |
| $t_{WR}$ | 0 | | 0 | | ns |

## Figure 40: LB#/UB#-Controlled Asynchronous WRITE

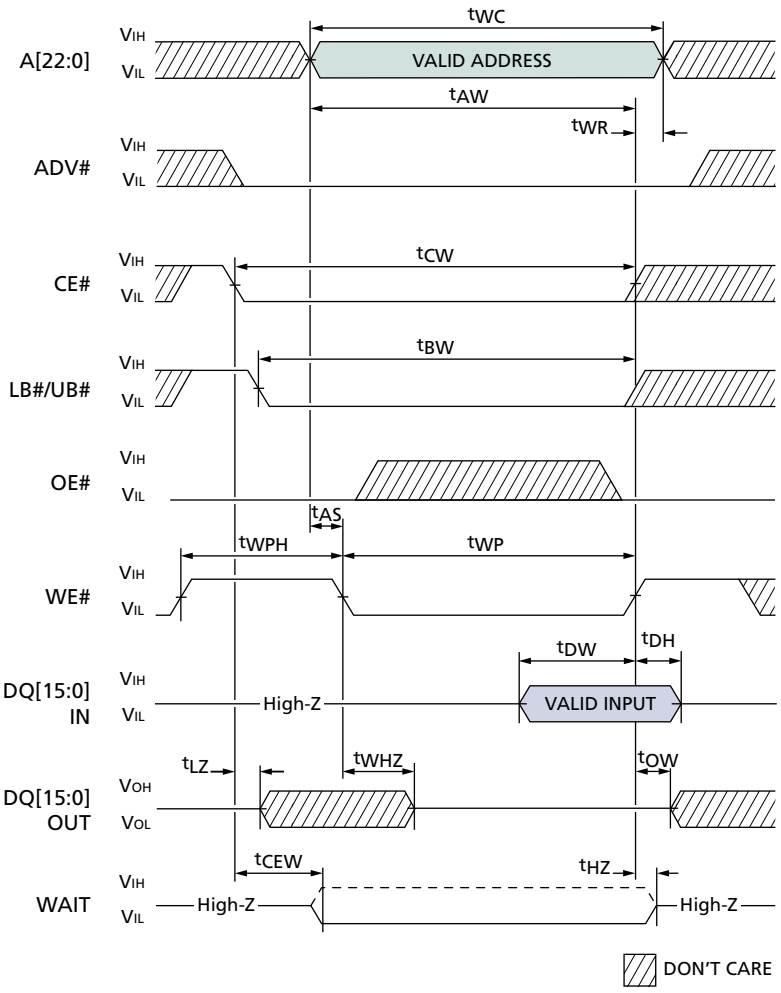



## Table 30: Asynchronous WRITE Timing Parameters—LB#/UB#-Controlled

| SYMBOL | -701/708 MIN | -701/708 MAX | -856 MIN | -856 MAX | UNITS |
|---|---|---|---|---|---|
| $t_{AS}$ | 0 | | 0 | | ns |
| $t_{AW}$ | 70 | | 85 | | ns |
| $t_{BW}$ | 70 | | 85 | | ns |
| $t_{CEW}$ | 1 | 7.5 | 1 | 7.5 | ns |
| $t_{CW}$ | 70 | | 85 | | ns |
| $t_{DH}$ | 0 | | 0 | | ns |
| $t_{DW}$ | 20 | | 20 | | ns |

| SYMBOL | -701/708 MIN | -701/708 MAX | -856 MIN | -856 MAX | UNITS |
|---|---|---|---|---|---|
| $t_{HZ}$ | | 8 | | 8 | ns |
| $t_{LZ}$ | 10 | | 10 | | ns |
| $t_{WC}$ | 70 | | 85 | | ns |
| $t_{WHZ}$ | | 8 | | 8 | ns |
| $t_{WP}$ | 45 | | 55 | | ns |
| $t_{WPH}$ | 10 | | 10 | | ns |
| $t_{WR}$ | 0 | | 0 | | ns |

## Figure 41: WE#-Controlled Asynchronous WRITE

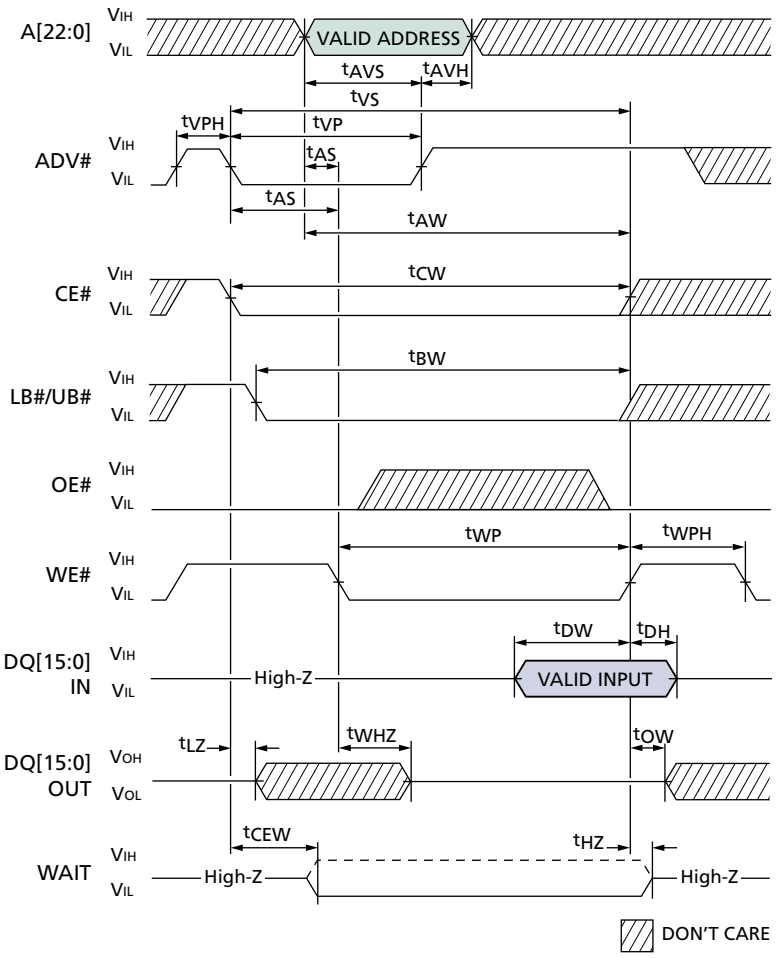



## Table 31: Asynchronous WRITE Timing Parameters—WE#-Controlled

| SYMBOL | -701/708 | | -856 | | UNITS |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| tAS | 0 | | 0 | | ns |
| tAW | 70 | | 85 | | ns |
| tBW | 70 | | 85 | | ns |
| tCEW | 1 | 7.5 | 1 | 7.5 | ns |
| tCW | 70 | | 85 | | ns |
| tDH | 0 | | 0 | | ns |
| tDW | 20 | | 20 | | ns |
| tHZ | | 8 | | 8 | ns |

| SYMBOL | -701/708 | | -856 | | UNITS |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| tLZ | 10 | | 10 | | ns |
| tOW | 5 | | 5 | | ns |
| tWC | 70 | | 85 | | ns |
| tWHZ | | 8 | | 8 | ns |
| tWP | 45 | | 55 | | ns |
| tWPH | 10 | | 10 | | ns |
| tWR | 0 | | 0 | | ns |

## Figure 42: Asynchronous WRITE Using ADV#

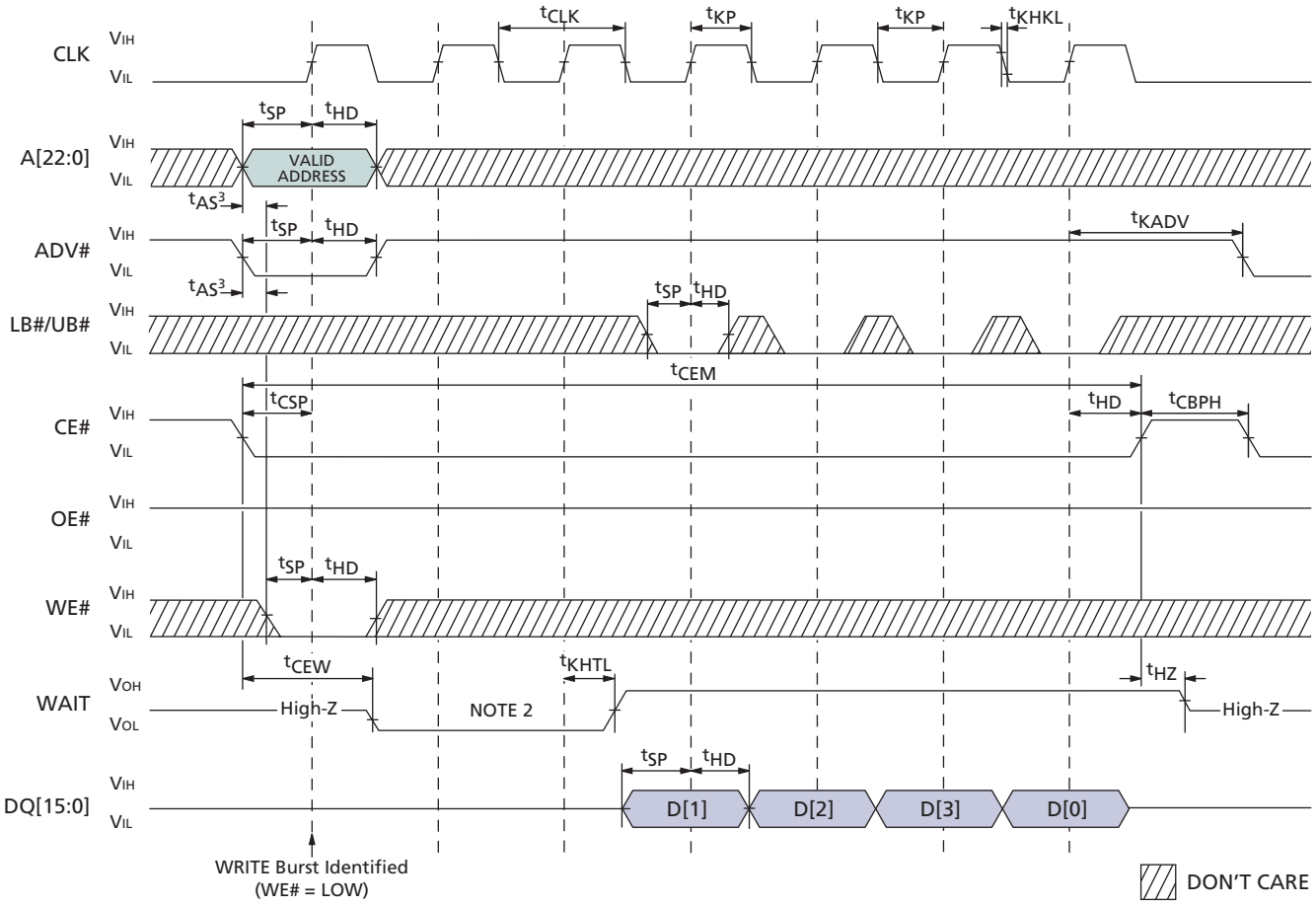



## Table 32: Asynchronous WRITE Timing Parameters Using ADV#

| SYMBOL | -701/708 MIN | -701/708 MAX | -856 MIN | -856 MAX | UNITS |
|---|---|---|---|---|---|
| $t_{AS}$ | 0 | | 0 | | ns |
| $t_{AVH}$ | 2 | | 2 | | ns |
| $t_{AVS}$ | 5 | | 5 | | ns |
| $t_{AW}$ | 70 | | 85 | | ns |
| $t_{BW}$ | 70 | | 85 | | ns |
| $t_{CEW}$ | 1 | 7.5 | 1 | 7.5 | ns |
| $t_{CW}$ | 70 | | 85 | | ns |
| $t_{DH}$ | 0 | | 0 | | ns |
| $t_{DW}$ | 20 | | 20 | | ns |

| SYMBOL | -701/708 MIN | -701/708 MAX | -856 MIN | -856 MAX | UNITS |
|---|---|---|---|---|---|
| $t_{HZ}$ | | 8 | | 8 | ns |
| $t_{LZ}$ | 10 | | 10 | | ns |
| $t_{OW}$ | 5 | | 5 | | ns |
| $t_{VP}$ | 5 | | 7 | | ns |
| $t_{VPH}$ | 10 | | 10 | | ns |
| $t_{VS}$ | 70 | | 85 | | ns |
| $t_{WHZ}$ | | 8 | | 8 | ns |
| $t_{WP}$ | 45 | | 55 | | ns |
| $t_{WPH}$ | 10 | | 10 | | ns |

## Figure 43: Burst WRITE Operation—Variable Latency Mode




NOTE:

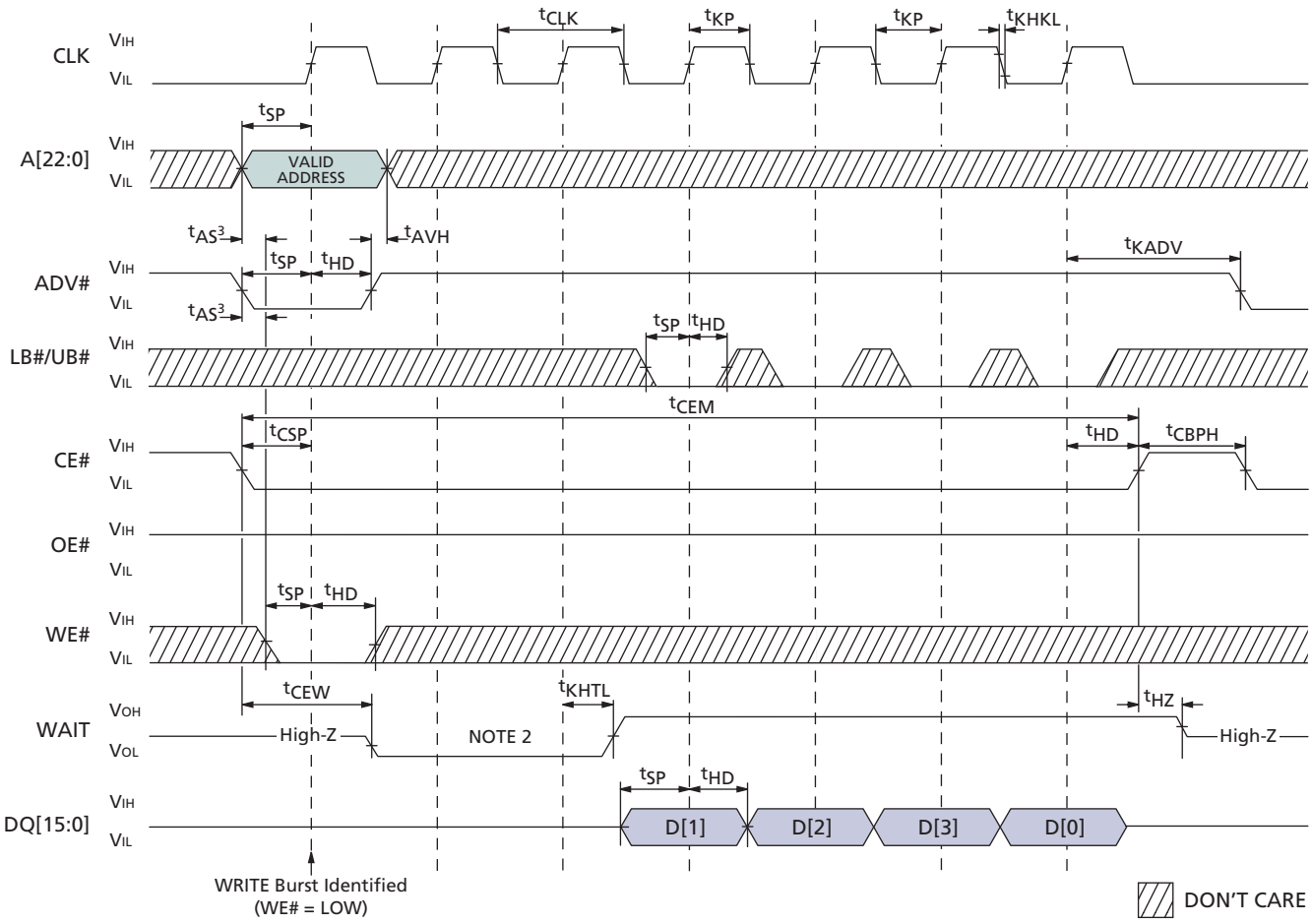
1. Non-default BCR settings for burst WRITE operation in variable latency mode: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay; burst length four; burst wrap enabled.
2. WAIT asserts for LC cycles for both fixed and variable latency. LC = Latency Code (BCR[13:11]).
3. $^{t}$AS required if $^{t}$CSP > 20ns.

## Table 33: Burst WRITE Timing Parameters

| | -701 | | -708 | | -856 | | |
|---|---|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | MIN | MAX | UNITS |
| $^{t}$AS | 0 | | 0 | | 0 | | ns |
| $^{t}$CBPH | 5 | | 6 | | 8 | | ns |
| $^{t}$CEM | | 4 | | 4 | | 4 | µs |
| $^{t}$CEW | 1 | 7.5 | 1 | 7.5 | 1 | 7.5 | ns |
| $^{t}$CLK | 9.62 | | 12.5 | | 15 | | ns |
| $^{t}$CSP | 3 | | 4 | | 5 | | ns |
| $^{t}$HD | 2 | | 2 | | 2 | | ns |

| | -701 | | -708 | | -856 | | |
|---|---|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | MIN | MAX | UNITS |
| $^{t}$HZ | | 8 | | 8 | | 8 | ns |
| $^{t}$KADV | 4 | | 6 | | 6 | | ns |
| $^{t}$KHKL | | 1.6 | | 1.8 | | 2.0 | ns |
| $^{t}$KHTL | | 7 | | 9 | | 11 | ns |
| $^{t}$KP | 3 | | 4 | | 5 | | ns |
| $^{t}$SP | 3 | | 3 | | 3 | | ns |

## Figure 44: Burst WRITE Operation—Fixed Latency Mode




NOTE:

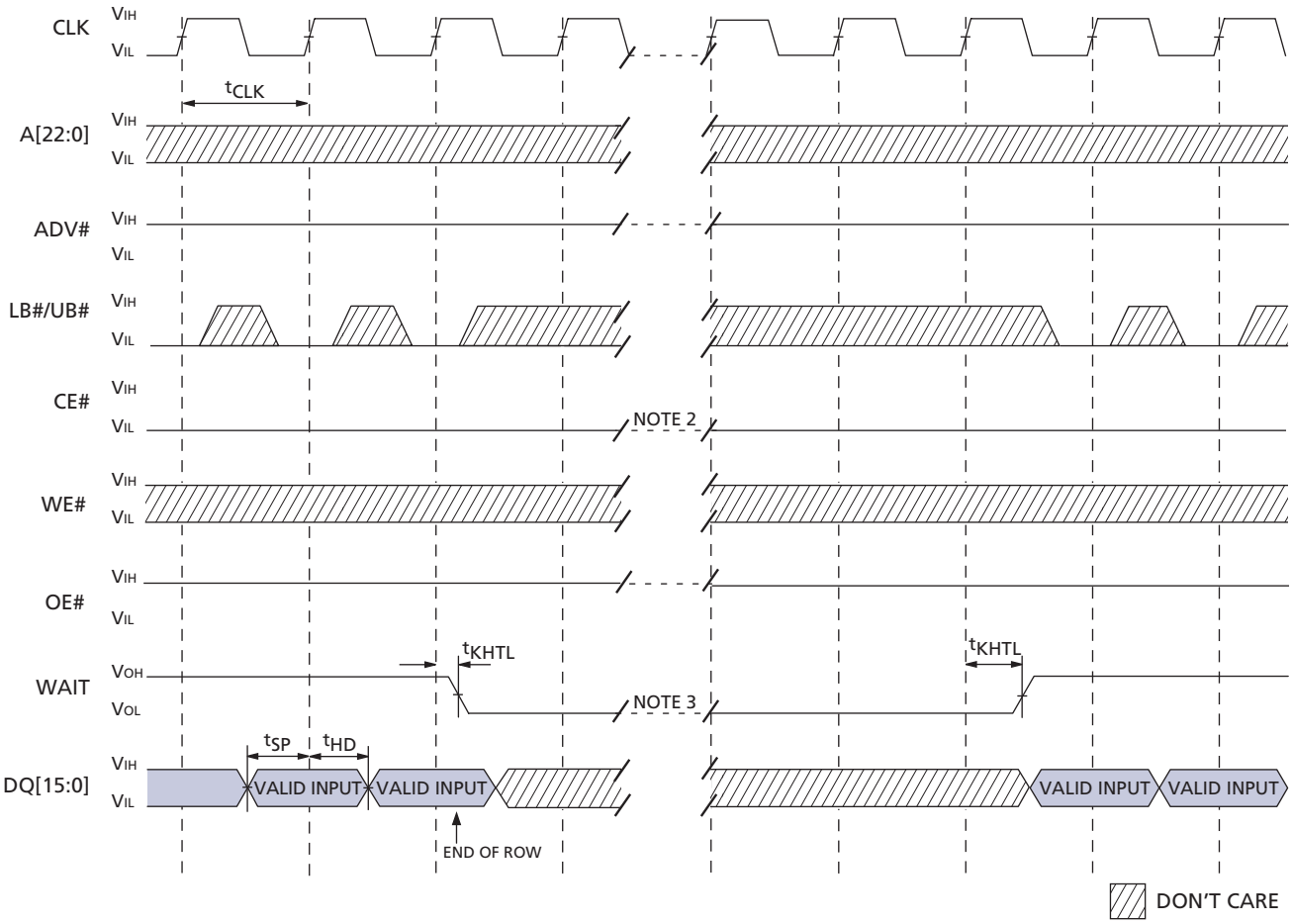
1. Non-default BCR settings for burst WRITE operation in fixed latency mode: Fixed latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay; burst length four; burst wrap enabled.
2. WAIT asserts for LC cycles for both fixed and variable latency. LC = Latency Code (BCR[13:11]).
3. $^{t}$AS required if $^{t}$CSP > 20ns.

## Table 34: Burst WRITE Timing Parameters

| SYMBOL | -701 | | -708 | | -856 | | UNITS |
|---|---|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | MIN | MAX | |
| $^{t}$AS | 0 | | 0 | | 0 | | ns |
| $^{t}$AVH | 2 | | 2 | | 2 | | ns |
| $^{t}$CBPH | 5 | | 6 | | 8 | | ns |
| $^{t}$CEM | | 4 | | 4 | | 4 | µs |
| $^{t}$CEW | 1 | 7.5 | 1 | 7.5 | 1 | 7.5 | ns |
| $^{t}$CLK | 9.62 | | 12.5 | | 15 | | ns |
| $^{t}$CSP | 3 | | 4 | | 5 | | ns |

| SYMBOL | -701 | | -708 | | -856 | | UNITS |
|---|---|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | MIN | MAX | |
| $^{t}$HD | 2 | | 2 | | 2 | | ns |
| $^{t}$HZ | | 8 | | 8 | | 8 | ns |
| $^{t}$KADV | 4 | | 6 | | 6 | | ns |
| $^{t}$KHKL | | 1.6 | | 1.8 | | 2.0 | ns |
| $^{t}$KHTL | | 7 | | 9 | | 11 | ns |
| $^{t}$KP | 3 | | 4 | | 5 | | ns |
| $^{t}$SP | 3 | | 3 | | 3 | | ns |

## Figure 45: Continuous Burst WRITE Showing an Output Delay with BCR[8] = 0 for Variable Latency End-of-Row Condition




NOTE:

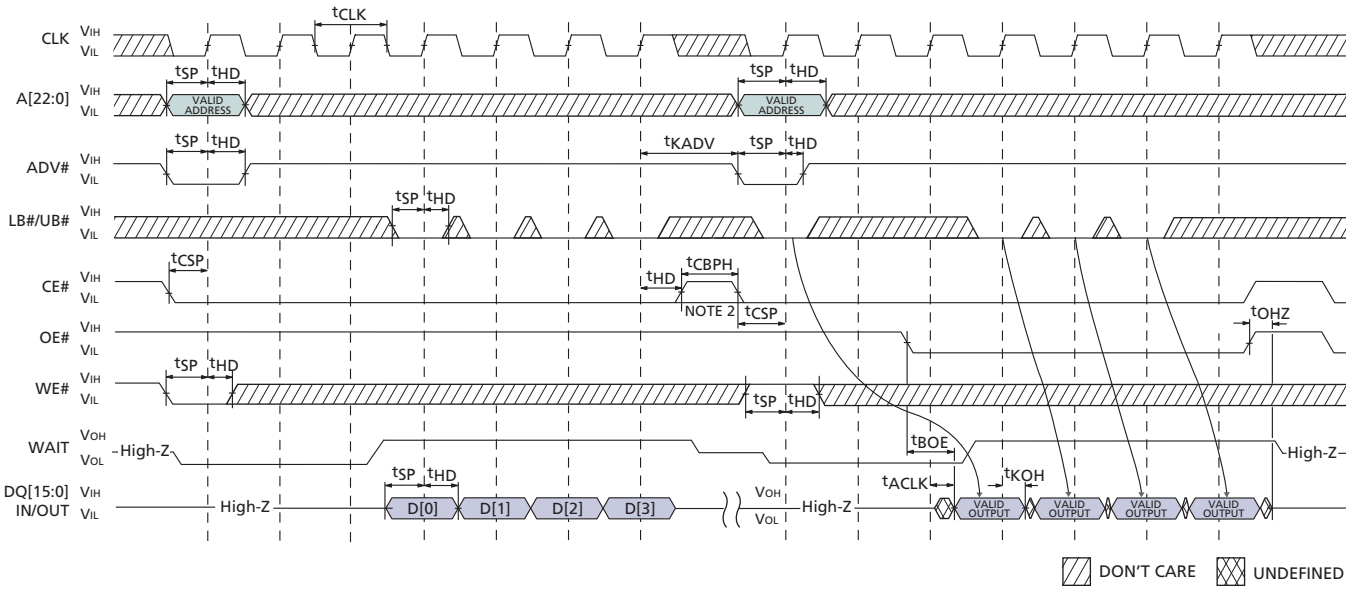
1. Non-default BCR settings for continuous burst WRITE, BCR[8] = 0: WAIT active LOW; WAIT asserted during delay. Do not cross row boundaries with fixed latency.
2. CE# must not remain LOW longer than $^{t}$CEM.
3. WAIT asserts for anywhere from LC to 2LC cycles. LC = Latency Code (BCR[13:11]).

## Table 35: Burst WRITE Timing Parameters—BCR[8] = 0

| SYMBOL | -701 | | -708 | | -856 | | UNITS |
|---|---|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | MIN | MAX | |
| $^{t}$CLK | 9.62 | | 12.5 | | 15 | | ns |
| $^{t}$HD | 2 | | 2 | | 2 | | ns |

| SYMBOL | -701 | | -708 | | -856 | | UNITS |
|---|---|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | MIN | MAX | |
| $^{t}$KHTL | | 7 | | 8 | | 11 | ns |
| $^{t}$SP | 3 | | 3 | | 3 | | ns |

## Figure 46: Burst WRITE Followed by Burst READ




NOTE:

1. Non-default BCR settings for burst WRITE followed by burst READ: Fixed or variable latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. A refresh opportunity must be provided every $^{t}$CEM. A refresh opportunity is satisfied by either of the following two conditions: a) clocked CE# HIGH, or b) CE# HIGH for longer than 15ns. CE# can stay LOW between burst READ and burst WRITE operations, but CE# must not remain LOW longer than $^{t}$CEM.

## Table 36: WRITE Timing Parameters—Burst WRITE Followed by Burst READ

| | -701 | | -708 | | -856 | | |
|---|---|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | MIN | MAX | UNITS |
| $^{t}$CBPH | 5 | | 6 | | 8 | | ns |
| $^{t}$CLK | 9.62 | 20 | 12.5 | 20 | 15 | 20 | ns |
| $^{t}$CSP | 3 | 20 | 4 | 20 | 5 | 20 | ns |

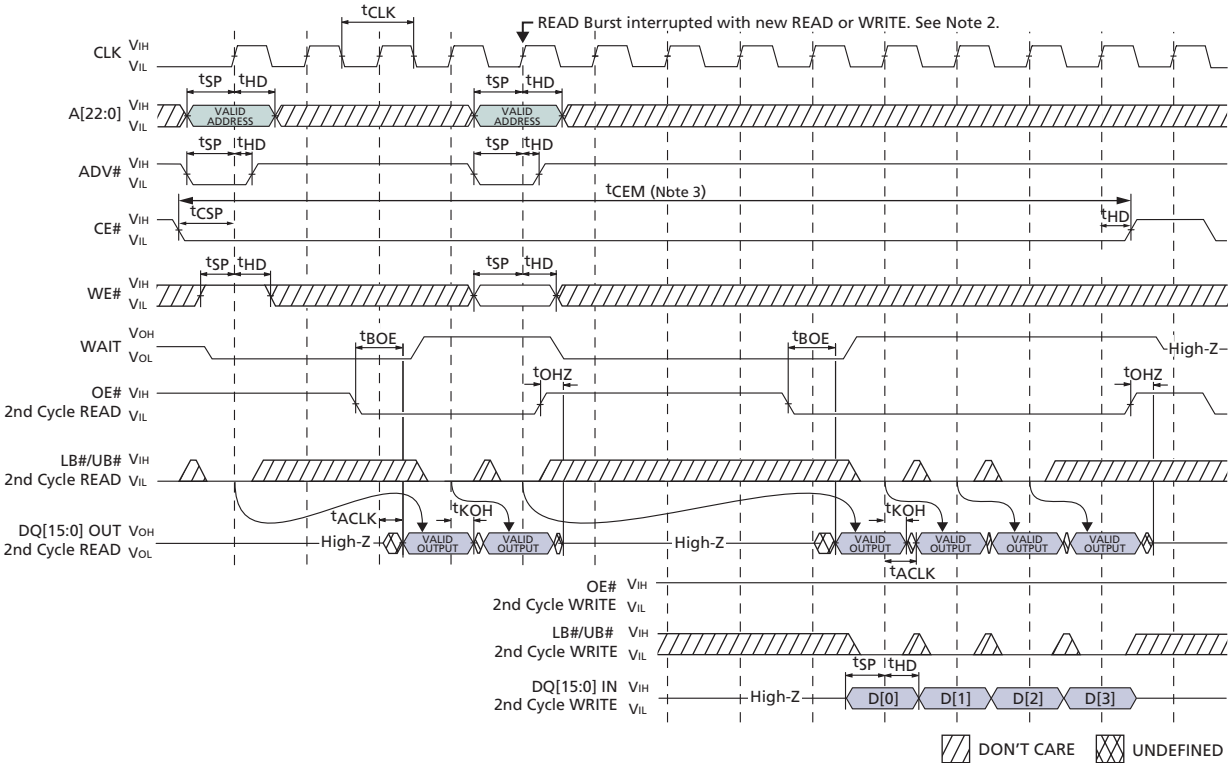
| | -701 | | -708 | | -856 | | |
|---|---|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | MIN | MAX | UNITS |
| $^{t}$HD | 2 | | 2 | | 2 | | ns |
| $^{t}$KADV | 4 | | 6 | | 6 | | ns |
| $^{t}$SP | 3 | | 3 | | 3 | | ns |

## Table 37: READ Timing Parameters—Burst WRITE Followed by Burst READ

| | -701 | | -708 | | -856 | | |
|---|---|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | MIN | MAX | UNITS |
| $^{t}$ACLK | | 7 | | 9 | | 11 | ns |
| $^{t}$BOE | | 20 | | 20 | | 20 | ns |
| $^{t}$CLK | 9.62 | | 12.5 | | 15 | | ns |
| $^{t}$CSP | 3 | | 4 | | 5 | | ns |

| | -701 | | -708 | | -856 | | |
|---|---|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | MIN | MAX | UNITS |
| $^{t}$HD | 2 | | 2 | | 2 | | ns |
| $^{t}$KOH | 2 | | 2 | | 2 | | ns |
| $^{t}$OHZ | | 8 | | 8 | | 8 | ns |
| $^{t}$SP | 3 | | 3 | | 3 | | ns |

## Figure 47: Burst READ Interrupted by Burst READ or WRITE




NOTE:

1. Non-default BCR settings for burst READ interrupted by burst READ or WRITE: Fixed or variable latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay. All bursts shown for variable latency; no refresh collision.
2. Burst interrupt shown on first allowable clock (i.e., after the first data received by controller).
3. CE# can stay LOW between burst operations, but CE# must not remain LOW longer than $^{t}$CEM.

## Table 38: READ Timing Parameters—Burst WRITE Interrupted

| SYMBOL | -701 MIN | -701 MAX | -708 MIN | -708 MAX | -856 MIN | -856 MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $^{t}$ACLK | | 7 | | 9 | | 11 | ns |
| $^{t}$BOE | | 20 | | 20 | | 20 | ns |
| $^{t}$CLK | 9.62 | | 12.5 | | 15 | | ns |
| $^{t}$CSP | 3 | | 4 | | 5 | | ns |

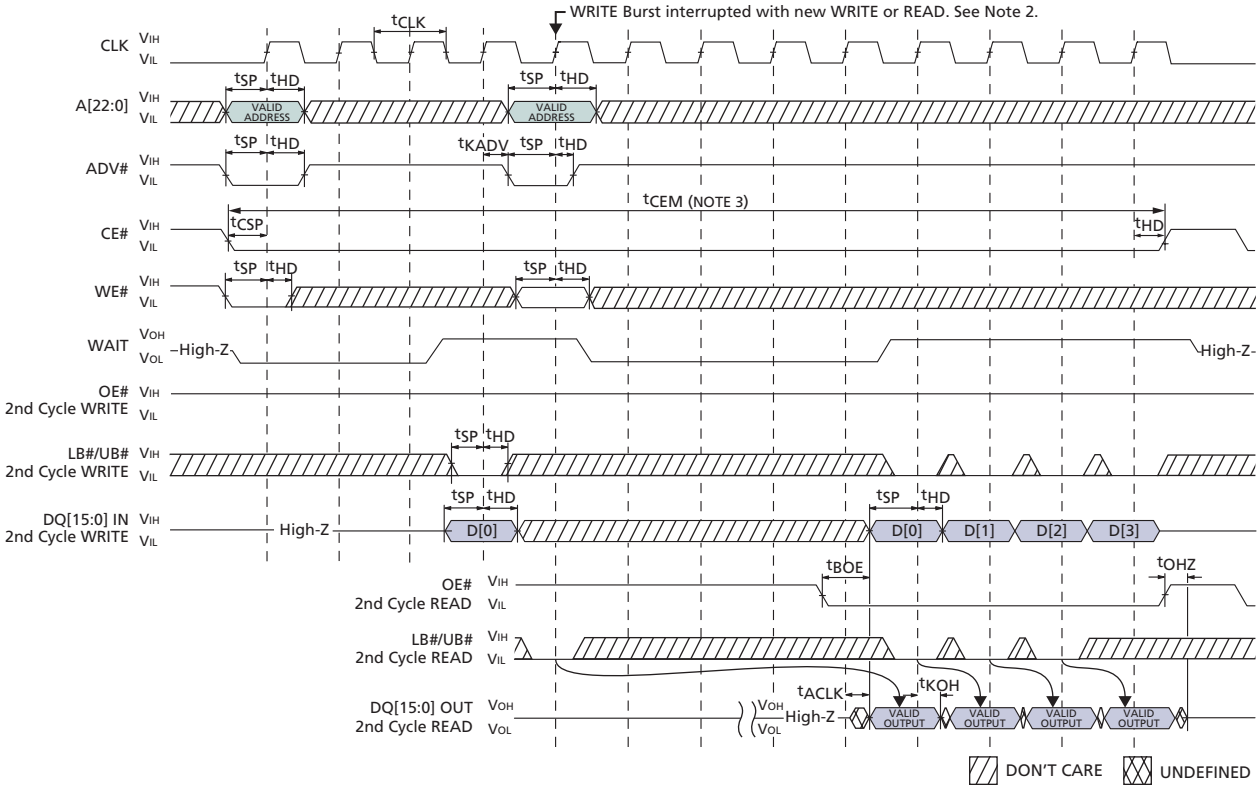
| SYMBOL | -701 MIN | -701 MAX | -708 MIN | -708 MAX | -856 MIN | -856 MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $^{t}$HD | 2 | | 2 | | 2 | | ns |
| $^{t}$KOH | 2 | | 2 | | 2 | | ns |
| $^{t}$OHZ | | 8 | | 8 | | 8 | ns |
| $^{t}$SP | 3 | | 3 | | 3 | | ns |

## Table 39: WRITE Timing Parameters—Burst WRITE Interrupted

| SYMBOL | -701 MIN | -701 MAX | -708 MIN | -708 MAX | -856 MIN | -856 MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $^{t}$CLK | 9.62 | 20 | 12.5 | 20 | 15 | 20 | ns |
| $^{t}$CSP | 3 | 20 | 4 | 20 | 5 | 20 | ns |

| SYMBOL | -701 MIN | -701 MAX | -708 MIN | -708 MAX | -856 MIN | -856 MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $^{t}$HD | 2 | | 2 | | 2 | | ns |
| $^{t}$SP | 3 | | 3 | | 3 | | ns |

## Figure 48: Burst WRITE Interrupted by Burst WRITE or READ—Variable Latency Mode




NOTE:

1. Non-default BCR settings for burst WRITE interrupted by burst WRITE or READ in variable latency mode: Fixed or variable latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay. All bursts shown for variable latency; no refresh collision.
2. Burst interrupt shown on first allowable clock (i.e., after first data word written).
3. CE# can stay LOW between burst operations, but CE# must not remain LOW longer than $^{t}$CEM.

## Table 40: WRITE Timing Parameters—Burst READ Interrupted

| SYMBOL | -701 | | -708 | | -856 | | UNITS |
|---|---|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | MIN | MAX | |
| $^{t}$CLK | 9.62 | 20 | 12.5 | 20 | 15 | 20 | ns |
| $^{t}$CSP | 3 | 20 | 4 | 20 | 5 | 20 | ns |
| $^{t}$HD | 2 | | 2 | | 2 | | ns |

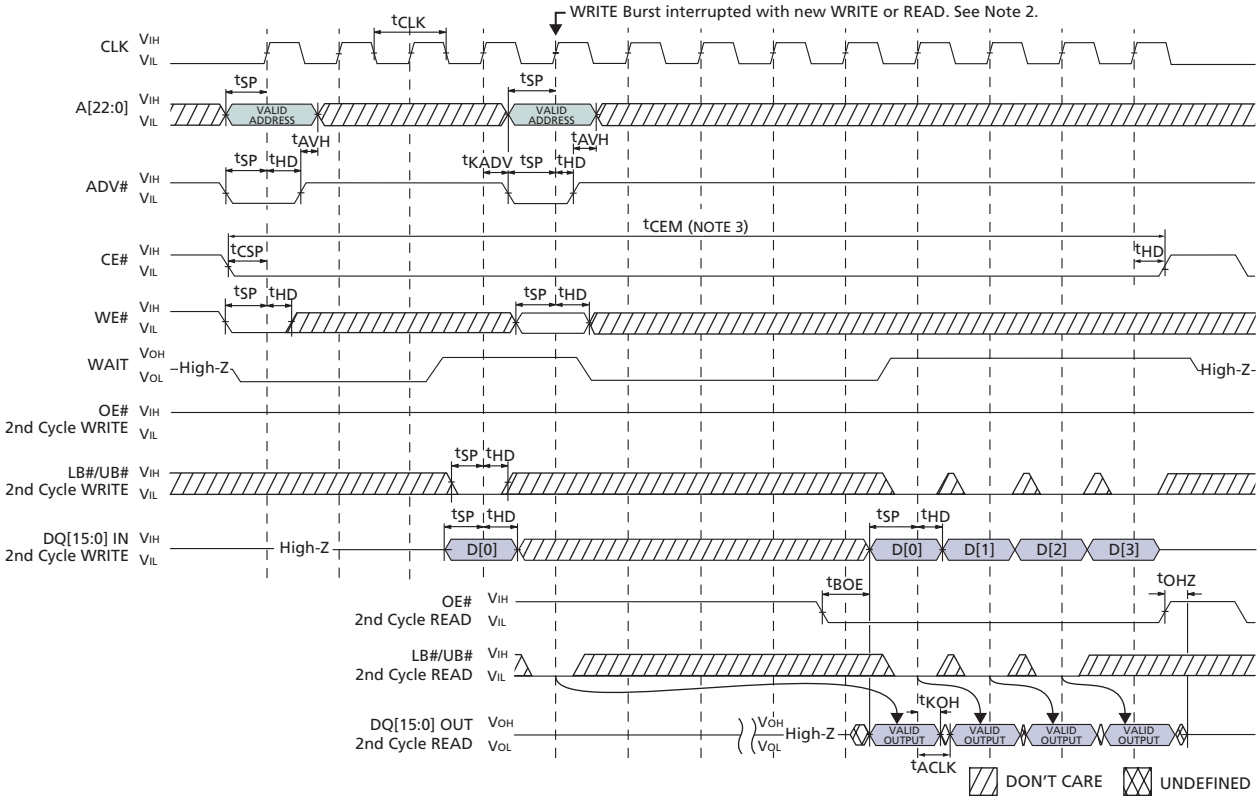
| SYMBOL | -701 | | -708 | | -856 | | UNITS |
|---|---|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | MIN | MAX | |
| $^{t}$KADV | 4 | | 6 | | 6 | | ns |
| $^{t}$SP | 3 | | 3 | | 3 | | ns |

## Table 41: READ Timing Parameters—Burst READ Interrupted

| SYMBOL | -701 | | -708 | | -856 | | UNITS |
|---|---|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | MIN | MAX | |
| $^{t}$ACLK | | 7 | | 9 | | 11 | ns |
| $^{t}$BOE | | 20 | | 20 | | 20 | ns |
| $^{t}$CLK | 9.62 | | 12.5 | | 15 | | ns |
| $^{t}$CSP | 3 | | 4 | | 5 | | ns |

| SYMBOL | -701 | | -708 | | -856 | | UNITS |
|---|---|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | MIN | MAX | |
| $^{t}$HD | 2 | | 2 | | 2 | | ns |
| $^{t}$KOH | 2 | | 2 | | 2 | | ns |
| $^{t}$OHZ | | 8 | | 8 | | 8 | ns |
| $^{t}$SP | 3 | | 3 | | 3 | | ns |

## Figure 49: Burst WRITE Interrupted by Burst WRITE or READ—Fixed Latency Mode




NOTE:

1. Non-default BCR settings for burst WRITE interrupted by burst WRITE or READ in fixed latency mode: Fixed latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. Burst interrupt shown on first allowable clock (i.e., after first data word written).
3. CE# can stay LOW between burst operations, but CE# must not remain LOW longer than $^{t}$CEM.

## Table 42: WRITE Timing Parameters—Burst READ Interrupted

| | -701 | | -708 | | -856 | | |
|---|---|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | MIN | MAX | UNITS |
| $^{t}$AVH | 2 | | 2 | | 2 | | ns |
| $^{t}$CLK | 9.62 | 20 | 12.5 | 20 | 15 | 20 | ns |
| $^{t}$CSP | 3 | 20 | 4 | 20 | 5 | 20 | ns |

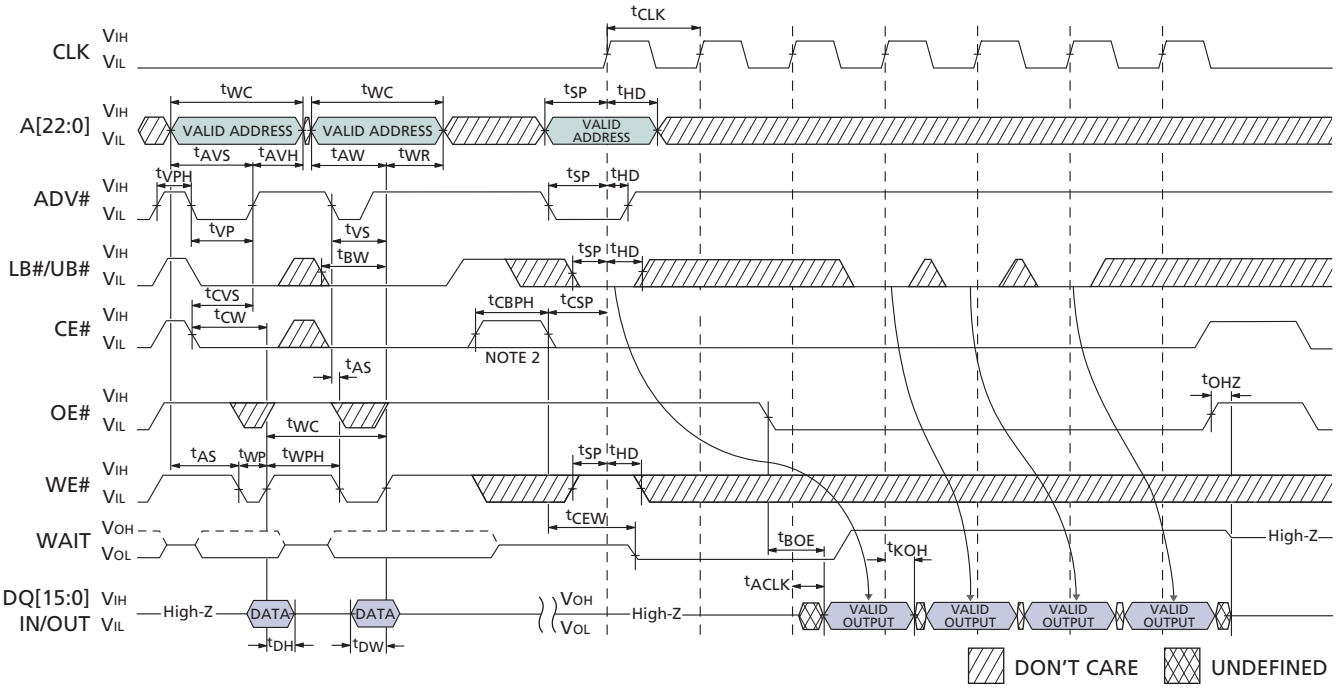
| | -701 | | -708 | | -856 | | |
|---|---|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | MIN | MAX | UNITS |
| $^{t}$HD | 2 | | 2 | | 2 | | ns |
| $^{t}$KADV | 4 | | 6 | | 6 | | ns |
| $^{t}$SP | 3 | | 3 | | 3 | | ns |

## Table 43: READ Timing Parameters—Burst READ Interrupted

| | -701 | | -708 | | -856 | | |
|---|---|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | MIN | MAX | UNITS |
| $^{t}$ACLK | | 7 | | 9 | | 11 | ns |
| $^{t}$BOE | | 20 | | 20 | | 20 | ns |
| $^{t}$CLK | 9.62 | | 12.5 | | 15 | | ns |
| $^{t}$CSP | 3 | | 4 | | 5 | | ns |

| | -701 | | -708 | | -856 | | |
|---|---|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | MIN | MAX | UNITS |
| $^{t}$HD | 2 | | 2 | | 2 | | ns |
| $^{t}$KOH | 2 | | 2 | | 2 | | ns |
| $^{t}$OHZ | | 8 | | 8 | | 8 | ns |
| $^{t}$SP | 3 | | 3 | | 3 | | ns |

## Figure 50: Asynchronous WRITE Followed by Burst READ




NOTE:

1. Non-default BCR settings for asynchronous WRITE followed by burst READ: Fixed or variable latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. When transitioning between asynchronous and variable-latency burst operations, CE# must go HIGH. CE# can stay LOW when transitioning to fixed-latency burst READs. A refresh opportunity must be provided every $^{t}$CEM. A refresh opportunity is satisfied by either of the following two conditions: a) clocked CE# HIGH, or b) CE# HIGH for longer than 15ns.

## Table 44: WRITE Timing Parameters—Async WRITE Followed by Burst READ

| | -701/708 | | -856 | | |
|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | UNITS |
| $^{t}$AVH | 2 | | 2 | | ns |
| $^{t}$AS | 0 | | 0 | | ns |
| $^{t}$AVS | 5 | | 5 | | ns |
| $^{t}$AW | 70 | | 85 | | ns |
| $^{t}$BW | 70 | | 85 | | ns |
| $^{t}$CVS | 7 | | 7 | | ns |
| $^{t}$CW | 70 | | 85 | | ns |
| $^{t}$DH | 0 | | 0 | | ns |

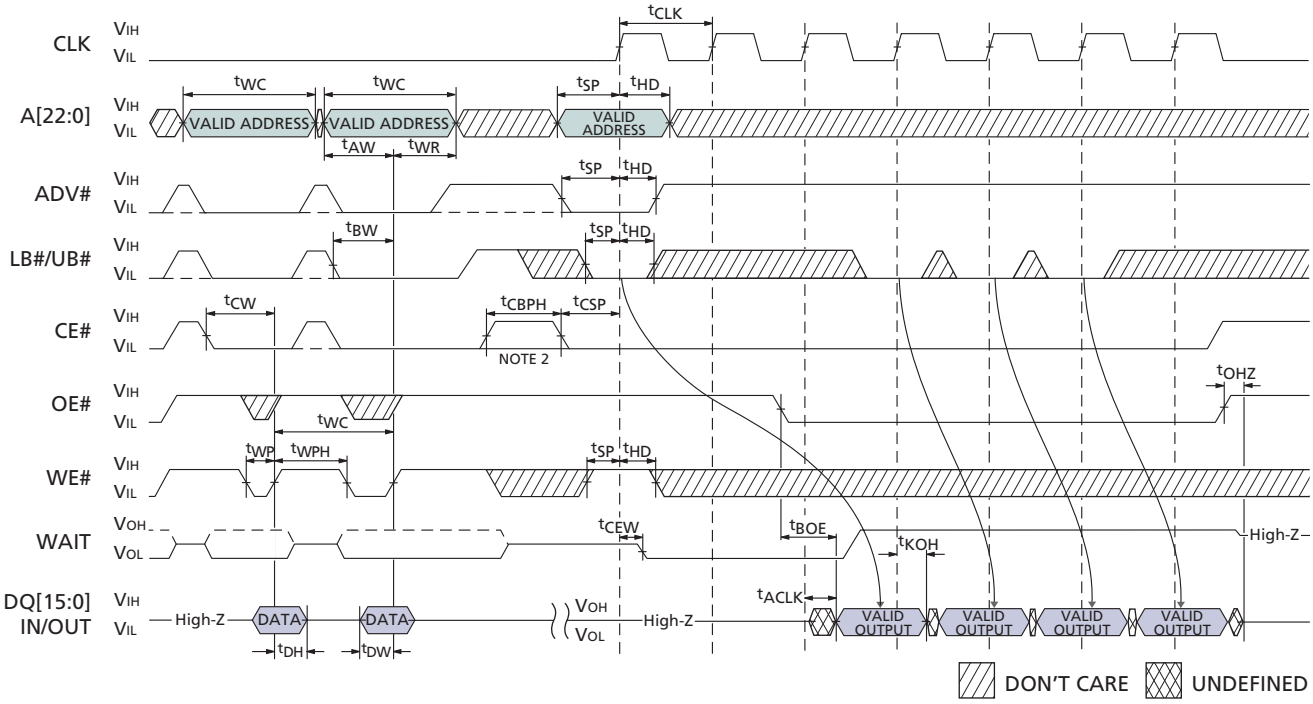
| | -701/708 | | -856 | | |
|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | UNITS |
| $^{t}$DW | 20 | | 20 | | ns |
| $^{t}$VP | 5 | | 7 | | ns |
| $^{t}$VPH | 10 | | 10 | | ns |
| $^{t}$VS | 70 | | 85 | | ns |
| $^{t}$WC | 70 | | 85 | | ns |
| $^{t}$WP | 45 | | 55 | | ns |
| $^{t}$WPH | 10 | | 10 | | ns |
| $^{t}$WR | 0 | | 0 | | ns |

## Table 45: READ Timing Parameters—Async WRITE Followed by Burst READ

| | -701 | | -708 | | -856 | | |
|---|---|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | MIN | MAX | UNITS |
| $^{t}$ACLK | | 7 | | 9 | | 11 | ns |
| $^{t}$BOE | | 20 | | 20 | | 20 | ns |
| $^{t}$CBPH | 5 | | 6 | | 8 | | ns |
| $^{t}$CEW | 1 | 7.5 | 1 | 7.5 | 1 | 7.5 | ns |
| $^{t}$CLK | 9.62 | | 12.5 | | 15 | | ns |

| | -701 | | -708 | | -856 | | |
|---|---|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | MIN | MAX | UNITS |
| $^{t}$CSP | 3 | | 4 | | 5 | | ns |
| $^{t}$HD | 2 | | 2 | | 2 | | ns |
| $^{t}$KOH | 2 | | 2 | | 2 | | ns |
| $^{t}$OHZ | | 8 | | 8 | | 8 | ns |
| $^{t}$SP | 3 | | 3 | | 3 | | ns |

## Figure 51: Asynchronous WRITE (ADV# LOW) Followed By Burst READ




NOTE:

1. Non-default BCR settings for asynchronous WRITE, with ADV# LOW, followed by burst READ: Fixed or variable latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. When transitioning between asynchronous and variable-latency burst operations, CE# must go HIGH. CE# can stay LOW when transitioning to fixed-latency burst READs. A refresh opportunity must be provided every $^{t}$CEM. A refresh opportunity is satisfied by either of the following two conditions: a) clocked CE# HIGH, or b) CE# HIGH for longer than 15ns.

## Table 46: Asynchronous WRITE Timing Parameters—ADV# LOW

| SYMBOL | -701/708 | | -856 | | UNITS |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| $^{t}$AW | 70 | | 85 | | ns |
| $^{t}$BW | 70 | | 85 | | ns |
| $^{t}$CW | 70 | | 85 | | ns |
| $^{t}$DH | 0 | | 0 | | ns |
| $^{t}$DW | 20 | | 20 | | ns |

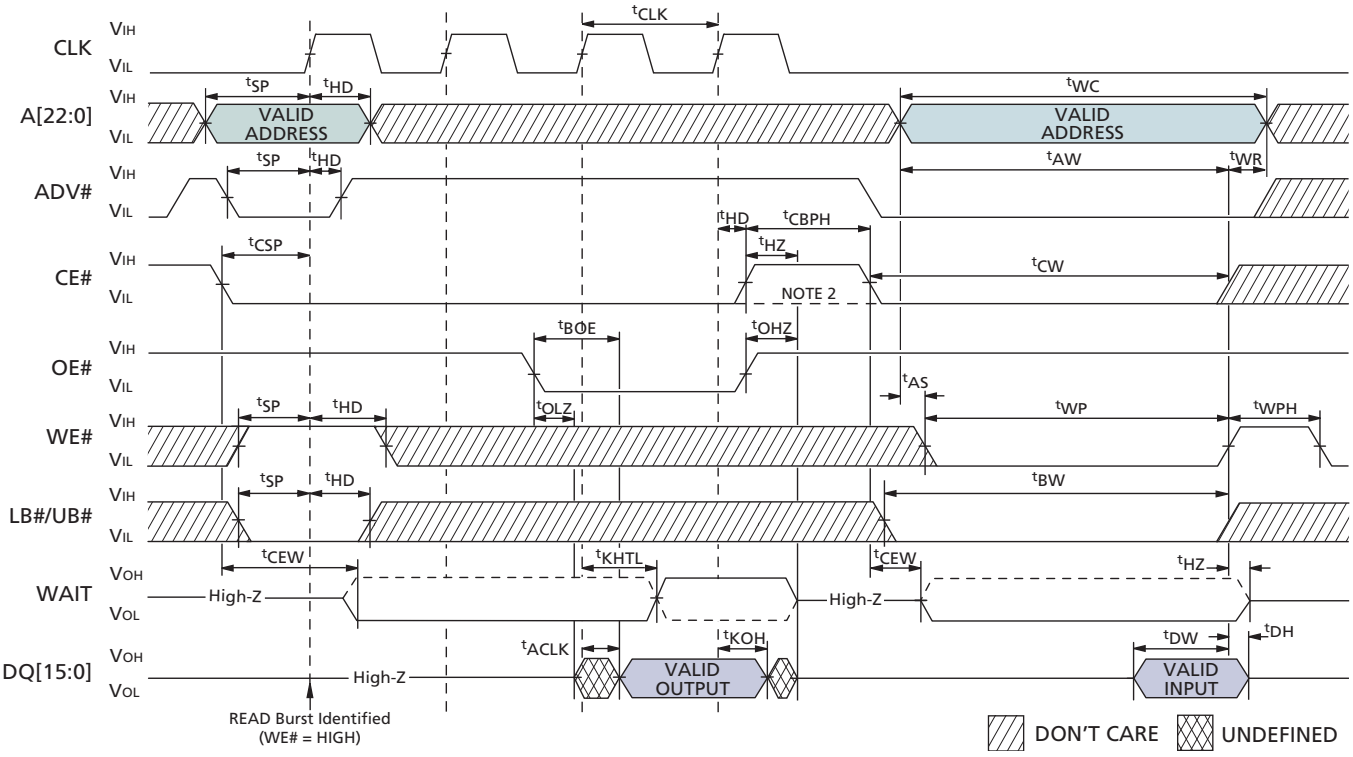
| SYMBOL | -701/708 | | -856 | | UNITS |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| $^{t}$WC | 70 | | 85 | | ns |
| $^{t}$WP | 45 | | 55 | | ns |
| $^{t}$WPH | 10 | | 10 | | ns |
| $^{t}$WR | 0 | | 0 | | ns |

## Table 47: Burst READ Timing Parameters

| SYMBOL | -701 | | -708 | | -856 | | UNITS |
|---|---|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | MIN | MAX | |
| $^{t}$ACLK | | 7 | | 9 | | 11 | ns |
| $^{t}$BOE | | 20 | | 20 | | 20 | ns |
| $^{t}$CBPH | 5 | | 6 | | 8 | | ns |
| $^{t}$CEW | 1 | 7.5 | 1 | 7.5 | 1 | 7.5 | ns |
| $^{t}$CLK | 9.62 | | 12.5 | | 15 | | ns |

| SYMBOL | -701 | | -708 | | -856 | | UNITS |
|---|---|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | MIN | MAX | |
| $^{t}$CSP | 3 | | 4 | | 5 | | ns |
| $^{t}$HD | 2 | | 2 | | 2 | | ns |
| $^{t}$KOH | 2 | | 2 | | 2 | | ns |
| $^{t}$OHZ | | 8 | | 8 | | 8 | ns |
| $^{t}$SP | 3 | | 3 | | 3 | | ns |

## Figure 52: Burst READ Followed by Asynchronous WRITE (WE#-Controlled)




NOTE:

1. Non-default BCR settings for burst READ followed by asynchronous WE#-controlled WRITE: Fixed or variable latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. When transitioning between asynchronous and variable-latency burst operations, CE# must go HIGH. CE# can stay LOW when transitioning from fixed-latency burst READs. A refresh opportunity must be provided every $^{t}$CEM. A refresh opportunity is satisfied by either of the following two conditions: a) clocked CE# HIGH, or b) CE# HIGH for longer than 15ns.

## Table 48: Burst READ Timing Parameters

| | -701 | | -708 | | -856 | | |
|---|---|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | MIN | MAX | UNITS |
| $^{t}$ACLK | | 7 | | 9 | | 11 | ns |
| $^{t}$BOE | | 20 | | 20 | | 20 | ns |
| $^{t}$CBPH | 5 | | 6 | | 8 | | ns |
| $^{t}$CEW | 1 | 7.5 | 1 | 7.5 | 1 | 7.5 | ns |
| $^{t}$CLK | 9.62 | | 12.5 | | 15 | | ns |
| $^{t}$CSP | 3 | | 4 | | 5 | | ns |

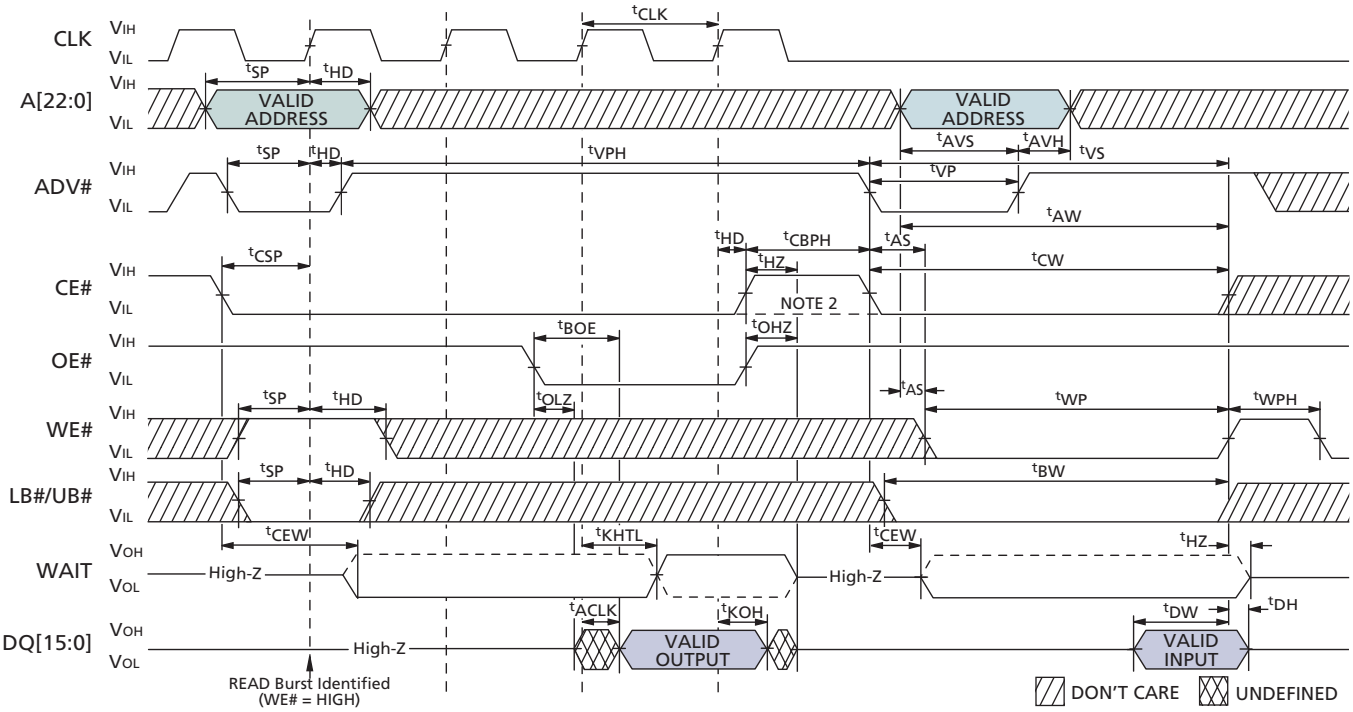
| | -701 | | -708 | | -856 | | |
|---|---|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | MIN | MAX | UNITS |
| $^{t}$HD | 2 | | 2 | | 2 | | ns |
| $^{t}$HZ | | 8 | | 8 | | 8 | ns |
| $^{t}$KHTL | | 7 | | 9 | | 11 | ns |
| $^{t}$KOH | 2 | | 2 | | 2 | | ns |
| $^{t}$OHZ | | 8 | | 8 | | 8 | ns |
| $^{t}$SP | 3 | | 3 | | 3 | | ns |

## Table 49: Asynchronous WRITE Timing Parameters—WE# Controlled

| | -701/-708 | | -856 | | |
|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | UNITS |
| $^{t}$AS | 0 | | | 0 | ns |
| $^{t}$AW | 70 | | 85 | | ns |
| $^{t}$BW | 70 | | 85 | | ns |
| $^{t}$CW | 70 | | 85 | | ns |
| $^{t}$DH | 0 | | 0 | | ns |
| $^{t}$DW | 20 | | 20 | | ns |

| | -701/-708 | | -856 | | |
|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | UNITS |
| $^{t}$HZ | | 8 | | 8 | ns |
| $^{t}$WC | 70 | | 85 | | ns |
| $^{t}$WP | 45 | | 55 | | ns |
| $^{t}$WPH | 10 | | 10 | | ns |
| $^{t}$WR | 0 | | 0 | | ns |

## Figure 53: Burst READ Followed by Asynchronous WRITE Using ADV#




NOTE:

1. Non-default BCR settings for burst READ followed by asynchronous WRITE using ADV#: Fixed or variable latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. When transitioning between asynchronous and variable-latency burst operations, CE# must go HIGH. CE# can stay LOW when transitioning from fixed-latency burst READs. A refresh opportunity must be provided every $^{t}$CEM. A refresh opportunity is satisfied by either of the following two conditions: a) clocked CE# HIGH, or b) CE# HIGH for longer than 15ns.

## Table 50: Burst READ Timing Parameters

| SYMBOL | -701 MIN | -701 MAX | -708 MIN | -708 MAX | -856 MIN | -856 MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $^{t}$ACLK | | 7 | | 9 | | 11 | ns |
| $^{t}$BOE | | 20 | | 20 | | 20 | ns |
| $^{t}$CBPH | 5 | | 6 | | 8 | | ns |
| $^{t}$CEW | 1 | 7.5 | 1 | 7.5 | 1 | 7.5 | ns |
| $^{t}$CLK | 9.62 | | 12.5 | | 15 | | ns |
| $^{t}$CSP | 3 | | 4 | | 5 | | ns |

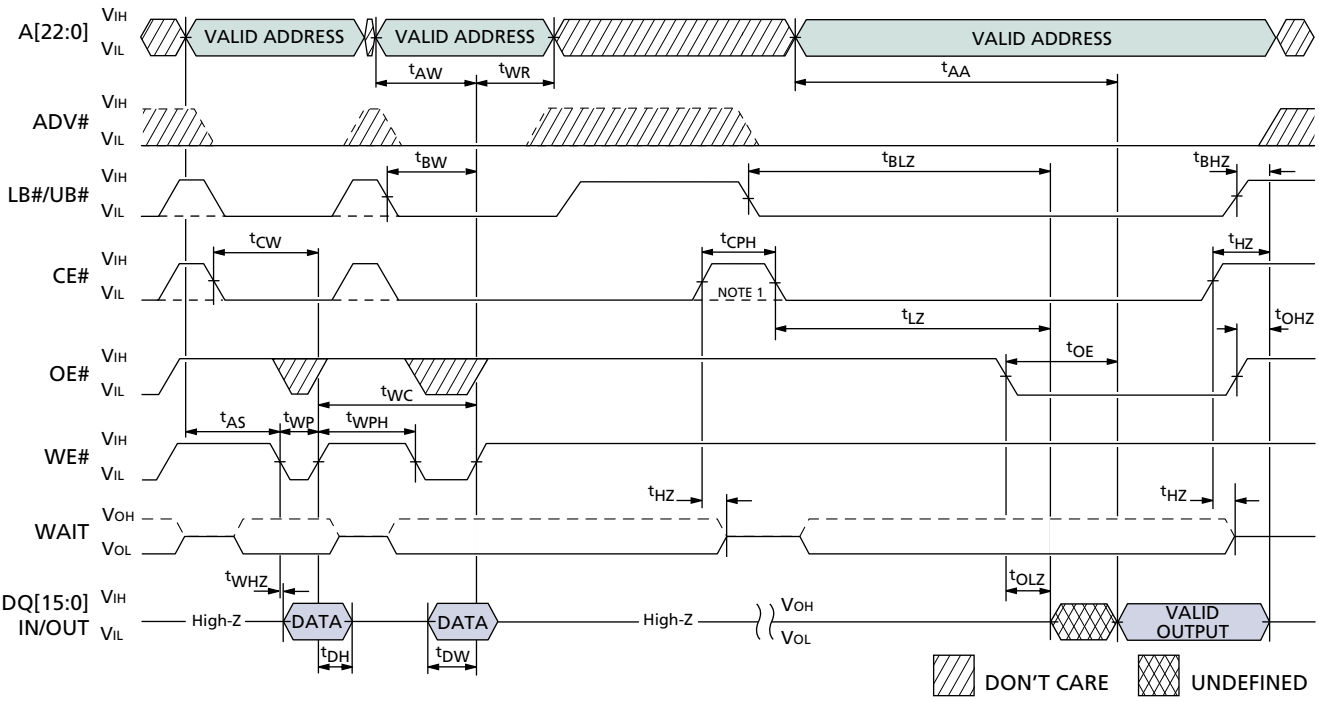
| SYMBOL | -701 MIN | -701 MAX | -708 MIN | -708 MAX | -856 MIN | -856 MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $^{t}$HD | 2 | | 2 | | 2 | | ns |
| $^{t}$HZ | | 8 | | 8 | | 8 | ns |
| $^{t}$KHTL | | 7 | | 9 | | 11 | ns |
| $^{t}$KOH | 2 | | 2 | | 2 | | ns |
| $^{t}$OHZ | | 8 | | 8 | | 8 | ns |
| $^{t}$SP | 3 | | 3 | | 3 | | ns |

## Table 51: Asynchronous WRITE Timing Parameters Using ADV#

| SYMBOL | -701/-708 MIN | -701/-708 MAX | -856 MIN | -856 MAX | UNITS |
|---|---|---|---|---|---|
| $^{t}$AS | 0 | | 0 | | ns |
| $^{t}$AVH | 2 | | 2 | | ns |
| $^{t}$AVS | 5 | | 5 | | ns |
| $^{t}$AW | 70 | | 85 | | ns |
| $^{t}$BW | 70 | | 85 | | ns |
| $^{t}$CEW | 1 | 7.5 | 1 | 7.5 | ns |
| $^{t}$CW | 70 | | 85 | | ns |
| $^{t}$DH | 0 | | 0 | | ns |

| SYMBOL | -701/-708 MIN | -701/-708 MAX | -856 MIN | -856 MAX | UNITS |
|---|---|---|---|---|---|
| $^{t}$DW | 20 | | 20 | | ns |
| $^{t}$HZ | | 8 | | 8 | ns |
| $^{t}$VP | 5 | | 7 | | ns |
| $^{t}$VPH | 10 | | 10 | | ns |
| $^{t}$VS | 70 | | 85 | | ns |
| $^{t}$WP | 45 | | 55 | | ns |
| $^{t}$WPH | 10 | | 10 | | ns |

## Figure 54: Asynchronous WRITE Followed by Asynchronous READ—ADV# LOW




NOTE:

1. When configured for synchronous mode (BCR[15] = 0), CE# must remain HIGH for at least 5ns ($^{t}$CPH) to schedule the appropriate refresh interval. Otherwise, $^{t}$CPH is only required after CE#-controlled WRITEs.

## Table 52: WRITE Timing Parameters—ADV# LOW

| SYMBOL | -701/-708 | | -856 | | UNITS |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| $^{t}$AS | 0 | | 0 | | ns |
| $^{t}$AW | 70 | | 85 | | ns |
| $^{t}$BW | 70 | | 85 | | ns |
| $^{t}$CPH | 5 | | 5 | | ns |
| $^{t}$CW | 70 | | 85 | | ns |
| $^{t}$DH | 0 | | 0 | | ns |
| $^{t}$DW | 20 | | 20 | | ns |

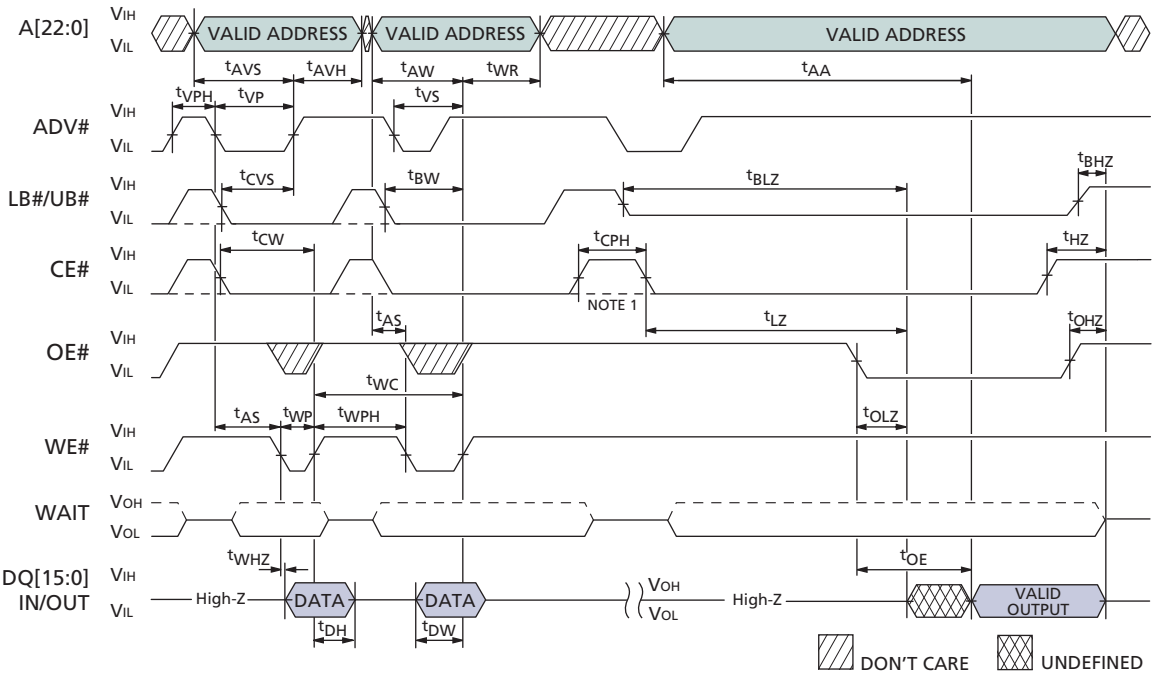
| SYMBOL | -701/-708 | | -856 | | UNITS |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| $^{t}$HZ | | 8 | | 8 | ns |
| $^{t}$WC | 70 | | 85 | | ns |
| $^{t}$WHZ | | 8 | | 8 | ns |
| $^{t}$WP | 45 | | 55 | | ns |
| $^{t}$WPH | 10 | | 10 | | ns |
| $^{t}$WR | 0 | | 0 | | ns |

## Table 53: READ Timing Parameters—ADV# LOW

| SYMBOL | -701/-708 | | -856 | | UNITS |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| $^{t}$AA | | 70 | | 85 | ns |
| $^{t}$BHZ | | 8 | | 8 | ns |
| $^{t}$BLZ | 10 | | 10 | | ns |
| $^{t}$HZ | | 8 | | 8 | ns |

| SYMBOL | -701/-708 | | -856 | | UNITS |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| $^{t}$LZ | 10 | | 10 | | ns |
| $^{t}$OE | | 20 | | 20 | ns |
| $^{t}$OHZ | | 8 | | 8 | ns |
| $^{t}$OLZ | 3 | | 3 | | ns |

## Figure 55: Asynchronous WRITE Followed by Asynchronous READ




NOTE:

1. When configured for synchronous mode (BCR[15] = 0), CE# must remain HIGH for at least 5ns ($^{t}$CPH) to schedule the appropriate refresh interval. Otherwise, $^{t}$CPH is only required after CE#-controlled WRITEs.

## Table 54: WRITE Timing Parameters—Async WRITE Followed by Async READ

| | -701/-708 | | -856 | | |
|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | UNITS |
| $^{t}$AS | 0 | | 0 | | ns |
| $^{t}$AVH | 2 | | 2 | | ns |
| $^{t}$AVS | 5 | | 5 | | ns |
| $^{t}$AW | 70 | | 85 | | ns |
| $^{t}$BW | 70 | | 85 | | ns |
| $^{t}$CPH | 5 | | 5 | | ns |
| $^{t}$CVS | 7 | | 7 | | ns |
| $^{t}$CW | 70 | | 85 | | ns |
| $^{t}$DH | 0 | | 0 | | ns |

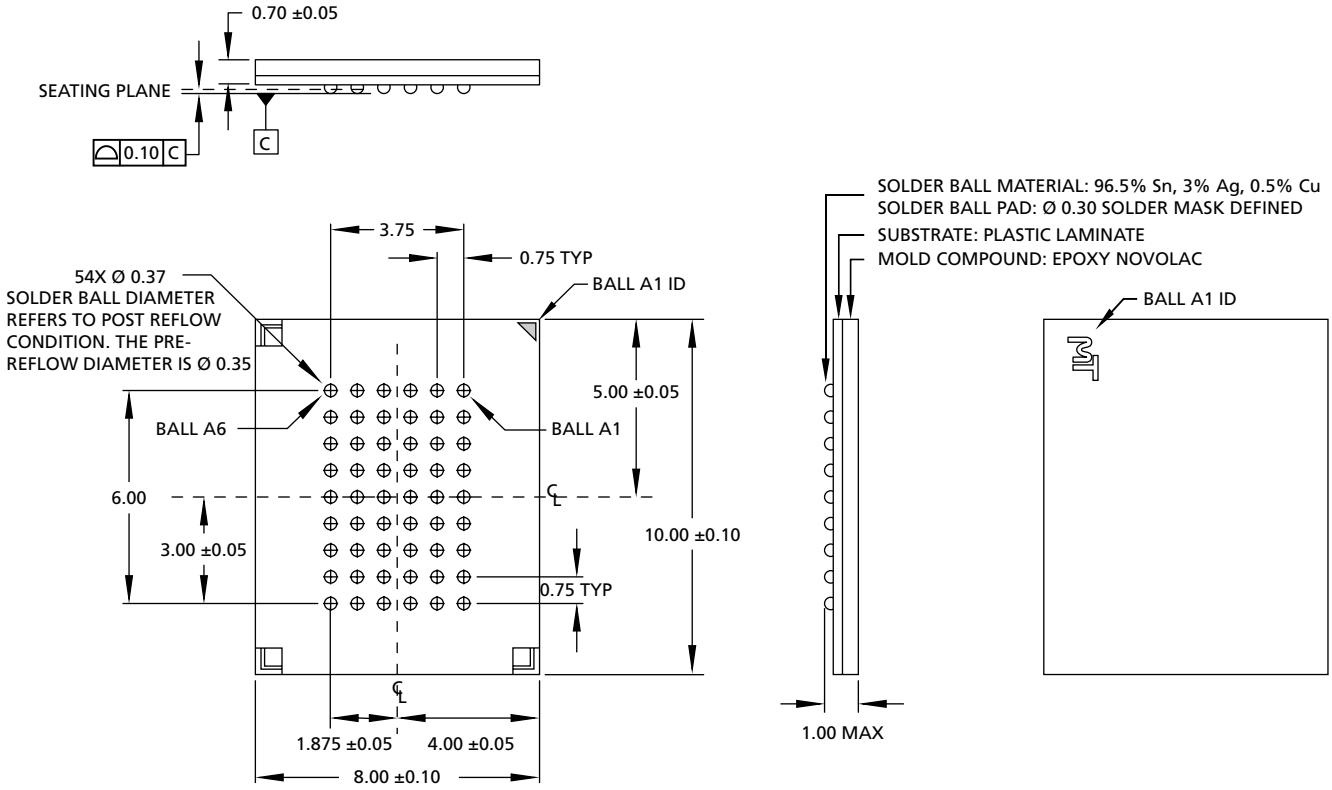
| | -701/-708 | | -856 | | |
|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | UNITS |
| $^{t}$DW | 20 | | 20 | | ns |
| $^{t}$VP | 5 | | 7 | | ns |
| $^{t}$VPH | 10 | | 10 | | ns |
| $^{t}$VS | 70 | | 85 | | ns |
| $^{t}$WC | 70 | | 85 | | ns |
| $^{t}$WHZ | | 8 | | 8 | ns |
| $^{t}$WP | 45 | | 55 | | ns |
| $^{t}$WPH | 10 | | 10 | | ns |
| $^{t}$WR | 0 | | 0 | | ns |

## Table 55: READ Timing Parameters—Async WRITE Followed by Async READ

| | -701/-708 | | -856 | | |
|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | UNITS |
| $^{t}$AA | | 70 | | 85 | ns |
| $^{t}$BHZ | | 8 | | 8 | ns |
| $^{t}$BLZ | 10 | | 10 | | ns |
| $^{t}$HZ | | 8 | | 8 | ns |

| | -701/-708 | | -856 | | |
|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | UNITS |
| $^{t}$LZ | 10 | | 10 | | ns |
| $^{t}$OE | | 20 | | 20 | ns |
| $^{t}$OHZ | | 8 | | 8 | ns |
| $^{t}$OLZ | 3 | | 3 | | ns |

## Figure 56: 54-Ball VFBGA




NOTE:

1. All dimensions in millimeters; MAX/MIN, or typical, as noted.

## Data Sheet Designation: Preliminary

This data sheet contains initial characterization limits, subject to change upon full characterization of production devices.

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## Revision History

Rev. A, Preliminary . . . . . 9/04
- Initial release.