CA3033, CA3047 Types
Operational Amplifiers

For High-Output-Current Applications

RCA-CA3033 is a high-performance integrated circuit operational amplifier featuring high input impedance, high gain, high power output, and low input-offset voltage and current. The device consists of two differential amplifiers in cascade and a single-ended class-B power output stage on a single monolithic silicon chip.

RCA-CA3033A has all the superior features and characteristics of the CA3033 but, in addition, can be operated at higher supply voltages to provide higher gain, higher common mode rejection, greater maximum output voltage swing, and more than double the power output.

RCA-CA3033 and CA3033A are hermetically sealed in 14-lead "dual-in-line" ceramic packages and are designed for operation over the full military temperature range of −55 °C to +125 °C.

The RCA-CA3047 and CA3047A are supplied in 14-lead, "dual-in-line" plastic packages and are designed to operate over the temperature range of 0°C to +70 °C, ambient.

Companion Application Note, ICAN-5641 "Application of RCA CA3033 and CA3033A High Performance Integrated-Circuit Operational Amplifiers."

The resistance values included on the schematic diagram have been supplied as a convenience to assist Equipment Manufacturers in optimizing the selection of "outboard" components of equipment designs. The values shown may vary as much as ±30%.

RCA reserves the right to make any changes in the Resistance Values provided such changes do not adversely affect the published performance characteristics of the device.

The RCA-CA3047 and CA3047A are electrically identical to the CA3033 and CA3033A, respectively, but are limited in operating and storage temperature range.

FEATURES

	CA3033 CA3047 V⁺ = +12 V V⁻ = −12 V	CA3033A CA3047A V⁺ = 15 V V⁻ = −15 V	
■ Output Current	36	76	mA min.
■ Input Offset Current	35	25	nA max.
■ Open Loop Differential Gain	84	87	dB min.
■ Output Voltage Swing.	18	23	V_{p-p} min.
■ Input Bias Current	350	180	nA max.
■ Power Output	80	220	mW min.
■ Common Mode Rejection Ratio	84	93	dB min.

APPLICATIONS

- Comparator
- Integrator
- Differentiator
- Audio Amplifier
- Summing Amplifier
- Servo Driver
- DC Amplifier
- Multivibrator
- Narrow Band and Band Pass Amplifier

ABSOLUTE-MAXIMUM RATINGS

	CA3033	CA3033A	CA3047	CA3047A
INPUT SIGNAL VOLTAGE	±10 V	−13 V, +10 V	±10 V	−13V, +10 V
DEVICE DISSIPATION:				
Up to T_A = 25 °C	1.2 W	1.2 W	750 mW	750 mW
Above T_A = 25 °C	Derate at 8 mW/°C		Derate at 6.67 mW/°C	
TEMPERATURE RANGE:				
Operating	−55 °C to +125 °C		0 °C to +70 °C	
Storage	−65 °C to +150 °C		−65 °C to +150 °C	
LEAD TEMPERATURE (During Soldering):				
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265°C			

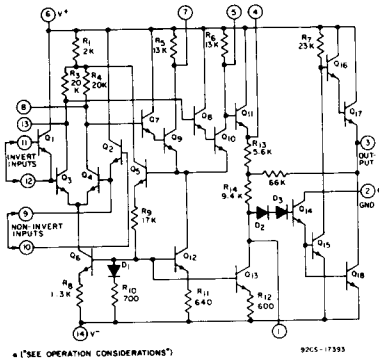

Fig. 1 - Schematic diagram of operational amplifiers, CA3033, CA3033A, CA3047, CA3047A.

MAXIMUM VOLTAGE RATINGS at T_A = 25° C — CA3033, CA3047

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 1 with respect to the horizontal terminal 14 is 0 to +4 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1		*	*	*	*	*	*	*	*	*	*	*	*	+4 0
2			*	*	*	*	*	*	*	*	*	*	*	+26 0
3				*	*	0 −26	*	*	*	*	*	*	*	+26 0
4					+5 −1	0 −15	*	*	*	*	*	*	*	+26 0
5						0 −26	*	+20 −1 Note 1	*	*	*	*	+20 −1 Note 1	*
6							+26 0	+26 0	+26 0	+26 0	+26 0	+26 0	+26 0	+26 0
7								+20 −2 Note 1	*	*	*	*	+20 −2 Note 1	+26 0
8									+20 −1 Note 2	+20 −2 Note 3	+20 −2 Note 3	+20 −1 Note 2	*	+26 0
9										+1 −5	*	+5 −5	+1 −20 Note 2	+26 −5
10											+10 −10	*	+2 −20 Note 3	+26 −10
11												+1 −5	+2 −20 Note 3	+26 −10
12													+1 −20 Note 2	+26 −5
13														*
14														Sub-strate

MAXIMUM CURRENT RATINGS

CA3033 CA3047 / CA3033A CA3047A

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	5	5
2	20	-
3	50	50
4	10	10
5	5	5
6	-	-
7	5	5
8	1	1
9	1	0.1
10	1	0.1
11	1	0.1
12	1	0.1
13	1	1
14	-	-

Notes: 1. This rating applies to the more positive terminal of terminals 8 and 13.
2. This rating applies to the more positive terminal of terminals 9 and 12.
3. This rating applies to the more positive terminal of terminals 10 and 11.

*Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

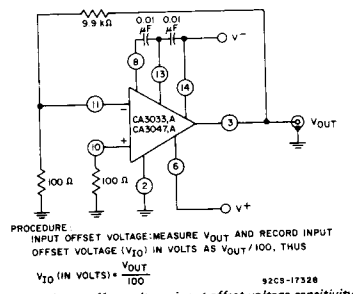

Fig. 2a - Input offset voltage, input offset voltage sensitivity, and device dissipation test circuit.

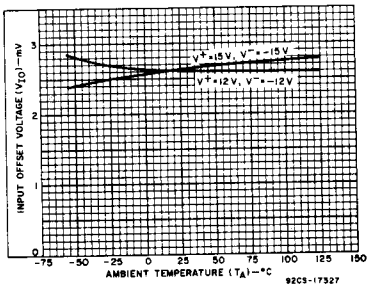

Fig. 2b - Typical input offset voltage vs. ambient temperature.

MAXIMUM VOLTAGE RATINGS at T_A = 25° C **CA3033A, CA3047A**

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 1 with respect to the horizontal terminal **14** is 0 to +4 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1		*	*	*	*	*	*	*	*	*	*	*	*	+4 0
2			*	*	*	*	*	*	*	*	*	*	*	+38 0
3				*	*	0 -38	*	*	*	*	*	*	*	+38 0
4					+5 -1	0 -22	*	*	*	*	*	*	*	+38 0
5						0 -38	*	+30 -1 Note 1	*	*	*	*	+30 -2 Note 1	*
6							+38 0	+38 0	+38 0	+38 0	+38 0	+38 0	+38 0	+38 0
7								+30 -2 Note 1	*	*	*	*	+20 -2 Note 1	+38 0
8									+30 -1 Note 2	+30 -2 Note 3	+30 -2 Note 3	+30 -1 Note 2	*	+38 0
9										+1 -5	*	+5 -5	+1 -30 Note 2	+38 -5
10											+10 -10	*	+2 -20 Note 3	+38 -10
11												+1 -5	+2 -30 Note 3	+38 -10
12													+1 -30 Note 2	+38 -5
13														*
14														Sub- strate

Notes: See CA3033, CA3047 Rating Chart Notes.

MAXIMUM CURRENT RATINGS are identical for all four types (See CA3033, CA3047 chart)

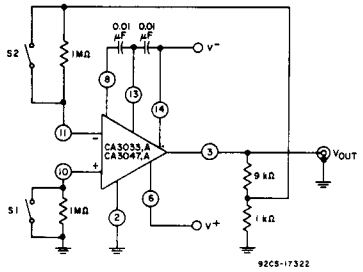

Fig. 3a - Input offset current and input bias current test circuit.

PROCEDURES:

A. Inverting Input Current,
Set switch, S_1 in closed position and set switch, S_2 in open position.
Measure output voltage and convert this reading to inverting input current using the following relation:

$$I_I \text{ inverting (in } \mu A) = \frac{V_{OUT} \text{ (in volts)}}{10}$$

B. Non-inverting Input Current
Set switch, S_1 in open position and set switch, S_2 in closed position.
Measure output voltage and convert this reading to non-inverting input current using the following relation:

$$I_I \text{ non-inverting (in } \mu A) = \frac{-V_{OUT} \text{ (in volts)}}{10}$$

C. Input Offset Current
Set switches, S_1 and S_2 in open positions.
Measure output voltage and convert this reading to input offset current using the following relation:

$$I_{IO} \text{ (in } \mu A) = \frac{V_{OUT} \text{ (in volts)}}{10}$$

ELECTRICAL CHARACTERISTICS
For Equipment Design

Characteristics	Symbols	Test Conditions				LIMITS						Units
						CA3033 CA3047			CA3033A CA3047A			
		Circuit	T_A = 25° C		Typical Characteristics Curves	DC Supply Voltage V^+ = 12 V V^- = −12 V			V^+ = 15 V V^- = −15 V			
		Fig.			Fig.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage	V_{IO}	2a			2b	–	2.6	5	–	2.9	5	mV
Input Offset Current	I_{IO}	3a			3b	–	5	35	–	9	25	nA
Input Bias Current	I_I	3a			3c	–	70	350	–	100	180	nA
Input Offset Voltage Sensitivity: Positive	$\Delta V_{IO}/\Delta V^+$	2a			–	–	0.3	0.5	–	0.2	0.5	mV/V
Negative	$\Delta V_{IO}/\Delta V^-$	2a			–	–	0.3	0.5	–	0.2	0.5	mV/V
Device Dissipation	P_T	2a			–	60	120	180	80	170	300	mW
Open-Loop Differential Voltage Gain	A_{OL}	–	f = 1 kHz		4	84	90	–	87	93	–	dB
Common-Mode Rejection Ratio	CMRR	–			5	84	100	–	93	105	–	dB
Common-Mode Input-Voltage Range	V_{ICR}	–	f = 1 kHz		–	−7.5	+5,−9	+3.5	−9.7	6,−11	4.7	V
Maximum Output-Voltage Swing	V_O(P-P)	–		R_L = 500 Ω	–	18	22	–	–	–	–	V_{P-P}
				R_L = 300 Ω		–	–	–	23	25	–	
Input Impedance	Z_I	–			–	0.25	1.5	–	0.6	1	–	MΩ
Output Current	I_O	–		R_L = 500 Ω	6	35	44	–	–	–	–	mA-(P-P)
				R_L = 300 Ω		–	–	–	76	83	–	
Power Output THD <5%	P_o	–		R_L = 500 Ω	7	80	122	–	–	–	–	mW
				R_L = 300 Ω		–	–	–	220	255	–	

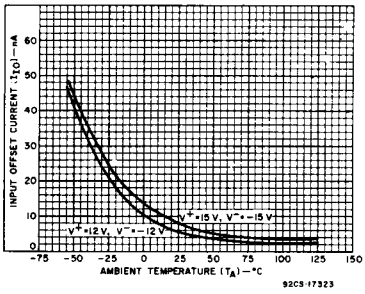

Fig. 3b - Typical input offset current vs. ambient temperature.

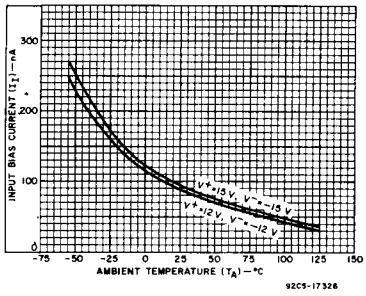

Fig. 3c - Typical input bias current vs. ambient temperature.

ELECTRICAL CHARACTERISTICS

Typical Values Intended Only for Design Guidance

Input Offset Voltage Drift −55°C to 125°C	$V_{IO}/\Delta T$	2a		2b	–	6.6	–	–	6.6	–	μV/°C
Input Offset Current Drift											
−55°C to 25°C	$I_{IO}/\Delta T$	3a		3b	–	1	–	–	1	–	nA/°C
25°C to 125°C					–	0.08	–	–	0.08	–	
60-dB Amplifier Bandwidth	BW	8a	C_X, C_Y = 0.001 μF	8b,c	–	230	–	–	350	–	kHz
Slew Rate	SR	9	(amplifier circuit only)	–	–	2.7	–	–	3	–	V/μs

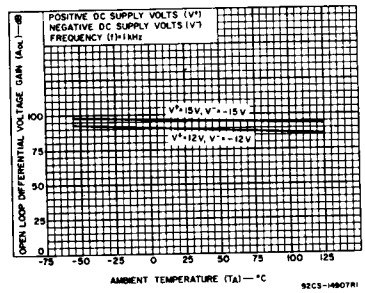

Fig. 4 - Typical open-loop differential voltage gain vs. ambient temperature.

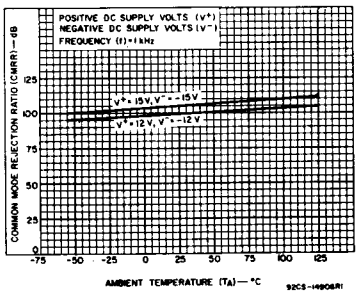

Fig. 5 - Typical common mode rejection ratio vs. ambient temperature.

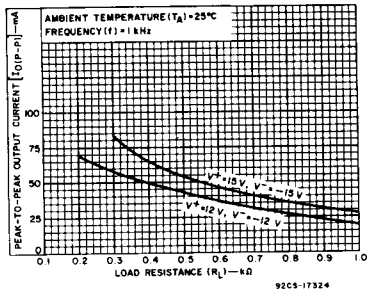

Fig. 6 - Typical peak-to-peak output current vs. load resistance.

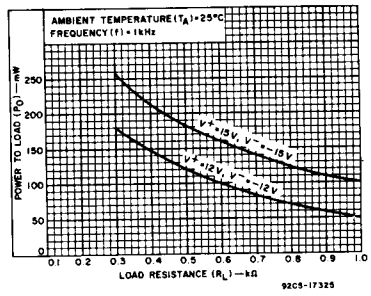

Fig. 7 - Typical power output vs. load resistance.

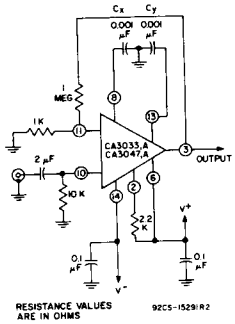

Fig. 8a - Typical 60-dB amplifier.

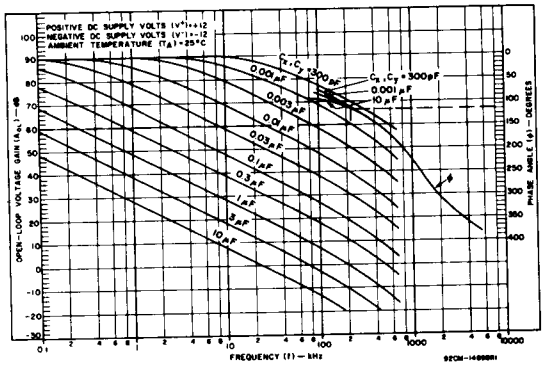

Fig. 8b - Typical phase compensation characteristics for CA3033, CA3047 (V^+ = +12 V, V^- = −12 V)

For any desired closed loop gain (in decibels), read horizontally along the gain line to the attenuation curve which provides the desired closed loop bandwidth. The required values for the compensation capacitors is shown on the curve. Move vertically from the intersection of the gain and attenuation lines until the phase angle curve (ϕ) is reached and read the phase angle between the input and output on the right-hand scale. The difference between the indicated phase angle and 180° is the typical phase margin. (A minimum phase margin of 45° is recommended to allow for component variations and differences among amplifiers.) If the phase margin is smaller than required, the desired bandwidth can be stably achieved through the use of a more complex feedback network. As the closed loop gain approaches unity, the compensating capacitors required (0.3 μF to 1.0 μF) are bulky and costly. A capacitor one-half the value shown on the chart, connected between terminals 8 and 13, and a 0.001 μF capacitor from either terminals 8 or 13 to ground or V^- is an acceptable alternative method. This arrangement provides the same gain-phase roll-off shown on the curves and permits the use of more readily available, lower-voltage disc capacitors which are smaller and cost less. For linear operation, the maximum expected difference voltage between the two collectors is less than 1 volt.

Figure 8a shows the phase compensating capacitors (C_X, C_Y) returned to ground. In some systems with large parasitic impedances in the power supply system, returning these capacitors to the negative (V^-) supply may result in more stable operation.

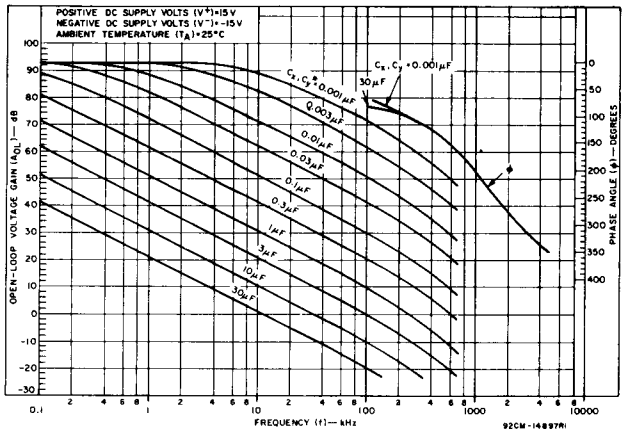

Fig. 8c - Typical phase compensation characteristics for CA3033A, CA3047A (V^+ = 15 V, V^- = −15 V).

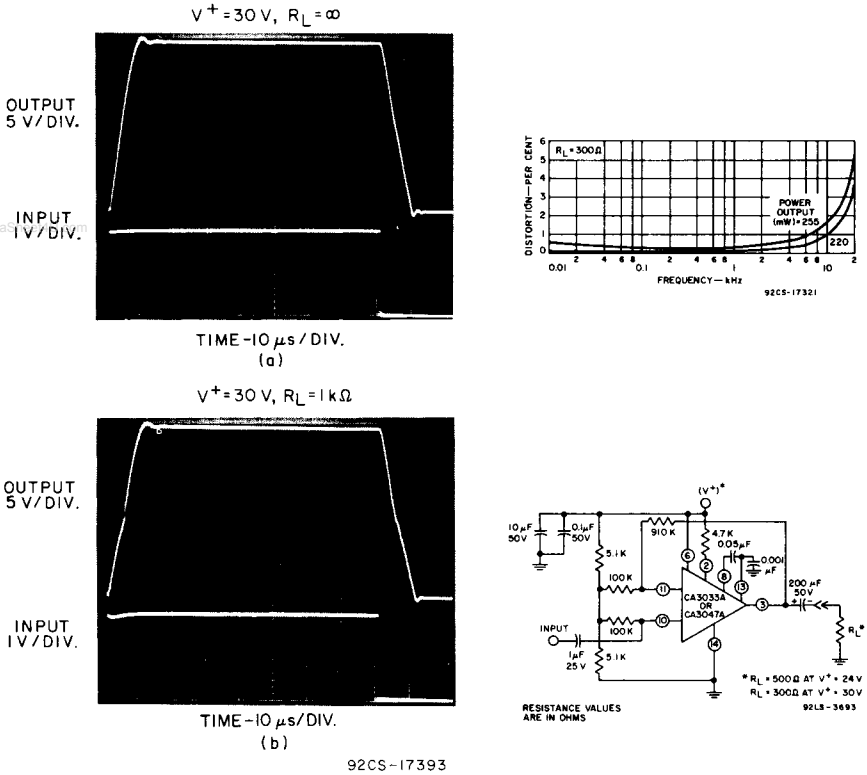

Fig. 9 - Amplifier with single voltage supply and associated pulse response waveforms and distortion curves.

OPERATING CONSIDERATIONS

The CA3033, CA3033A, CA3047, and CA3047A operational amplifiers have very high peak-pulse current capability. The open-loop output impedance is typically less than 30 ohms at 10 kHz and the peak short-circuit output current may exceed 100 milliamperes. To prevent possible damage to the chip because of excessive dissipation it is important that the output stage is not subjected to sustained high peak currents. To minimize the possibility of damage from accidental shorts, it is recommended that a 51-ohm resistor be placed in series with the output circuit.

When high peak output currents are required of the amplifier, it is desirable to provide a current-limiting resistor of about 2200 ohms in series with the collector of transistor Q_{14}. This resistor may be returned to ground, or, if its value is increased to 4700 ohms, it may be returned to the V^+ terminal.