



AWT1921S11

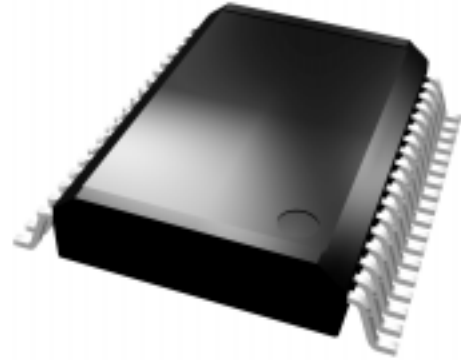
Integrated High Power Amp 1610 MHz
Advanced Product information
Rev 4

DESCRIPTION

The AWT1921 is a four stage monolithic amplifier for use in communication systems that require high gain and output intercept point. The device has been specifically designed for fixed satellite access equipment and handset booster amplifier applications.

DESCRIPTION

- High Output Intercept Point
- High Linearity
- True Surface Mount Package
- Internal Bias Circuit Requiring Nominal Input Voltages $\pm 10\%$
- Low Cost
- Off Chip Output Matching Circuit Allows Application Optimization



S11
SSOP-28
28 Pin Wide Body w/ Heat Slug

ABSOLUTE MAXIMUM RATINGS

PIN	SIGNAL	MAX RATING	PIN	SIGNAL	MAX RATING
2	V _{DD}	+7V _{DC}	11	V _{REF}	+7 V _{DC}
3	RF _{IN}	+20 dBm	12	V _{SS}	-7 V _{DC}
4,5	V _{D1}	+10 V _{DC}	18,19,20,21,22,23,24,25	V _{D3}	+10 V _{DC}

Operating Temperature: - 30 to + 85° C

Storage Temperature: - 55 to +100° C

ELECTRICAL SPECIFICATIONS ⁽¹⁾(Pin with CDMA modulation, $f_o = 1610 - 1626.5$ MHz, $V_{DS1} = V_{DS2} = V_{DS3} = V_{DS4} = 9.0V$, $V_{SS} = -5V$, $T_c=25C$, 50Ω System⁽²⁾)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS
Frequency	f_o	1610		1626.5	MHz
Power Output	P_{OUT}	-	35		dBm
Power Added Efficiency	η_{Eff}	-	25		%
Gain @ $P_{OUT} = +35$ dBm	PG	-	28		dB
ACPR @ 0.730 MHz 1.23 MHz	-	-	25 -28	-	dBc
Harmonics ⁽³⁾ 2nd 3rd 4th	-	-	45 52 -45	-	dBc
Stability: - 60 dBc all spurious outputs relative to desired signal	-	-	3:1	-	VSWR load, all phase angles
Bias supply currents	I_{SS} I_{REF} I_{DD}	-	15 5 15	-	mA
Quiescent Currents	I_{DQ1} I_{DQ2} I_{DQ3} I_{DQ4}	-	60 90 150 200	-	mA
Input Return Loss	-	-	10	-	dB
Gain Flatness @ $P_{out} = +35$ dBm	ΔPG	-	1.0	-	dB
Thermal Resistance ⁴	-	-	4.5	-	C/W

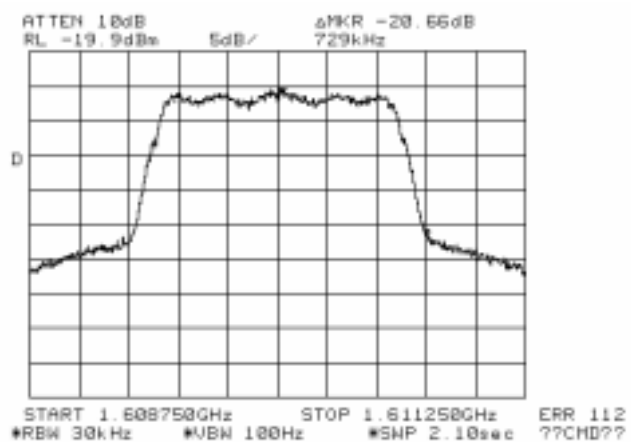
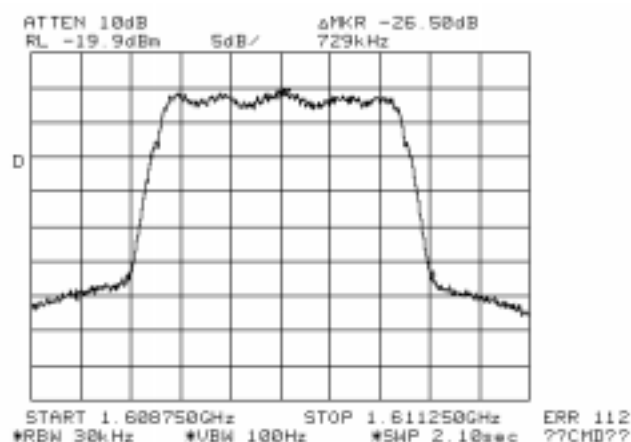
Notes:

1: As measured in ANADIGICS test fixture, see application section

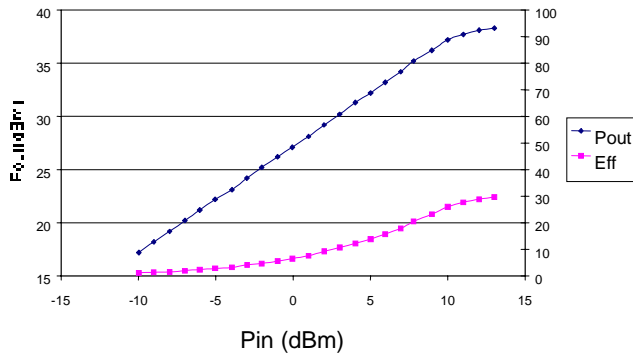
2: 50Ω Measurement system after off chip matching circuit, input terminated in 50Ω 3: Measured at $P_{out} = +35$ dBm

4: Thermal resistance for junction to bottom of slug

$$\Theta_{jc} = \frac{T_j - T_c}{(I_{D1} + I_{D2} + I_{D3} + I_{D4})V_{SUP} - P_{OUT}}$$

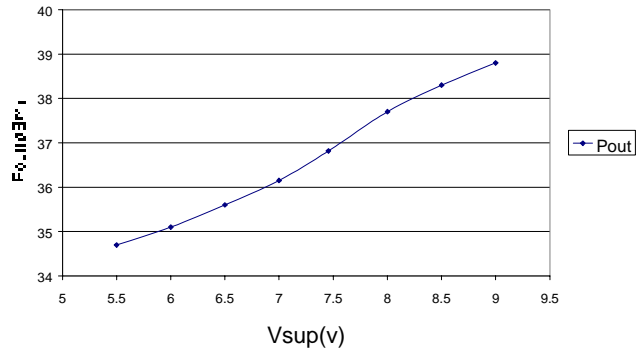
ACPR @ Pout = 35 dBm**ACPR @ Pout = 35 dBm**

Pout & Eff vs Pin



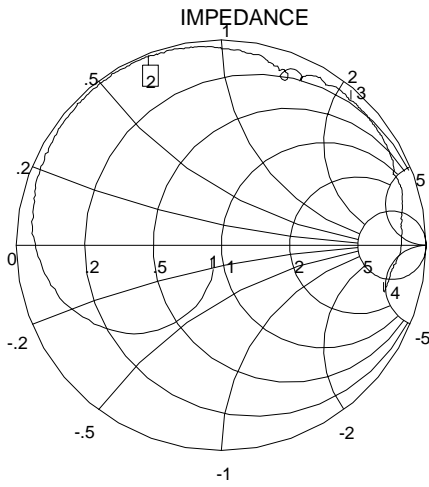
* Pout with CDMA Modulation

Pout vs Supply Voltage



Pin = 10 dBm, with CDMA Modulation

S11 FORWARD REFLECTION

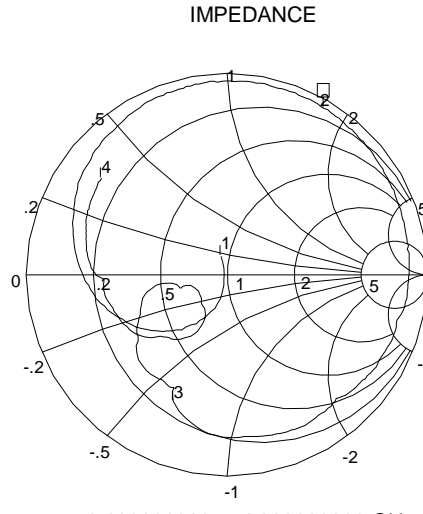


0.100000000 - 4.800000000 GHz

Impedance as seen by V_{DS1}

CH 1 - S11
REFERENCE PLANE
6.3507 cm
MARKER 2
1.615750000 GHz
542.467 m
34.621 j
MARKER TO MAX
MARKER TO MIN
1 0.100000000 GHz
45.066
-10.839 j
3 3.225500000 GHz
7.790
112.368 j
4 4.800000000 GHz
164.733
-244.870 j
MARKER READOUT
FUNCTIONS

S11 FORWARD REFLECTION

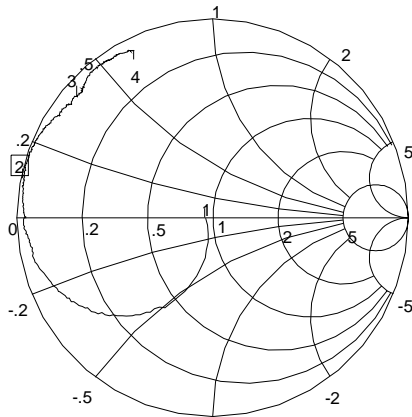


0.100000000 - 4.800000000 GHz

Impedance as seen by V_{DS2}

CH 1 - S11
REFERENCE PLANE
6.3507 cm
MARKER 2
1.615750000 GHz
4.443
86.992 j
MARKER TO MAX
MARKER TO MIN
1 0.100000000 GHz
46.485
8.658 j
3 3.225500000 GHz
13.359
-31.442 j
4 4.800000000 GHz
6.663
16.669 j
MARKER READOUT
FUNCTIONS

S11 FORWARD REFLECTION
IMPEDANCE

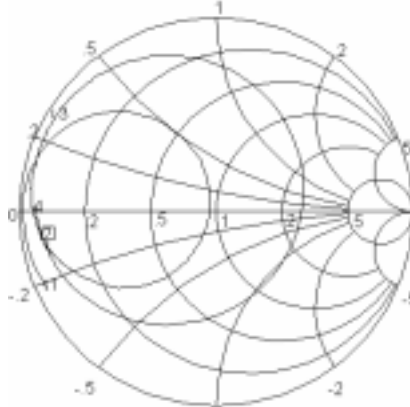


0.100000000 - 4.800000000 GHz

Impedance as seen by V_{DS3}

CH 1 - S11
REFERENCE PLANE
6.3507 cm
MARKER 2
1.615750000 GHz
423.067 m
4.971 j
MARKER TO MAX
MARKER TO MIN
1 0.100000000 GHz
46.696
-381.126 j
3 3.225500000 GHz
2.436
18.889 j
4 4.800000000 GHz
2.544
31.529 j
MARKER READOUT
FUNCTIONS

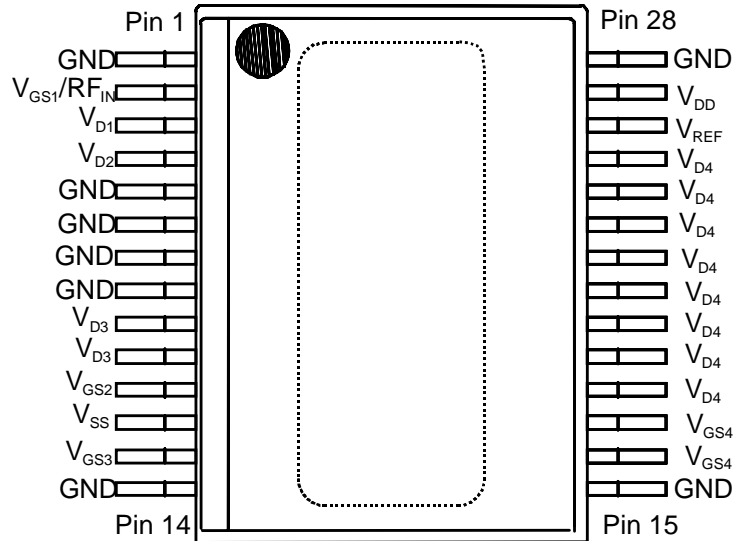
S11 FORWARD REFLECTION
IMPEDANCE



0.100000000 - 4.800000000 GHz

Impedance as seen by V_{DS4}

CH 1 - S11
REFERENCE PLANE
6.3507 cm
MARKER 2
1.615750000 GHz
2.202
-5.787 j
MARKER TO MAX
MARKER TO MIN
1 0.100000000 GHz
1.462
-11.138 j
3 3.225500000 GHz
1.397
13.314 j
4 4.800000000 GHz
2.436
-565.322 j
MARKER READOUT
FUNCTIONS



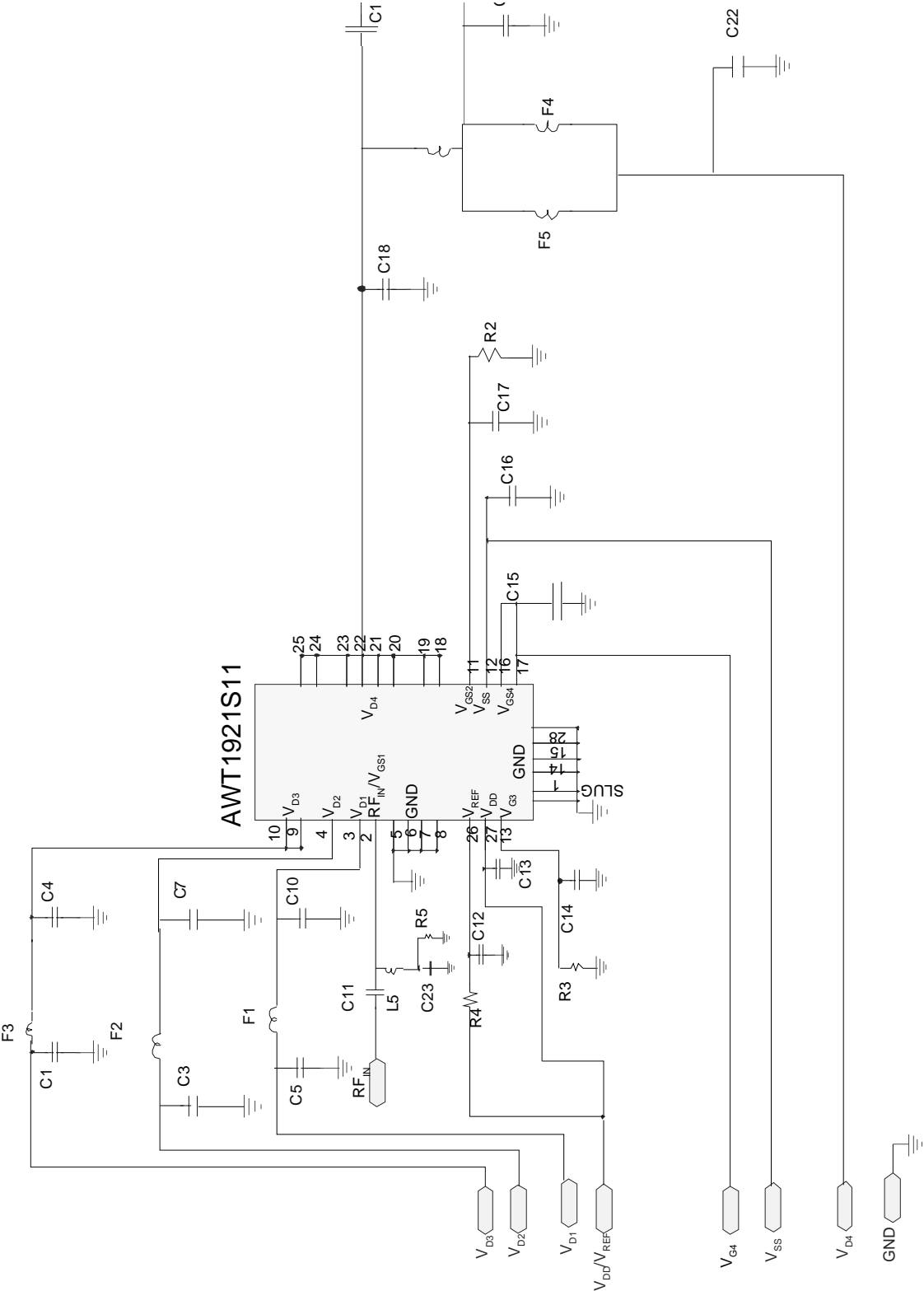
PIN DESCRIPTION

PIN	SIGNAL	DESCRIPTION
1,14,15,28, slug	GND	AC and RF Ground
2	V_{GS1} & RF_{IN}	First Stage Gate terminal & RF Input
27	V_{DD}	Positive Supply of Bias Circuit(+5V)
4	V_{D2}	Second Stage drain supply (+9V)
3	V_{D1}	First Stage drain supply (+9V)
5,6,7,8	GND	First and Second Stage Source ground
9,10	V_{D3}	Third Stage drain supply (+9V)
11	V_{GS2}	Second Stage Gate Terminal
26	V_{REF}	Bias control Pin (+5V)
12	V_{SS}	Negative Supply for Bias Circuit (-5V)
13	V_{GS3}	Third Stage Gate terminal
16,17	V_{GS4}	Fourth Stage Gate terminal
18-25	V_{D4}	Fourth Stage drain supply (+9V) & RF out

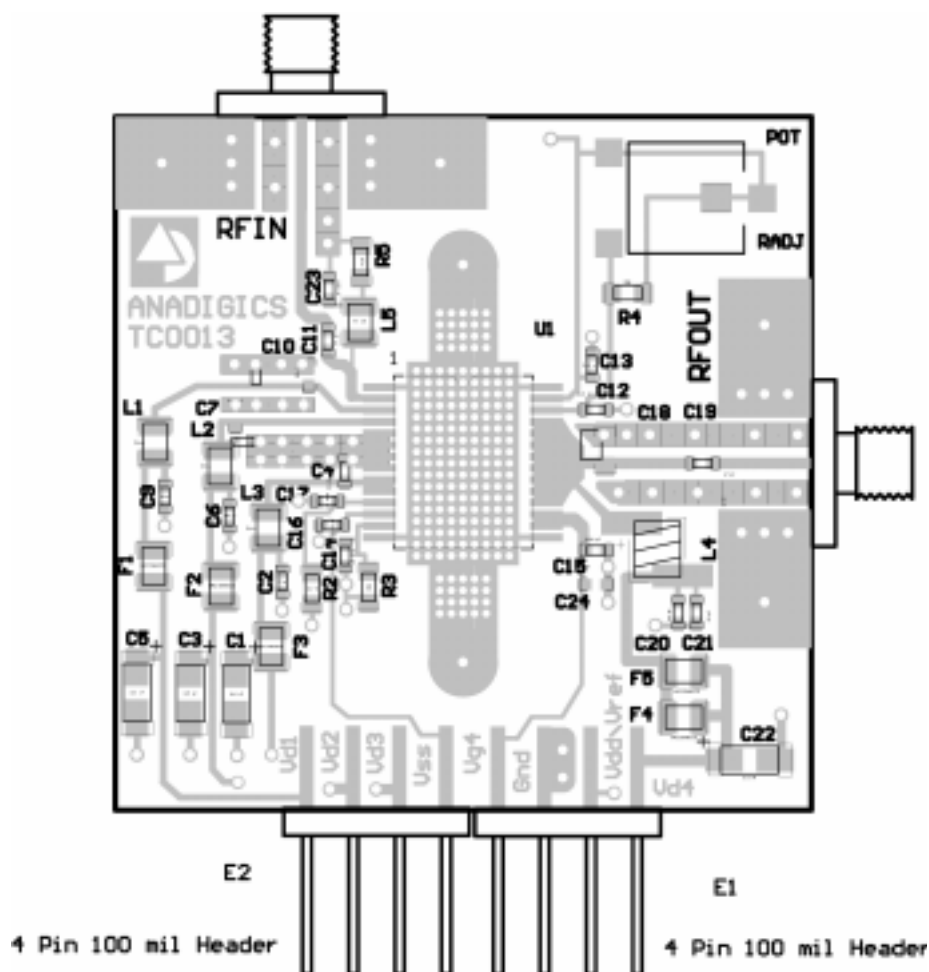
PROCEDURE FOR AMPLIFIER OPERATION AND TEST

- 1) Slug must be thermally and electrically connected to obtain rated performance
- 2) The V_{SS} Voltage should be applied first to the amplifier prior to V_{D1} , V_{D2} , V_{D3} , or V_{D4} voltages
- 3) V_{GS1} , V_{GS2} , V_{GS3} , V_{GS4} may be used as monitor points to verify that the bias circuit is working properly. These pins should measure as negative voltage potential, after V_{SS} is applied.
- 4) The Bias Pins V_{DD} and V_{REF} may be applied with no V_{SS} voltage present
- 5) Always Follow ESD precautions when handling these devices

1610 – 1626.5 MHZ TEST CIRCUIT SCHEMATIC



TEST CIRCUIT SCHEMATIC FOR 1610 -1626.5 MHZ APPLICATION



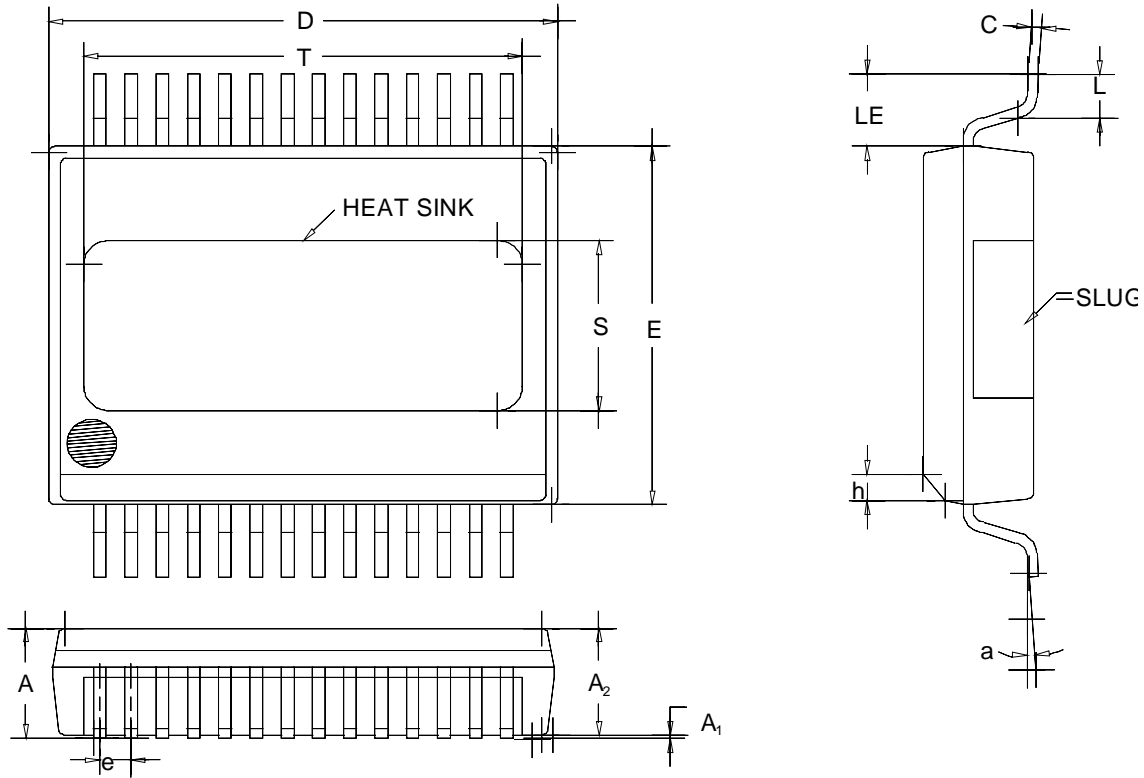
1610 – 1626.5 MHz Test Circuit Layout

DESIGNATION	VALUE
C1,C3,C5,C22	2.2 μ F
C2,C7,C9,C24	Not Used
C4	15 pF
C6, C10	10 pF
C11,C19	27 pF
C12,C13,C20,C21	33 pF
C14,C16,C17,C23	0.01 μ F
C15	22 pF
C18	4.7 pF
F1,F2,F3,F4,F5	Feritte
L1,L3	Shim
L2	2.7 nH
L4	8 nH
L5	47 nH
R2, R5	5600 ?
R3	1500 ?
R4	2200 ?

Notes:

1. Material 6 layer FR4
2. 1 oz. copper
3. 14 mil layers
4. Gerber files available

PACKAGE OUTLINE



SYMBOL	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	0.087	0.093	2.21	2.36	
A ₁	0.000	0.004	0.00	0.10	
A ₂	0.087	0.089	2.21	2.25	
B	0.008	0.012	0.36	0.46	
C	0.007	0.009	0.18	0.25	
D	0.400	0.408	10.16	10.36	2
E	0.292	0.296	7.42	7.52	2
e	0.025	BSC	0.64	BSC	4
H	0.410	0.418	10.41	40.62	
h	0.018	0.024	0.48	0.61	
L	0.034	0.038	0.86	0.97	
LE	0.84		1.37		
a	0	8	0	8	
S	0.139	0.141	3.54	3.55	5
T	0.349	0.351	8.86	8.92	5

Notes:

1. Controlling dimensions : inches
2. Dimension "d" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions and gate burrs shall not exceed 0.006 (0.16mm)
3. Dimension "e" does not include inter-lead or protrusions. Inter-lead flash and protrusions shall not exceed 0.010 (0.25mm) per side.
4. Maximum lead twist/skew to be 0.002 (0.05mm)
5. Mold flash shall not extend more than 0.010 (0.25mm) on any edge of heat slug

Designation	Value	Manufacture	Manufacture Part #	Web Address
C1,C3,C5,C22	2.2 μ F	Panasonic	ECS-H1AY225R	www.panasonic.com
C2,C7,C9,C24	Not Used			
C4	15 pF	Murata	GRM36COG150J50	www.murata.com
C6,C10	10 pF	Murata	GRM36COG100J50	
C11,C19	27 pF	Murata	GRM36COG270J50	www.murata.com
C12,C13,C20,C21	33 pF	Murata	GRM36COG330J50	www.murata.com
C14,C16,C17, C23	0.01 μ F	Murata	GRM36X7R103K16	www.murata.com
C15	22 pF	Murata	GRM36COG220J50	www.murata.com
C18	4.7 pF	American Technical Ceramics	ATC100A4R7CW150X	www.atc-cap.com
F1,F2,F3,F4,F5	Ferrite 47 Ω @ 100 MHz, 1A Rating	Taiyo Yuden	BK2125HS470	www.t-yuden.com
L1, L3	Shim			
L2	2.7 nH	Toko	LL2012-F2N7S	www.tokoam.com
L4	8 nH	Coilcraft	A03T	www.coilcraft.com
L5	47 nH	Coilcraft	0805CS470XMBC	www.coilcraft.com
R2,R5	5600 Ω	Panasonic	ERJ-36SYJ562V	www.panasonic.com
R3	1500 Ω	Panasonic	ERJ-36SYJ302V	www.panasonic.com
R4	2200 Ω	Panasonic	ERJ-36SYJ512V	www.panasonic.com

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