Winbond Electronics Corp.

256K ´ 16 CMOS FLASH MEMORY

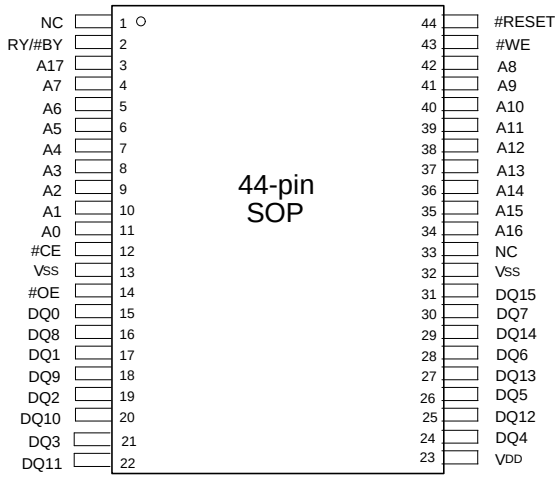
1. GENERAL DESCRIPTION

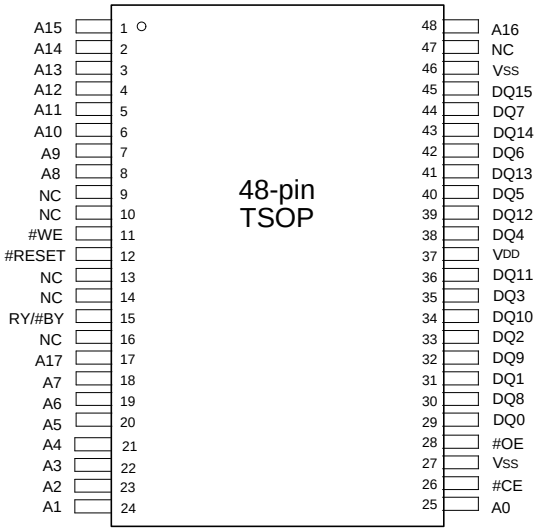
The W49L401(T) is a 4-megabit, 3.3-volt only CMOS flash memory organized as 256K × 16 bits. The device can be programmed and erased in-system with a standard 3.3-volt power supply. A 12-volt V_{PP} is not required. The unique cell architecture of the W49L401(T) results in fast program/erase operations with extremely low current consumption (compared to other comparable 3.3-volt flash memory products). The device can also be programmed and erased using standard EPROM programmers.

2. FEATURES

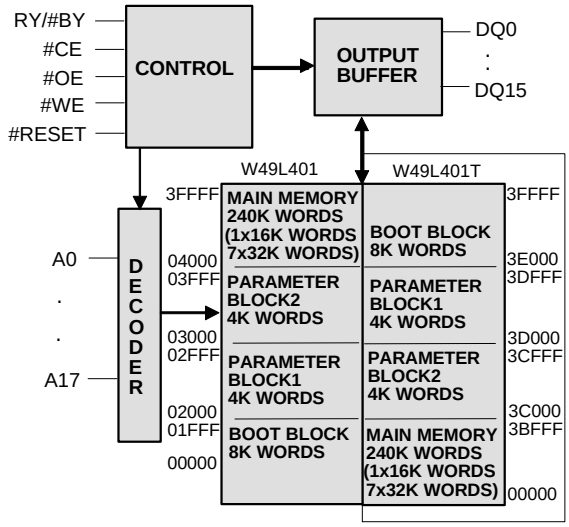
- Single Voltage operations:
  - 3.0 – 3.6V Read/Erase/Program
- Fast Program operation:
  - Word-by-Word programming: 30 μS (typ.)
- Fast Erase operation:
  - Page/Block Erase time: 50 mS (typ.)
  - Chip Erase time: 200 mS (typ.)
- Fast Read access time: 70 nS
- Endurance: 10K cycles (typ.)
- Twenty-year data retention
- Hardware data protection
- Block configuration
  - One 8K-word boot block with lockout protection
  - Two 4K-word parameter blocks
  - One 16K-word main memory array block
  - Seven 32K-word main memory array blocks
  - 128 uniform 2K-word pages
- Optional Uniform Page configuration
- Low power consumption
  - Active current: 10 mA (typ.)
  - Standby current: 5 μA (typ.)
- Automatic program and erase timing with internal V_{PP} generation
- End of program or erase detection
  - Toggle bit
  - Data polling
- RY/#BY open-drain output provides hardware end-of-write detection
- Hardware #RESET pin
- Latched address and data
- TTL compatible I/O
- JEDEC standard word-wide pinouts
- Available packages: 44-pin SOP, 48-pin TSOP

3. PIN CONFIGURATIONS





4. BLOCK DIAGRAM



5. PIN DESCRIPTION

SYMBOL	PIN NAME
#RESET	Reset
RY/#BY	Ready/#Busy Output
A0 – A17	Address Inputs
DQ0 – DQ15	Data Inputs/Outputs
#CE	Chip Enable
#OE	Output Enable
#WE	Write Enable
VDD	Power Supply
VSS	Ground
NC	No Connection

6. FUNCTIONAL DESCRIPTION

Read Mode

The read operation of the W49L401(T) is controlled by #CE and #OE, both of which have to be low for the host to obtain data from the outputs. #CE is used for device selection. When #CE is high, the chip is de-selected and only standby power will be consumed. #OE is the output control and is used to gate data to the output pins. The data bus is in high impedance state when either #CE or #OE is high. Refer to the timing waveforms for further details.

Reset Operation

The #RESET input pin can be used in some application. When #RESET pin is at high state, the device is in normal operation mode. When #RESET pin is driven low for at least a period of T_{RP}, it will halt the device and all outputs are at high impedance state. The device also resets the internal state machine to read array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence to assure data integrity. As the high state re-asserted to the #RESET pin, the device will return to read or standby mode, it depends on the control signals. The system can read data T_{RH} after the #RESET pin returns to V_{IH}. The other function for #RESET pin is temporary reset the boot block. By applying the 12V to #RESET pin, the boot block can be reprogrammed even though the boot block lockout function is enabled.

Boot Block Operation

There is one 8K-word boot block in this device, which can be used to store boot code. It is located in the first 8K words (for W49L401T, located in the last 8K words) of the memory with the address range from 0000(hex) to 1FFF(hex). (for W49L401T, address range from 3E000h to 3FFFFh)

See Command Codes for Boot Block Lockout Enable for the specific code. Once this feature is set, the data for the designated block cannot be erased or programmed (programming lockout); the regular programming method can change the data in other memory locations.

There is one condition that the lockout feature can be over-ridden. Just apply 12V to #RESET pin, the lockout feature will temporarily be inactivated and the boot block can be erased/programmed. Once the #RESET pin returns to CMOS/TTL level, the lockout feature will be activated again.

In order to detect whether the boot block feature is set on the 8K-words block, users can perform software command sequence: enter the product identification mode (see Command Codes for Identification/Boot Block Lockout Detection for specific code), and then read from address "0002 hex". If the output data in DQ0 is "1", the boot block programming lockout feature is activated; if the output data in DQ0 is "0", the lockout feature is inactivated and the block can be erased/programmed.

To return to normal operation, perform a three-byte command sequence (or an alternate single-word command) to exit the identification mode. For the specific code, see Command Codes for Identification/Boot Block Lockout Detection.

Chip Erase Operation

The chip-erase mode can be initiated by a six-word command sequence. After the command loading cycle, the device enters the internal chip erase mode, which is automatically timed and will be completed in a fast 200 mS (typical). The host system is not required to provide any control or timing during this operation. The entire memory array will be erased to FFFF(hex) by the chip erase operation if the boot block programming lockout feature is not activated. Once the boot block lockout feature is activated, the chip erase function will erase all the blocks/pages except the boot block.

Block/Page Erase Operation

The W49L401(T) provides both uniform small page (2K-word) and non-symmetrical block (4K/8K/16K/32K-word) erase capabilities for versatile Flash applications.

Each block or page can be erased individually by initiating a six-word command sequence. The block address (BA) or page address (PA) is latched on the falling #WE edge of the sixth cycle while the XX30/XX50(hex) data input command is latched at the rising edge of #WE. After the command loading cycle, the device enters the internal block/page erase mode, which is automatically timed and will be completed in a fast 50 mS (typical). The host system is not required to provide any control or timing during this operation. The device will automatically return to normal read mode after the erase operation completed. Data-polling, Toggle-Bit and/or RY/#BY pin can be used to detect end of erase cycle.

The bootblock (8K-words) consists of 4 corresponding uniform pages of 2K-words each. When the boot block lockout feature is activated, any page/block erase command with the associated PA/BA within the bootblock address range (0000-01FFF for W49L401, and 3E000-3FFFF for W49L401T) will be ignored and the device will return to read mode without any data changes.

Program Operation

The W49L401(T) is programmed on a word-by-word basis. Program operation can only change logical data "1" to logical data "0" The erase operation (changed entire data in individual page/block or whole chip from "0" to "1") is needed before programming.

The program operation is initiated by a 4-word command cycle (see Command Codes for Word Programming). The device will internally enter the program operation immediately after the word-program command is entered. The internal program timer will automatically time-out (50 μS max. - T_{BP}) once completed and return to normal read mode. Data_polling, Toggle_Bit and/or RY/#BY pin can be used to detect end of program cycle.

Hardware Data Protection

The integrity of the data stored in the W49L401(T) is also hardware protected in the following ways:

(1) Noise/Glitch Protection: A #WE pulse of less than 10 nS in duration will not initiate a write cycle.

(2) V_{DD} Power Up/Down Detection: The programming operation and read are inhibited when V_{DD} is less than 1.8V typical.

(3) Write Inhibit Mode: Forcing #OE low, #CE high, or #WE high will inhibit the write operation. This prevents inadvertent writes during power-up or power-down periods.

(4) V_{DD} power-on delay: When V_{DD} has reached its sense level, the device will automatically time-out 10 mS before any write (erase/program) operation.

Data Polling (DQ_7)- Write Status Detection

The W49L401(T) includes a data polling feature to indicate the end of a program or erase cycle. When the W49L401(T) is in the internal program or erase cycle, any attempt to read DQ_7 of the last word loaded will receive the complement of the true data. Once the program or erase cycle is completed, DQ_7 will show the true data. Note that, DQ_7 will show logical "0" during the erase cycle. And it will become logical "1" or true data when the erase cycle is completed.

Toggle Bit (DQ_6)- Write Status Detection

In addition to data polling, the W49L401(T) provides another method for determining the end of a program cycle. During the internal program or erase cycle, any consecutive attempts to read DQ_6 will

produce alternating 0's and 1's. When the program or erase cycle is completed, this toggling between 0's and 1's will stop. The device is then ready for the next operation.

Ready/#Busy

The W49L401(T) also provides the hardware method to detect the completion of program/erase cycle . The RY/#BY output pin will be asserted low (busy) during programming/erasing operations, and will be released to high state by an external pull-up (ready) when internal program/erase cycle is completed. This is an open-drain output pin for easy external connection.

Product Identification

The product ID operation outputs the manufacturer code and device code. Programming equipment automatically matches the device with its proper erase and programming algorithms.

The manufacturer and device codes can be accessed by software or hardware operation. In the software access mode, a six-word (or JEDEC 3-word) command sequence can be used to access the product ID. A read from address 0000H outputs the manufacturer code, 00DA(hex). A read from address 0001(hex) outputs the device code, 003D(hex) for bottom boot (and TBD for top boot). The product ID operation can be terminated by a three-word command sequence or an alternative one-word command sequence (see Command Definition table).

In the hardware access mode, access to the product ID is activated by forcing #CE and #OE low, #WE high, and raising A9 to V_{HH} (12V $^{+}/_{-}$ 0.5V).

Table of Operating Modes

Operating Mode Selection

(V_{HH} = 12V ± 0.5V)

MODE	PINS					
	#CE	#OE	#WE	#RESET	ADDRESS	DQ.
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	A_{IN}	Dout
Erase/Program	V_{IL}	V_{IH}	V_{IL}	V_{IH}	A_{IN}	Din
Standby	V_{IH}	X	X	V_{IH}	X	High Z
Erase/Program Inhibit	V_{IH}	X	X	V_{IH}	X	High Z
	X	V_{IL}	X	V_{IH}	X	High Z/D_{OUT}
	X	X	V_{IH}	V_{IH}	X	High Z/D_{OUT}
Output Disable	X	V_{IH}	X	V_{IH}	X	High Z
Product ID	V_{IL}	V_{IL}	V_{IH}	V_{IH}	A0 = V_{IL}; A1–A15 = V_{IL}; A9 = V_{HH}	Manufacturer Code 00DA (Hex)
					A0 = V_{IH}; A1 – A15 = V_{IL}; A9 = V_{HH}	Device Code 003D (Hex) for bottom TBD for Top
Reset	X	X	X	V_{IL}	X	High Z

Table of Software Command Definition

COMMAND DESCRIPTION	NO. OF Cycles	1ST CYCLE		2ND CYCLE		3RD CYCLE		4TH CYCLE		5TH CYCLE		6TH CYCLE	
		Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Chip Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	10
Block Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	BA(5)	30
Page Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	PA(4)	50
Word Program	4	5555	AA	2AAA	55	5555	A0	A_{IN}	D_{IN}				
Boot Block Lockout	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	40
Product ID Entry	3	5555	AA	2AAA	55	5555	90						
Product ID Exit (1)	3	5555	AA	2AAA	55	5555	F0						
Product ID Exit (1)	1	XXXX	F0										

Notes:

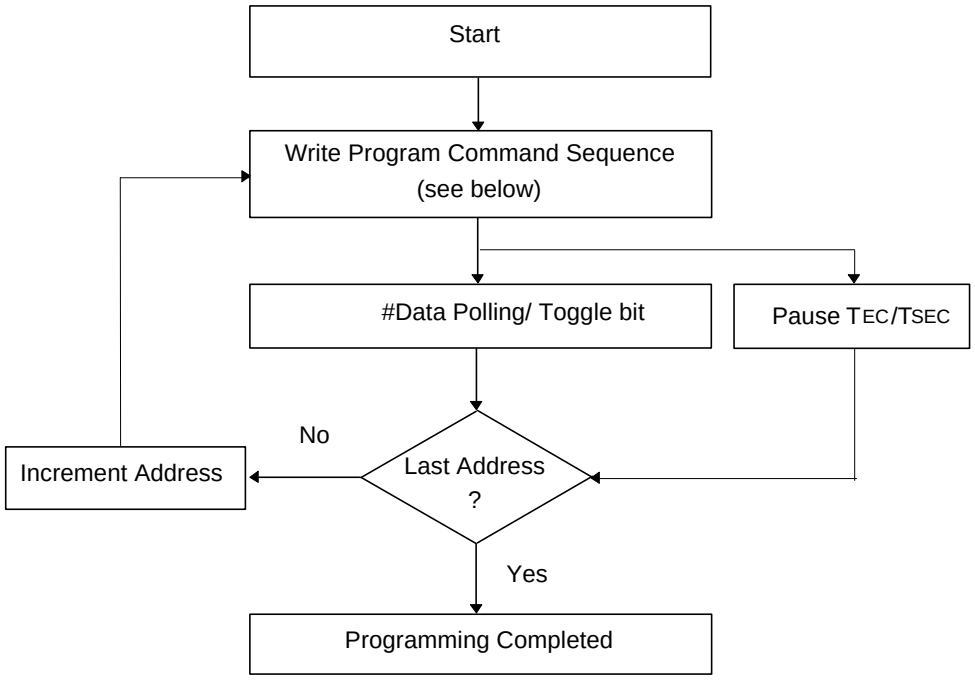
1. Address Format: A14 – A0 (Hex); Data Format: DQ15 – DQ8 (Don't Care); DQ7 – DQ0 (Hex)
2. If any invalid command or read cycle (both #CE & #OE are active low) is inserted during any of the above software command sequence, it will abort the operation and the device return to read mode.
3. Either one of the two Product ID Exit commands can be used, and Read mode is resumed after this command executed.
4. PA: Page Address

W49L401	W49L401T
PA = 00000h to 007FFh for Page0	PA = 3F800h to 3FFFFh for Page0
PA = 00800h to 00FFFh for Page1	PA = 3F000h to 3F7FFh for Page1
PA = 01000h to 017FFh for Page2	PA = 3E800h to 3EFFFh for Page2
PA = 01800h to 01FFFh for Page3	PA = 3E000h to 3E7FFh for Page3
PA = 02000h to 027FFh for Page4	PA = 3D800h to 3DFFFh for Page4
PA = 02800h to 02FFFh for Page5	PA = 3D000h to 3D7FFh for Page5
…	…
…	…
…	…
PA = 3D000h to 3D7FFh for Page122	PA = 02800h to 02FFFh for Page122
PA = 3D800h to 3DFFFh for Page123	PA = 02000h to 027FFh for Page123
PA = 3E000h to 3E7FFh for Page124	PA = 01800h to 01FFFh for Page123
PA = 3E800h to 3EFFFh for Page125	PA = 01000h to 017FFh for Page125
PA = 3F000h to 3F7FFh for Page126	PA = 00800h to 00FFFh for Page126
PA = 3F800h to 3FFFFh for Page127	PA = 00000h to 007FFh for Page127

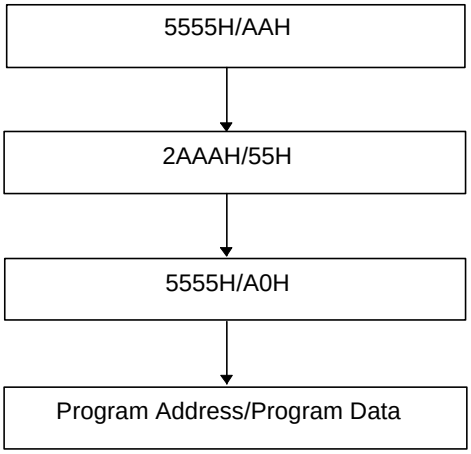
5. BA: Block Address

W49L401	W49L401T
BA = 00000h to 01FFFh for Boot Block (8KW)	BA = 3E000h to 3FFFFh for Boot Block (8KW)
BA = 02XXXh for Parameter Block1 (4KW)	BA = 3DXXXh for Parameter Block1 (4KW)
BA = 03XXXh for Parameter Block2 (4KW)	BA = 3CXXXh for Parameter Block2 (4KW)
BA = 04000h to 07FFFh for Main Memory Block1 (16KW)	BA = 38000h to 3BFFFh for Main Memory Block1 (16KW)
BA = 08000h to 0FFFFh for Main Memory Block2 (32KW)	BA = 30000h to 37FFFh for Main Memory Block2 (32KW)
BA = 10000h to 17FFFh for Main Memory Block3 (32KW)	BA = 28000h to 2FFFFh for Main Memory Block2 (32KW)
BA = 18000h to 1FFFFh for Main Memory Block4 (32KW)	BA = 20000h to 27FFFh for Main Memory Block3 (32KW)
BA = 20000h to 27FFFh for Main Memory Block5 (32KW)	BA = 18000h to 1FFFFh for Main Memory Block4 (32KW)
BA = 28000h to 2FFFFh for Main Memory Block6 (32KW)	BA = 10000h to 17FFFh for Main Memory Block5 (32KW)
BA = 30000h to 37FFFh for Main Memory Block7 (32KW)	BA = 08000h to 07FFFh for Main Memory Block7 (32KW)
BA = 38000h to 3FFFFh for Main Memory Block8 (32KW)	BA = 00000h to 07FFFh for Main Memory Block8 (32KW)

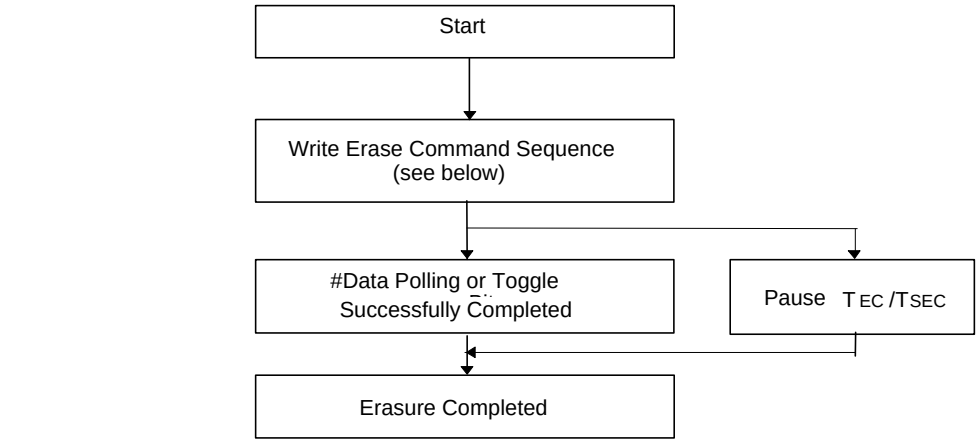
Embedded Programming Algorithm



Program Command Sequence (Address/Command):

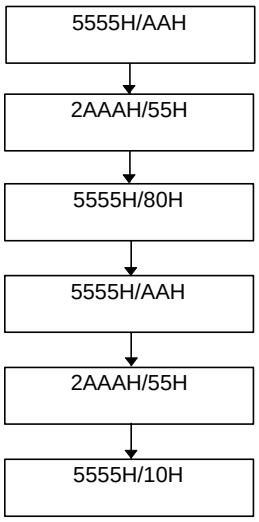


Embedded Erase Algorithm

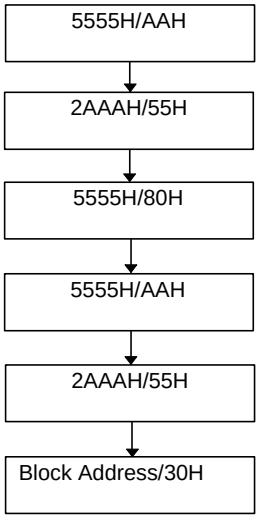


Chip Erase Command Sequence

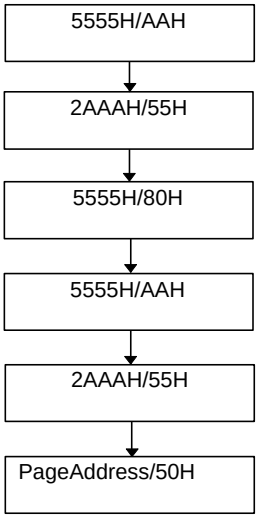
(Address/Command):



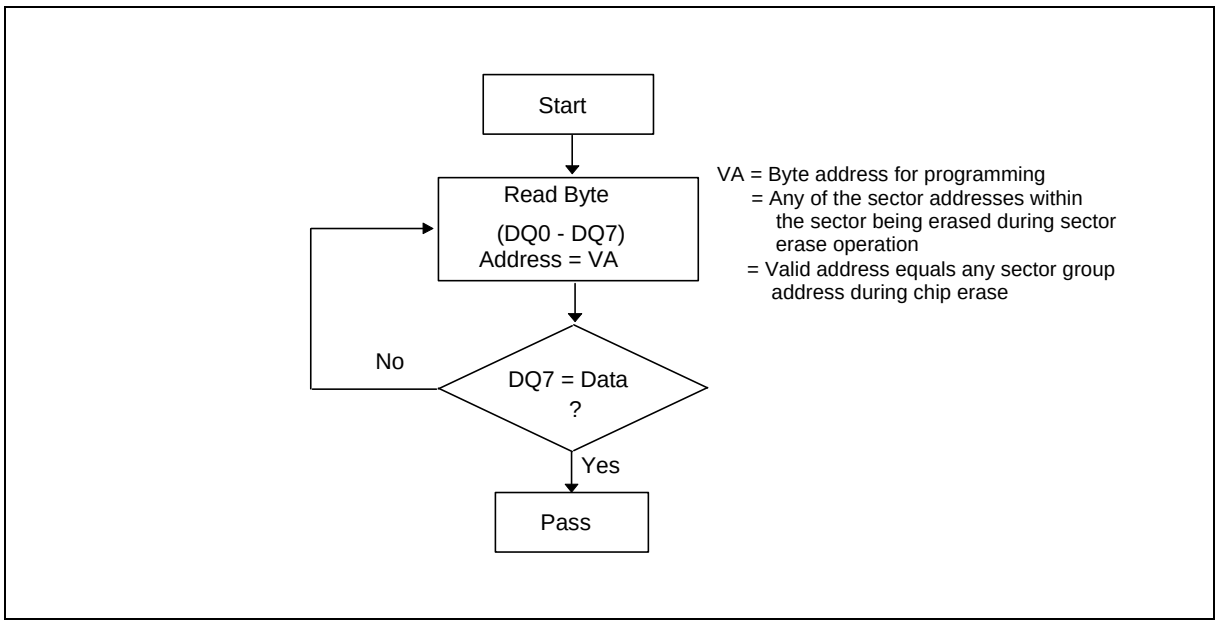
Individual BlockErase Command Sequence (Address/Command):



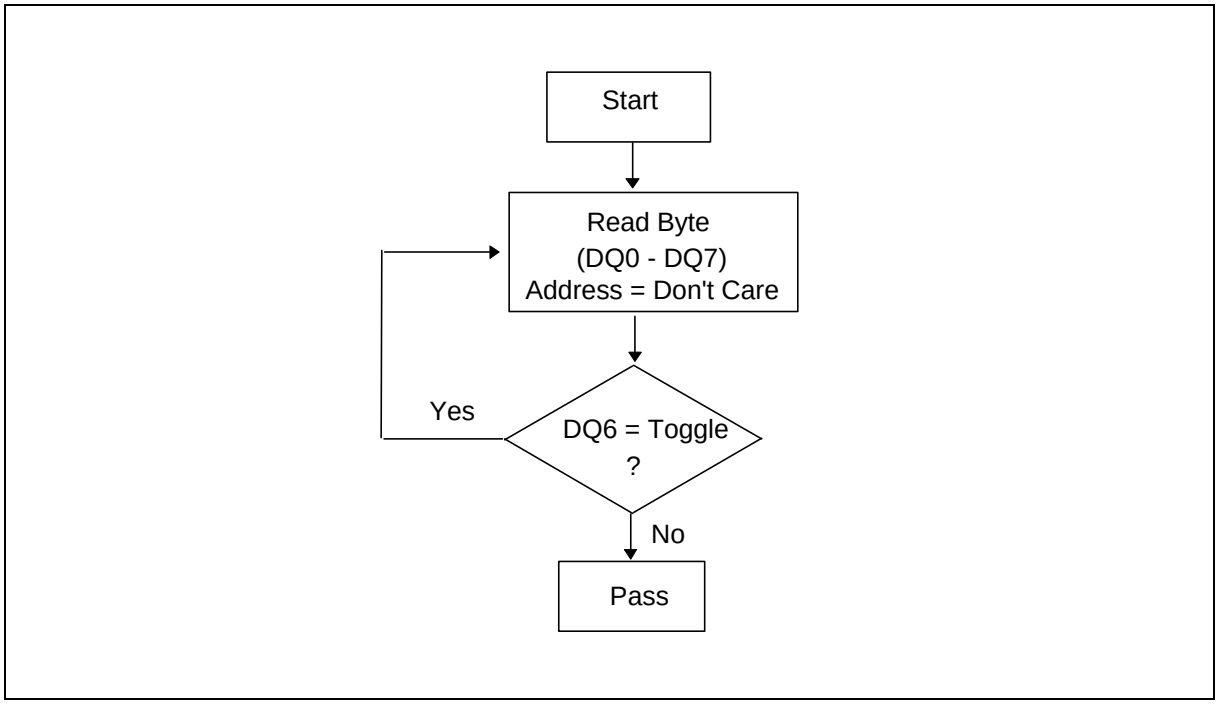
Individual PageErase Command Sequence (Address/Command):



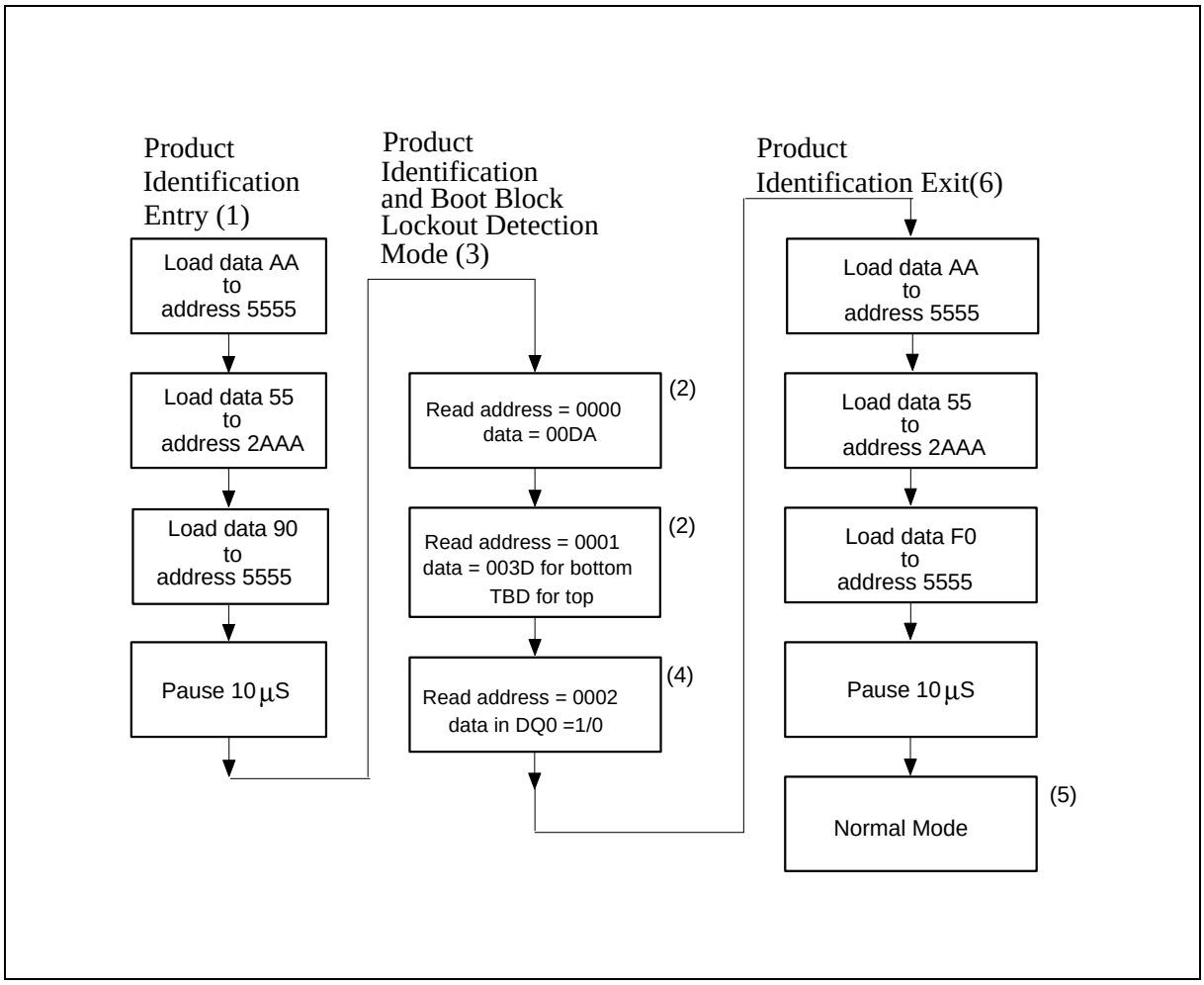
Embedded #Data Polling Algorithm



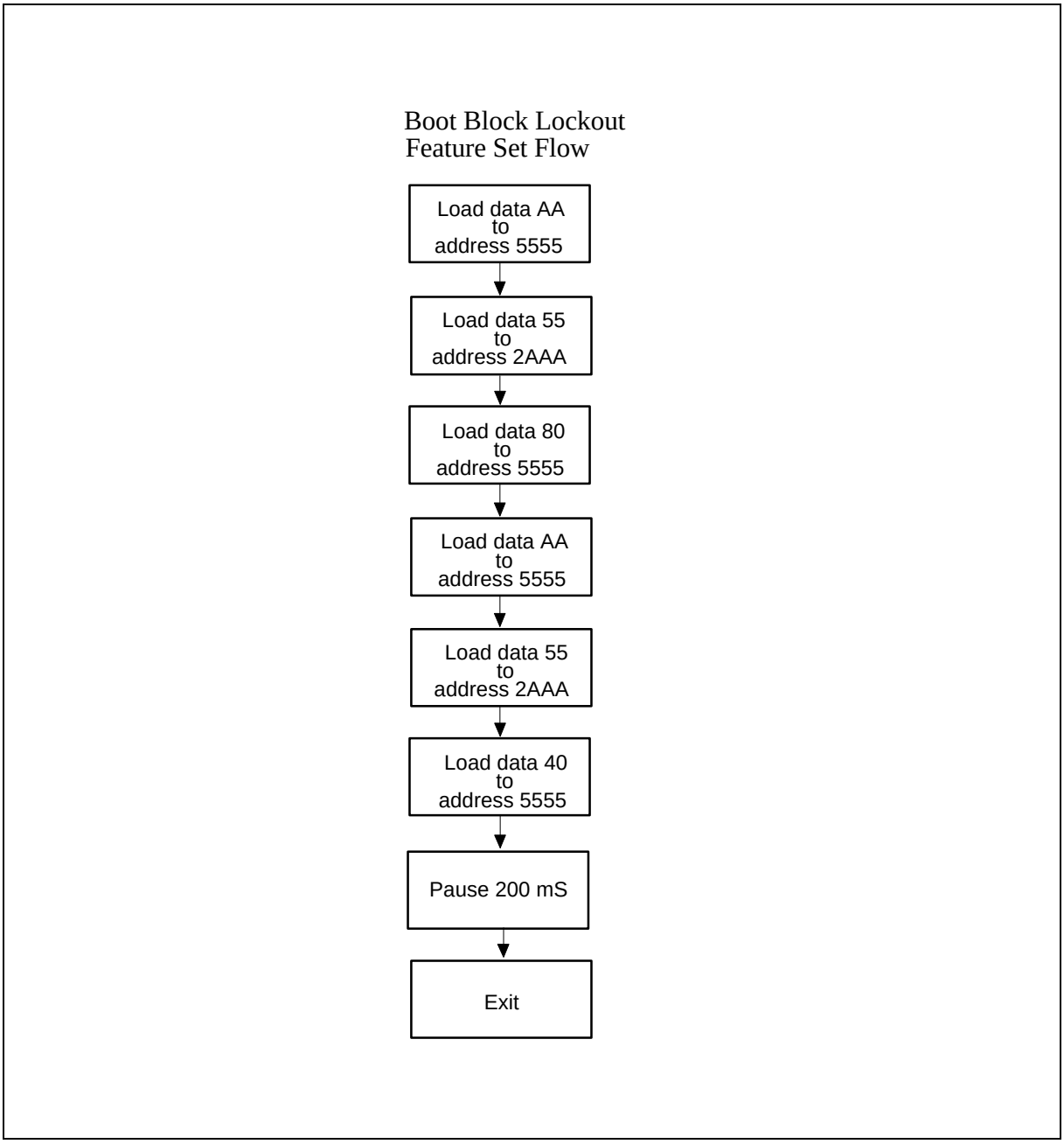
Embedded Toggle Bit Algorithm



Software Product Identification and Boot Block Lockout Detection Acquisition Flow



Boot Block Lockout Enable Acquisition Flow



7. DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage to V_{SS} Potential	-0.5 to +4.6	V
Operating Temperature	0 to +70	°C
Storage Temperature	-65 to +150	°C
D.C. Voltage on Any Pin to Ground Potential except A9 or #RESET	-0.5 to V_{DD} +1.0	V
Transient Voltage (<20 nS) on Any Pin to Ground Potential	-1.0 to V_{DD} +1.0	V
Voltage on A9 or #RESET Pin to Ground Potential	-0.5 to 12.5	V

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC Operating Characteristics

(V_{DD} = 3.0 ~ 3.6V, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
V_{DD} Current - Read	I_{CC}	#CE = #OE = V_{IL}, #WE = V_{IH}, all DQs open Address inputs = V_{IL}/V_{IH}, at f = 5 MHz	-	10	20	mA
V_{DD} Current - Write	I_{CCW}	#CE = #WE = V_{IL}, #OE = V_{IH}	-	15	25	mA
Standby V_{DD} Current (TTL input)	I_{SB1}	#CE = V_{IH}, all DQs open Other inputs = V_{IL}/V_{IH}	-	-	1	mA
Standby V_{DD} Current (CMOS input)	I_{SB2}	#CE = V_{DD} -0.3V, all DQs open Other inputs = V_{DD} -0.3V / V_{SS}	-	5	50	µA
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{DD}	-	-	10	µA
Output Leakage Current	I_{LO}	V_{OUT} = V_{SS} to V_{DD}	-	-	10	µA
Input Low Voltage	V_{IL}	-	-0.2	-	0.8	V
Input High Voltage	V_{IH}	-	2.0	-	V_{DD} +0.3	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA	-	-	0.45	V
Output High Voltage	V_{OH}	I_{OH} = -0.4 mA	2.4	-	-	V

Power-up Timing

PARAMETER	SYMBOL	TYPICAL	UNIT
Power-up to Read Operation	$T_{PU. READ}$	200	µS
Power-up to Write Operation	$T_{PU. WRITE}$	10	mS

Capacitance

(V_{DD} = 3.3V, T_A = 25° C, f = 1 MHz)

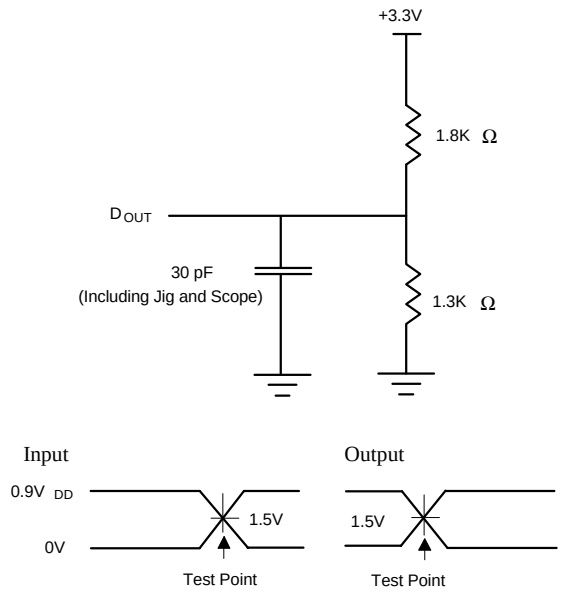
PARAMETER	SYMBOL	CONDITIONS	MAX.	UNIT
I/O Pin Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	12	pf
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pf

8. AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 0.9 V_{DD}
Input Rise/Fall Time	< 5 nS
Input/Output Timing Level	1.5V/1.5V
Output Load	1 TTL Gate and C_L = 30 pF

AC Test Load and Waveform



AC Characteristics, continued

Read Cycle Timing Parameters

(V_{DD} = 3.0 ~ 3.6V, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYMBOL	70 nS		UNIT
		MIN.	MAX.	
Read Cycle Time	T_{RC}	70	-	nS
Chip Enable Access Time	T_{CE}	-	70	nS
Address Access Time	T_{AA}	-	70	nS
Output Enable Access Time	T_{OE}	-	35	nS
#CE Low to Active Output	T_{CLZ}	0	-	nS
#OE Low to Active Output	T_{OLZ}	0	-	nS
#CE High to High-Z Output	T_{CHZ}	-	25	nS
#OE High to High-Z Output	T_{OHZ}	-	25	nS
Output Hold from Address Change	T_{OH}	0	-	nS

Note: The parameter of T_{CLZ}, T_{OLZ}, T_{CHZ}, T_{OHZ} are characterized only and is not 100% tested.

Write Cycle Timing Parameters

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Address Setup Time	T_{AS}	10	-	-	nS
Address Hold Time	T_{AH}	100	-	-	nS
#WE and #CE Setup Time	T_{CS}	10	-	-	nS
#WE and #CE Hold Time	T_{CH}	10	-	-	nS
#OE High Setup Time	T_{OES}	10	-	-	nS
#OE High Hold Time	T_{OEH}	0	-	-	nS
#CE Pulse Width	T_{CP}	100	-	-	nS
#WE Pulse Width	T_{WP}	100	-	-	nS
#WE High Width	T_{WPH}	50	-	-	nS
Data Setup Time	T_{DS}	100	-	-	nS
Data Hold Time	T_{DH}	10	-	-	nS
Word programming Time	T_{BP}	-	30	50	µS
Page Erase Cycle Time	T_{PEC}	-	25	50	mS
Block Erase Cycle Time	T_{BEC}	-	25	50	mS
Chip Erase Cycle Time	T_{EC}	-	100	200	mS

Note: All AC timing signals observe the following guidelines for determining setup and hold times:
(a) High level signal's reference level is V_{IH} and (b) low level signal's reference level is V_{IL}.

AC Characteristics, continued

Data Polling and Toggle Bit Timing Parameters

PARAMETER	SYM.	70 nS		UNIT
		MIN.	MAX.	
#OE to Data Polling Output Delay	TOEP	-	35	nS
#CE to Data Polling Output Delay	TCEP	-	70	nS
#WE High to #OE Low for Data Polling	TOEHP	100	-	nS
#OE to Toggle Bit Output Delay	TOET	-	35	nS
#CE to Toggle Bit Output Delay	TCET	-	70	nS
#WE High to #OE Low for Toggle Bit	TOEHT	100	-	nS

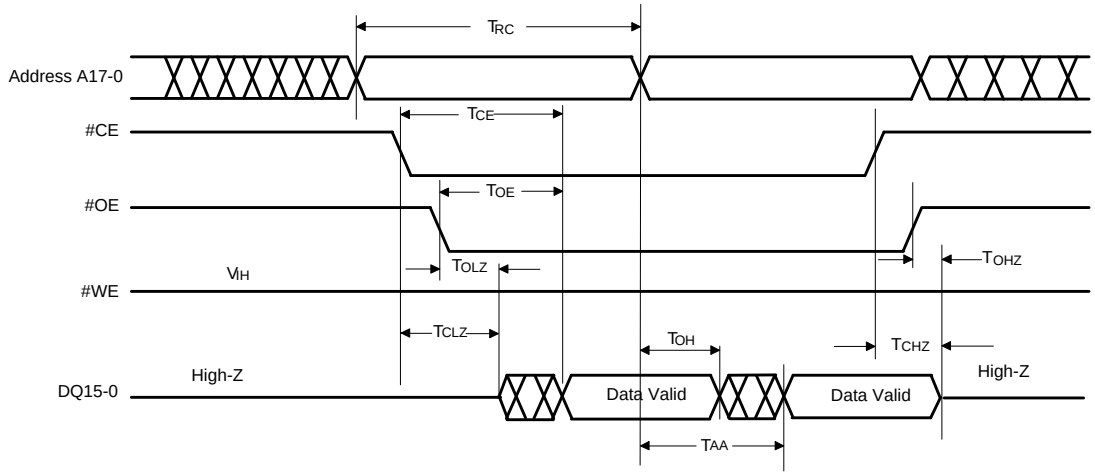
Hardware Reset Timing Parameters

PARAMETER	SYM.	MIN.	MAX.	UNIT
#RESET Pulse Width	TRP	500	-	nS
#RESET High Time Before Read (1)	TRH	50	-	µS

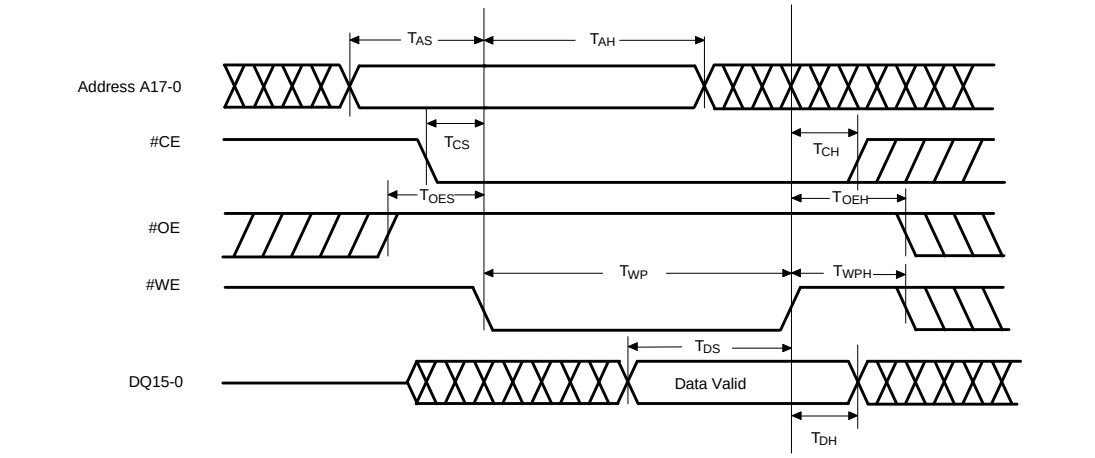
Note: 1. The parameters are characterized only and is not 100% tested.

9. TIMING WAVEFORMS

Read Cycle Timing Diagram

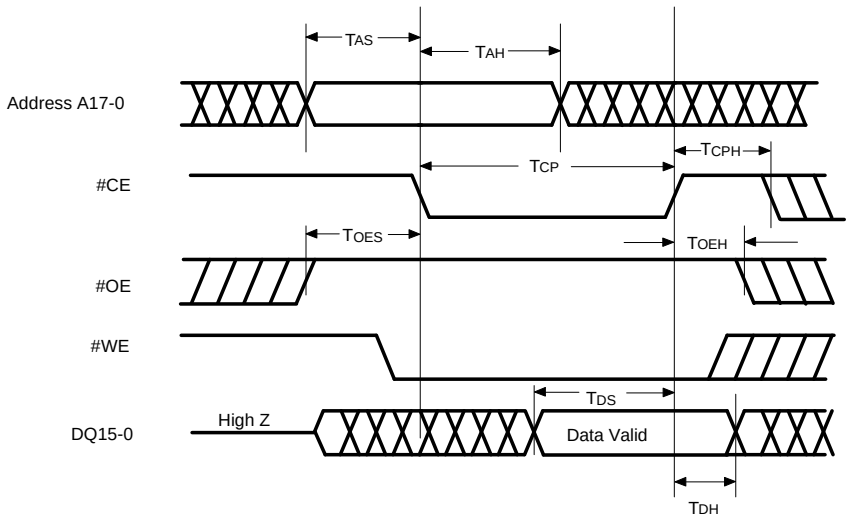


#WE Controlled Command Write Cycle Timing Diagram

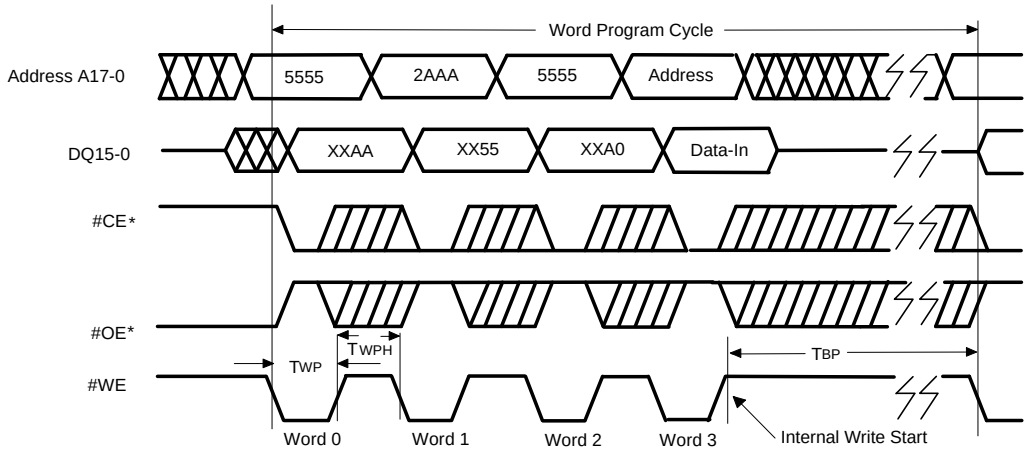


Timing Waveforms, continued

#CE Controlled Command Write Cycle Timing Diagram



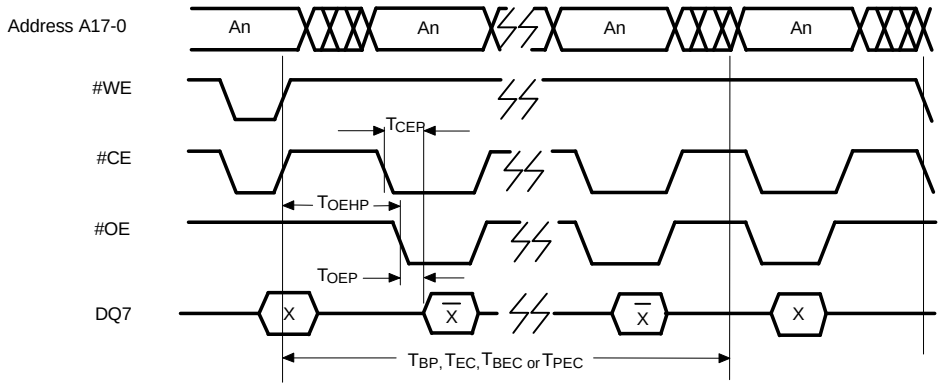
Program Cycle Timing Diagram



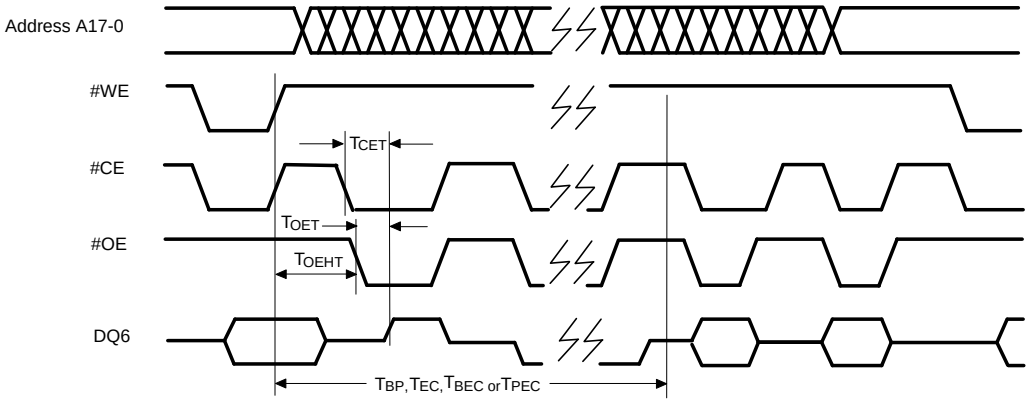
*Note: It is not allowed to assert read operation(#CE & #OE are both active) during the command sequence. If read command is asserted during the command sequence, then the device will return to read mode (abort write).

Timing Waveforms, continued

#DATA Polling Timing Diagram

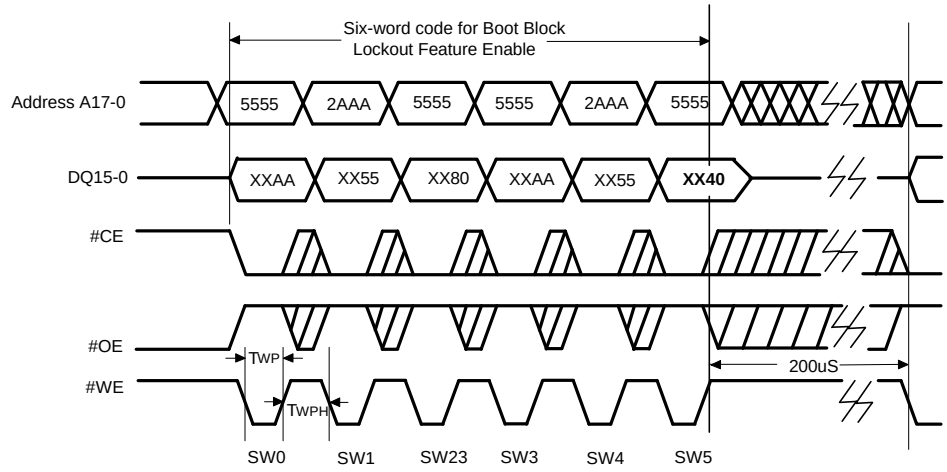


Toggle Bit Timing Diagram



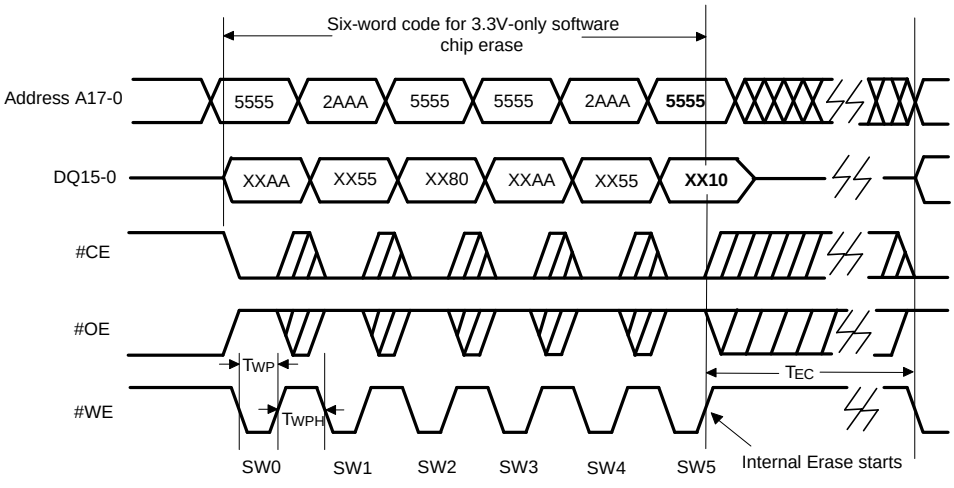
Timing Waveforms, continued

Boot Block Lockout Enable Timing Diagram



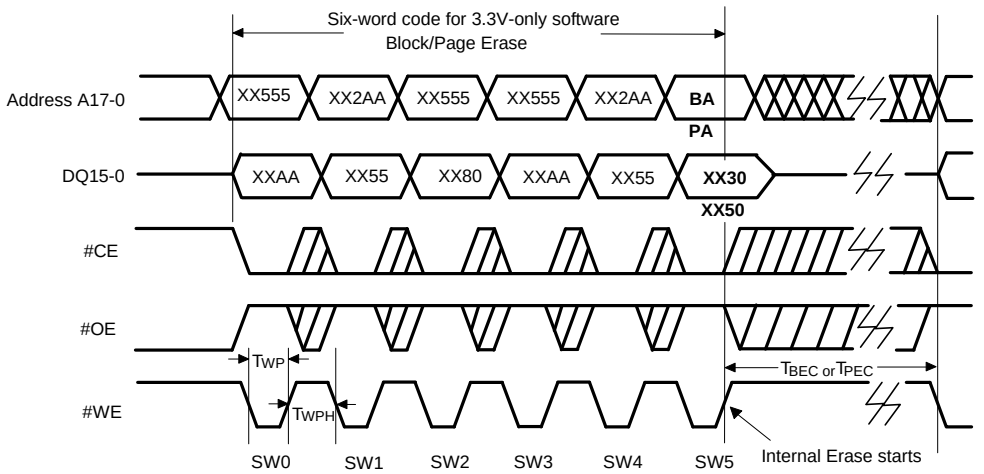
*Note: It is not allowed to assert read operation(#CE & #OE are both active) during the command sequence. If read command is asserted during the command sequence, then the device will return to read mode(abort write).

Chip Erase Timing Diagram



Timing Waveforms, continued

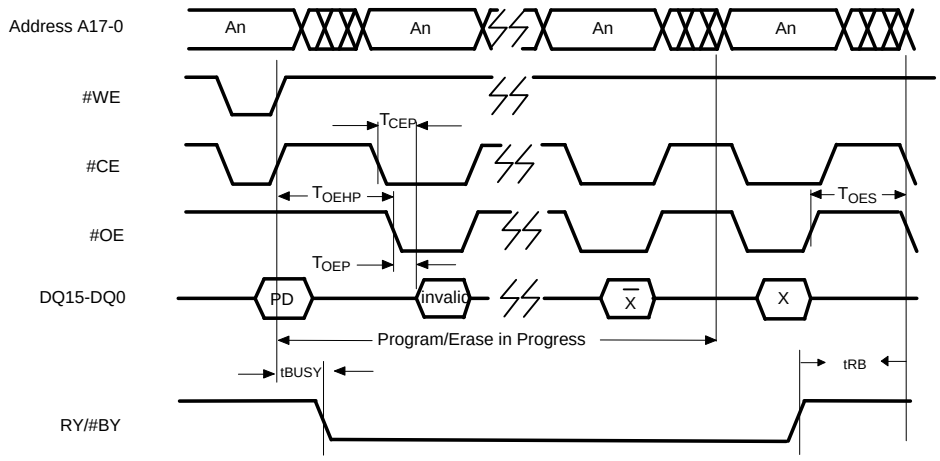
Block/Page Erase Timing Diagram



*Note: It is not allowed to assert read operation(#CE & #OE are both active) during command sequence. If read command is asserted during the comma sequence, then the device will return to read mode(abort wri

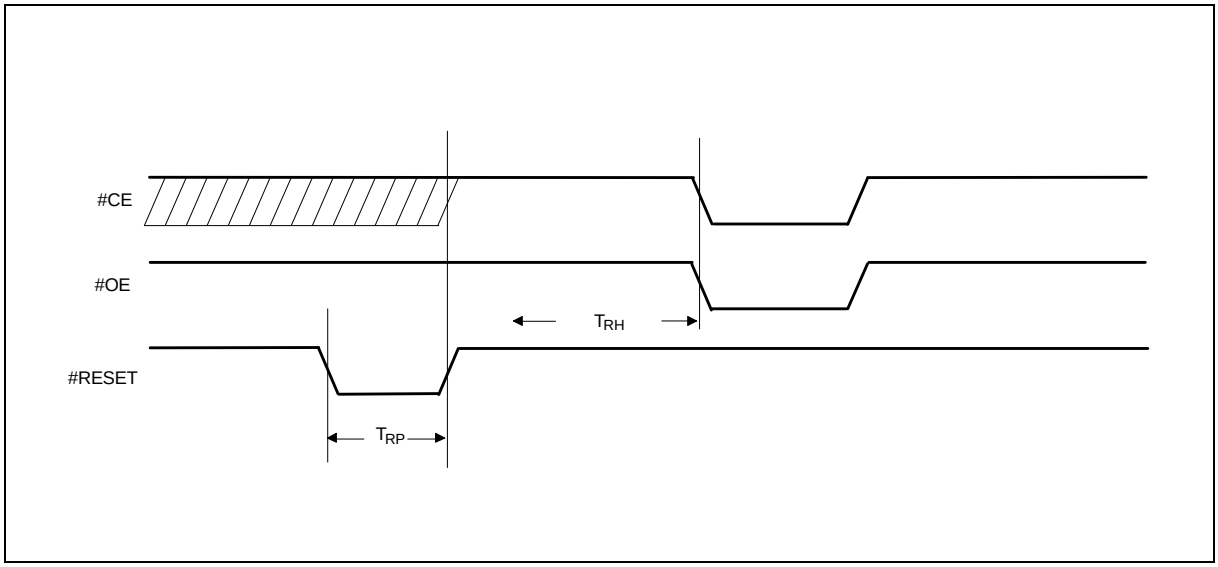
BA = Block Address; PA = Page Address

Ready/#Busy Timing Diagram



Timing Waveforms, continued

Reset Timing Diagram



10. ORDERING INFORMATION

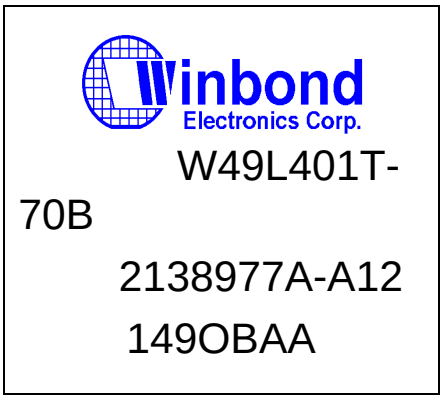
PART NO.	ACCESS TIME (nS)	OPERATING VOLTAGE (V)	BOOT BLOCK LOCATION	PACKAGE
W49L401S-70B	70	3.0 ~ 3.6	BOTTOM	44-pin SOP
W49L401T-70B	70	3.0 ~ 3.6	BOTTOM	48-pin TSOP (12 mm × 20 mm)
W49L401TS70B	70	3.0 ~ 3.6	TOP	44-pin SOP
W49L401TT70B	70	3.0 ~ 3.6	TOP	48-pin TSOP (12 mm × 20 mm)

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

11. HOW TO READ THE TOP MARKING

Example: The top marking of 48-pin TSOP W49L401T-70B



1st line: winbond logo

2nd line: the part number: W49L401T-70B

3rd line: the lot number

4th line: the tracking code: 149 O B AA

149: Packages made in 01, week 49

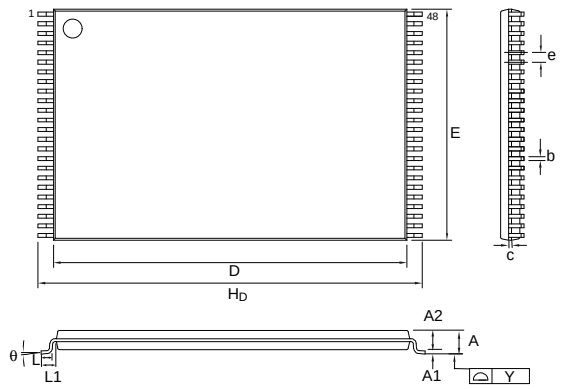
O: Assembly house ID: A means ASE, O means OSE, ... etc.

B: IC revision; A means version A, B means version B, ... etc.

AA: Process code

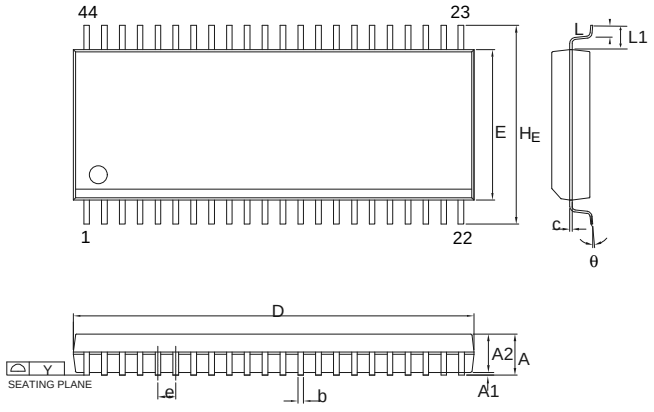
12. PACKAGE DIMENSIONS

48-pin TSOP (12 mm ´ 20 mm)



Symbol	Dimension in mm			Dimension in Inches		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.05	—	—	0.002	—	—
A2	0.95	1.00	1.05	0.037	0.039	0.041
D	18.3	18.4	18.5	0.720	0.724	0.728
H_D	19.8	20.0	20.2	0.780	0.787	0.795
E	11.9	12.0	12.1	0.468	0.472	0.476
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.10	—	0.21	0.004	—	0.008
e	—	0.50	—	—	0.020	—
L	0.50	0.60	0.70	0.020	0.024	0.028
L1	—	0.80	—	—	0.031	—
Y	—	—	0.10	—	—	0.004
θ	0	—	5	0	—	5

44-pin SOP



Symbol	Dimension in mm			Dimension in Inches		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	3.00	—	—	0.118
A1	0.10	—	—	0.004	—	—
A2	2.26	—	2.82	0.089		0.111
b	0.36	0.41	0.50	0.014	0.016	0.020
c	0.10	0.15	0.21	0.004	0.006	0.008
D	28.07	28.19	28.32	1.105	1.110	1.115
E	13.10	13.30	13.50	0.516	0.524	0.531
HE	15.80	16.00	16.20	0.622	0.630	0.638
e	1.12	1.27	1.42	0.044	0.050	0.056
L	0.60	0.80	1.00	0.024	0.032	0.040
L1	—	1.35	—	—	0.053	—
Y	—	—	0.10	—	—	0.004
θ	0	—	7	0	—	7

13. VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Apr. 2001	-	Initial Issued
A2	July 2001	18	Change T_{RH} from 50 nS to 10 µS
A3	January 2, 2002	1, 3, 6, 15	Delete the description of Auto-Power Saving
		18	Change T_{RH} from 10 µS to 30 µS (min.)
		17	Change T_{EC} from 200/1000 to 100/200 mS (typ./max.)
			Change T_{PEC}, T_{PBC} from 50/200 to 25/50 mS (typ./max.)
		1, 18, 19, 26	Delete read access time of 55 nS
		26	Add HOW TO READ THE TOP MARKING
		9, 10, 11, 12, 13	Delete old flow chart and add embedded algorithm
		4	Modify V_{DD} Power Up/Down Detection in Hardware Data Protection
		21	Modify Program Cycle Timing Diagram
A4	August 16, 2002	9 – 13	Modify Flow charts
		23	Modify Reset Timing Diagram

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