Digital color space converter

SAA7192A

FEATURES

- Input formatter with:
  - multiplexer
  - Y-delay line
  - Cr and Cb interpolating filters
- Conversion matrix (acc. to CCIR 601)
- Video look-up tables (provide gamma correction
- Pipeline delay line (horizontal reference signal)
- I²C-bus interface
- 883 compliant burn-in
- Extended temperature range testing
- ESD protection exceeds 2000V per MIL-STD-883 method 3015
- Available in low cost plastic package
- Package qualified per Philips standard package eval

GENERAL DESCRIPTION

The Digital Color Space Converter (DCSC) is a digital matrix which is used to transform 16/24-bit digital input signals, i.e., Y (luminance), Cr (color, R-Y) and Cb (color, B-Y), into an RGB 24-bit format in accordance with the CCIR-601 recommendations.

Accepting inputs from the different formats of the DMSD2 decoder family, the device has a constant propagation delay and a maximum data rate of 16 MHz. A matched pipeline delay line is available to permit the HREF signal to be synchronized with the video data at the output.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{DO}	Supply voltage	–0.5	7	V
VI	input voltage	–0.5	7	V
VO	output voltage	–0.5	7	V
P_{TOT}	total	–	1.5	W
T_{STG}	storage temperature range	–65	+150	C
T_{AMB}	operating ambient temperature	–40	+125	C

ORDERING INFORMATION

Description	Order Code
68-pin plastic leaded chip carrier	SAA7192A/AA68A

BLOCK DIAGRAM

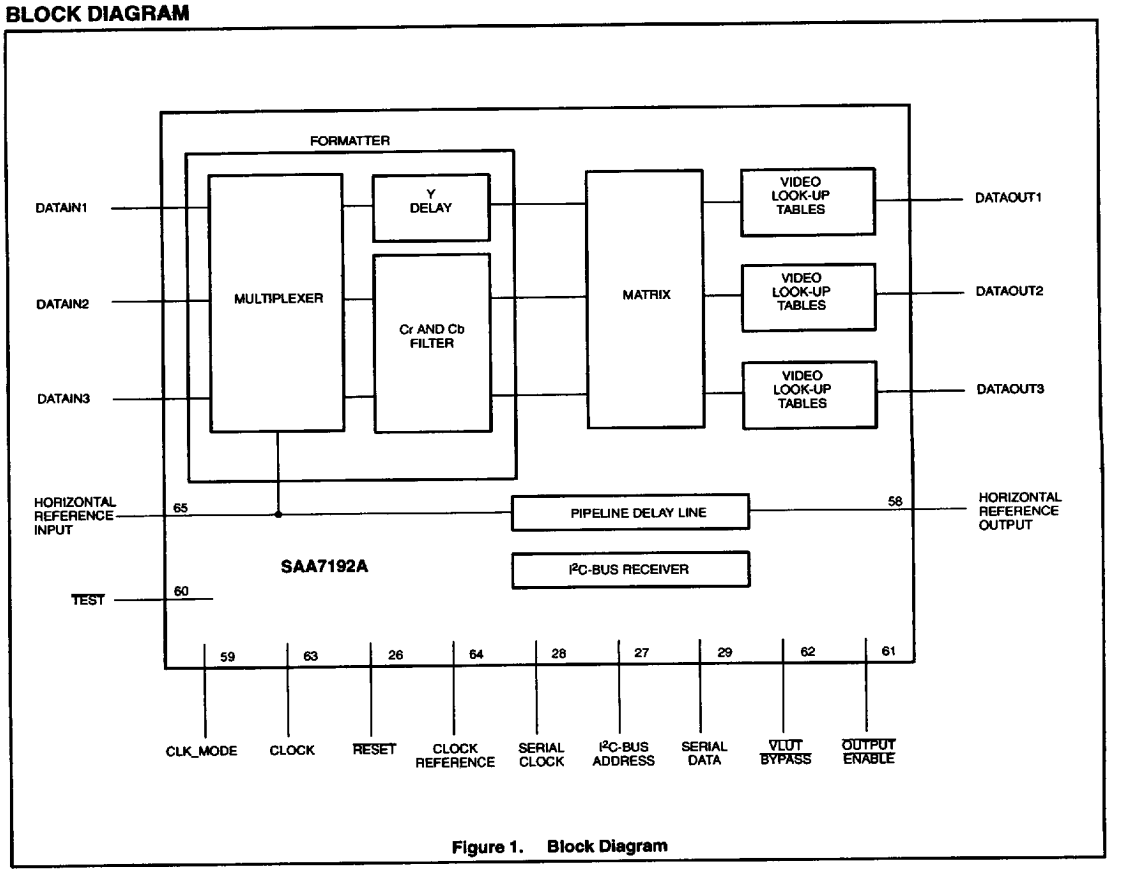


Figure 1. Block Diagram

PIN CONFIGURATION

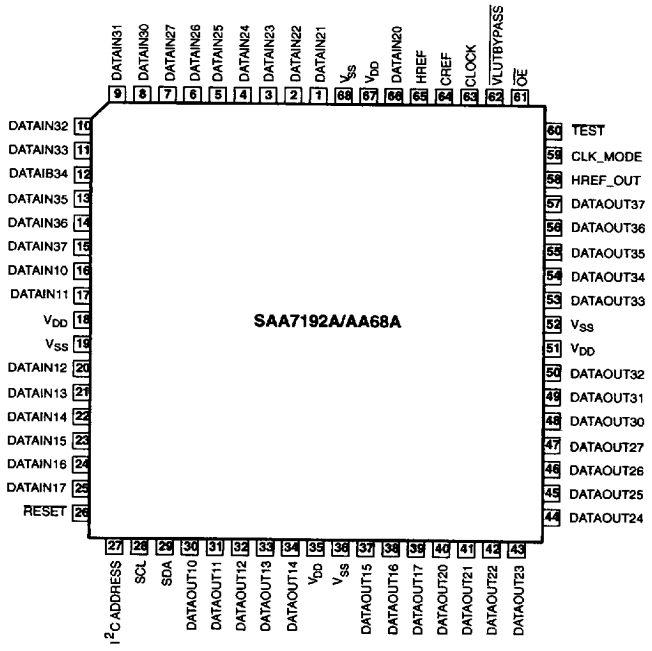


Figure 2. Pin configuration

PINNING

SYMBOL	PIN	DESCRIPTION
DATAIN (10-17)	16-17 and 20-25	luminance signal Y (0-7)
DATAIN (20-27)	1-7 and 66	color difference signal Cr (0-7)
DATAIN (30-37)	8-15	color difference signal Cb (0-7) or multiplexed Cb and Cr
DATAOUT (10-17)	30-34 and 37-39	RED (0-7)
DATAOUT (20-27)	40-47	GREEN (0-7)
DATAOUT (30-37)	48-50 and 53-57	BLUE (0-7)
$\overline{\text{RESET}}$	26	Initially resets the functions
HREF_OUT	58	delayed horizontal reference signal
CLK_MODE	59	16MHz or DMSD clock mode selection
$\overline{\text{TEST}}$	60	test mode, usually not connected
$\overline{\text{OE}}$	61	output enable (fast switch)
$\overline{\text{VLUTBYPASS}}$	62	fast switch to operate the VLUTs in bypass
CLOCK	63	system clock
CREF	64	clock reference signal (DMSD mode)
HREF	65	horizontal reference signal
V_{DD}	18, 67 35, 51	positive supply, voltage core (+5V) positive supply voltage, output stages (+5V)
V_{SS}	19, 68 36, 52	negative supply, voltage core (ground) negative supply, output stages
I^2C-bus ADDRESS	27	I^2C-bus SLAVE ADDRESS selection
SCL	28	I^2C-bus SERIAL CLOCK input
SDA	29	I^2C-bus SERIAL DATA input

NOTE:
All DATAIN and DATAOUT busses count from 0 (LSB) to 7 (MSB).

Table 1. Functional modes

MODE	FUNCTION
1	4:1:1 filter, no matrix, no VLUT; DATAOUT = upsampled DATAIN
2	4:1:1 filter, matrix, no VLUT; DATAOUT = RGB
3	4:1:1 filter, no matrix, VLUT; DATAOUT = upsampled DATAIN multiplied by the factor loaded into the VLUT
4	4:1:1 filter, matrix, VLUT; DATAOUT = RGB multiplied by the factor loaded into the VLUT
5	4:2:2 filter, no matrix, no VLUT; DATAOUT = upsampled DATAIN
6	4:2:2 filter, matrix, no VLUT; DATAOUT = RGB
7	4:2:2 filter, no matrix, VLUT; DATAOUT = upsampled DATAIN multiplied by the factor loaded into the VLUT
8	4:2:2 filter, matrix, VLUT; DATAOUT = RGB multiplied by the factor loaded into the VLUT
9	no filter, no matrix, no VLUT; DATAOUT – DATAIN "Process Bypass"
10	no filter, no matrix, no VLUT; DATAOUT = RGB
11	no filter, no matrix, VLUT; DATAOUT = DATAIN multiplied by the factor loaded into the VLUT
12	no filter, no matrix, VLUT; DATAOUT = RGB multiplied by the factor loaded into the VLUT

NOTE:
Figures 3 to 10 illustrate the various functional modes.

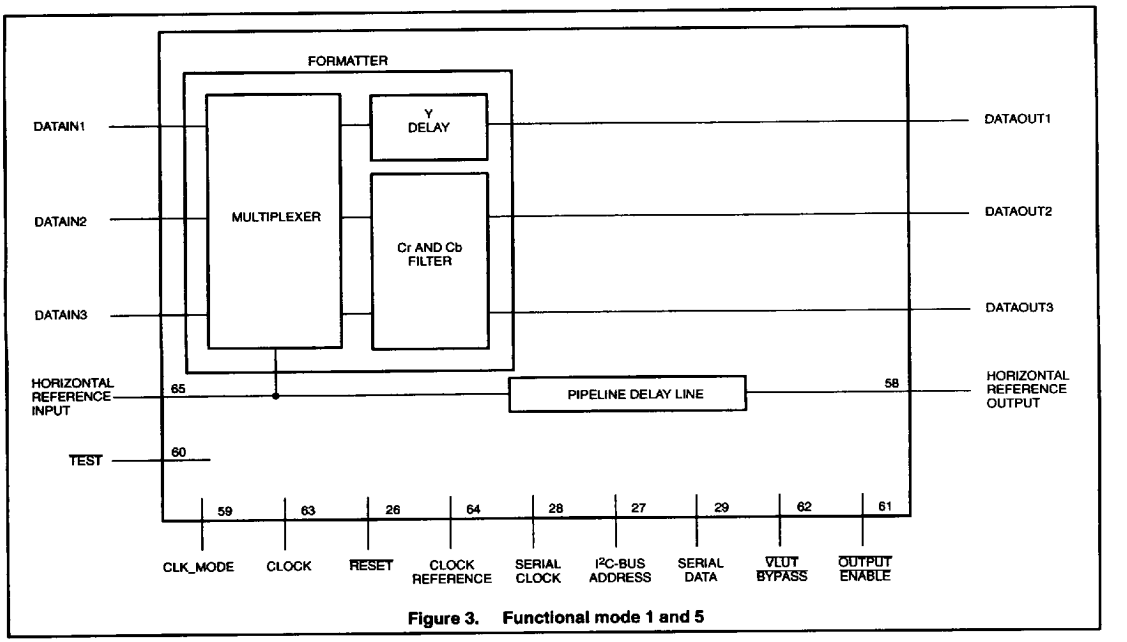


Figure 3. Functional mode 1 and 5

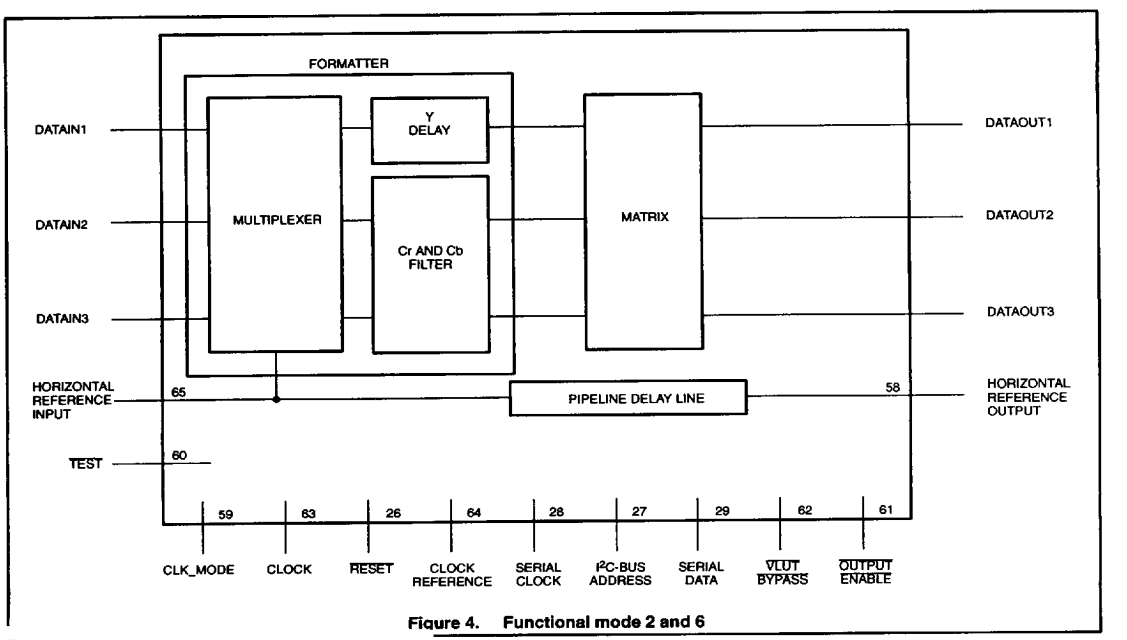


Figure 4. Functional mode 2 and 6

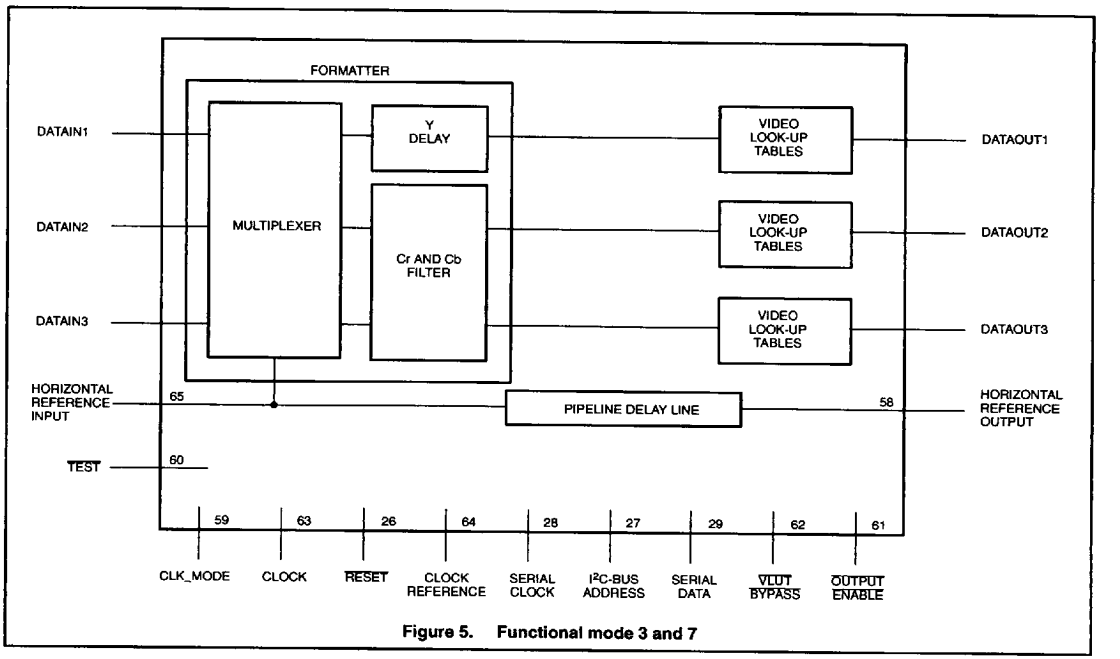


Figure 5. Functional mode 3 and 7

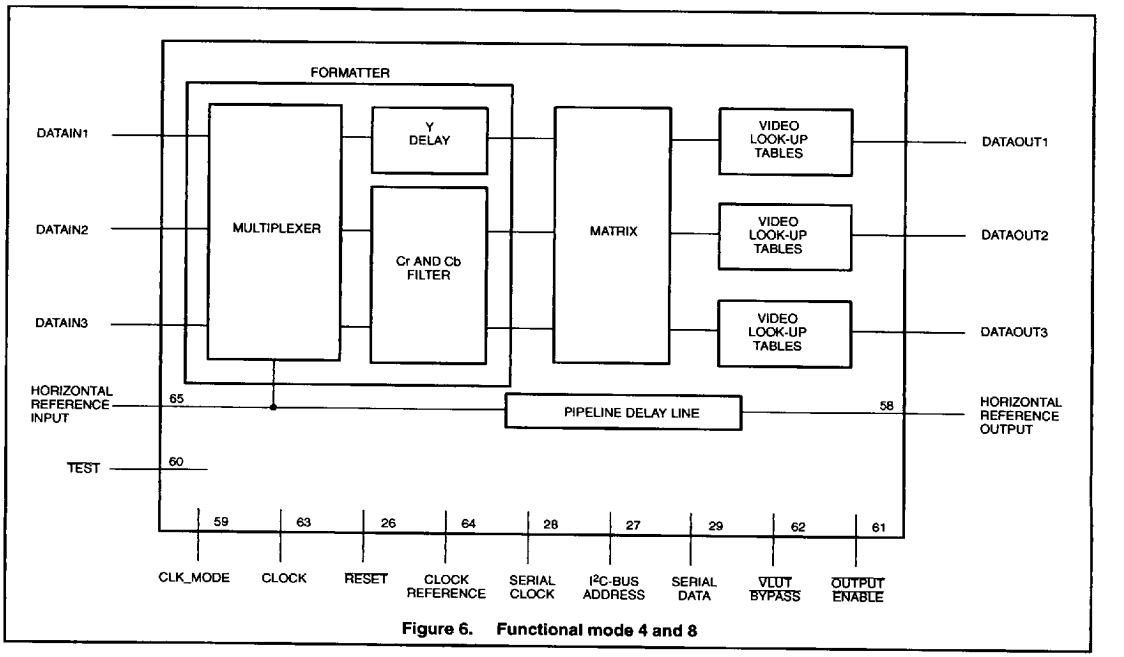


Figure 6. Functional mode 4 and 8

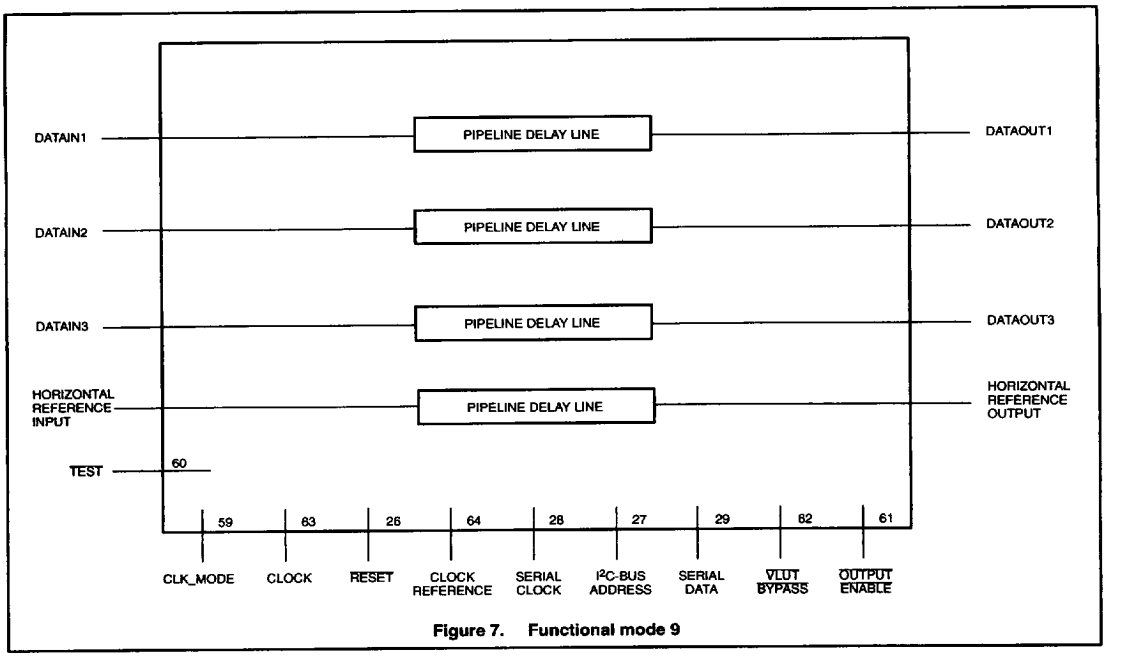


Figure 7. Functional mode 9

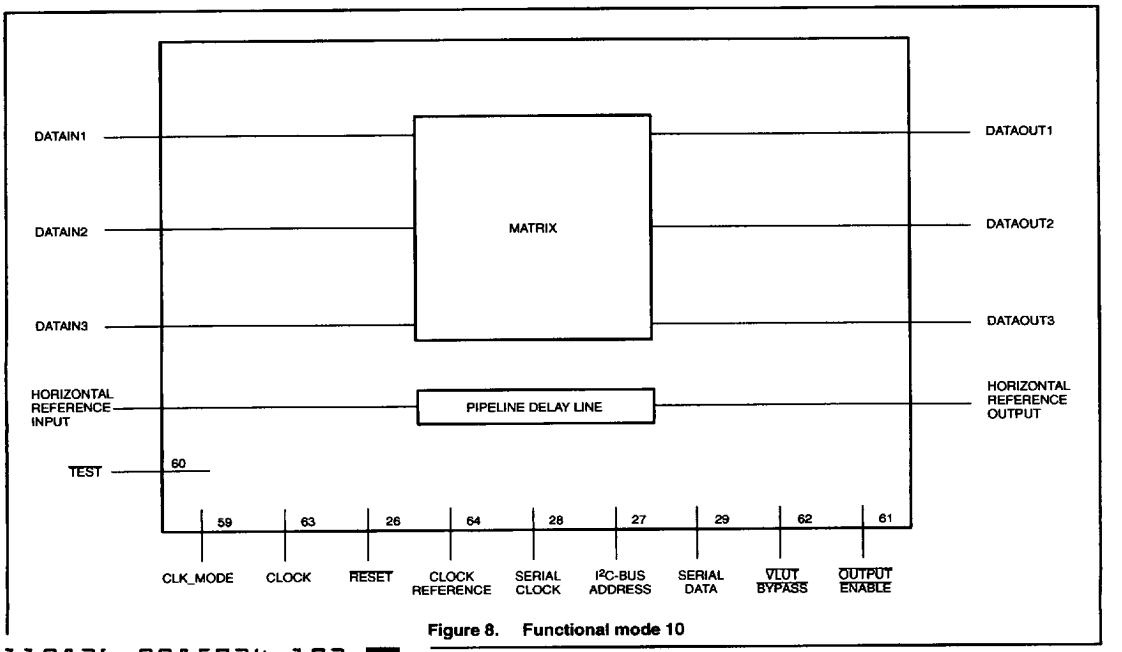


Figure 8. Functional mode 10

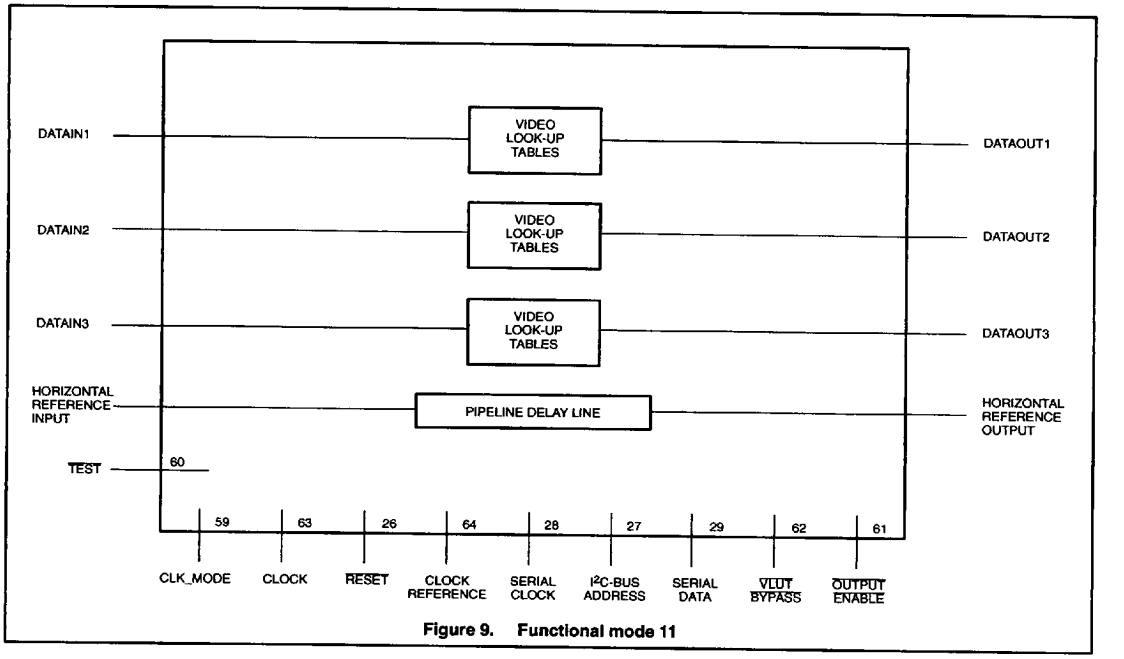


Figure 9. Functional mode 11

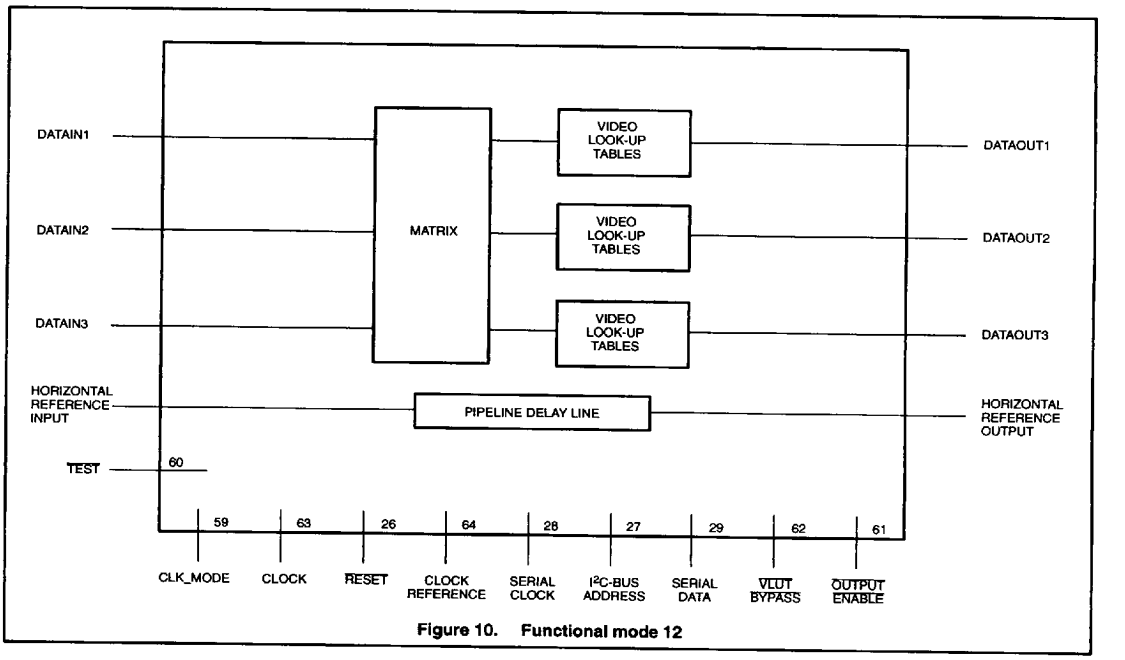


Figure 10. Functional mode 12

CONTROL FACILITIES

After power-up all device internal control signals are at undefined values. The I²C-bus receiver must, therefore, be reset by using the external RESET signal

Table 2. I²C-bus control signals (subadd 00H) after an external RESET is received

SYMBOL	BIT	STATUS
IICOE	D5	= 1 ; $\overline{OE}$ pin 61 enabled
FMTCNTRL	D0-D2	= 4 ; format 4:4:4
$\overline{MATBYPASS}$	D3	= 0 ; matrix by-passed
$\overline{INRESET}$	D4	= 0 ; input data set to fixed values

Table 3. Input formats and functional modes

FMTCNTRL	$\overline{MATBYPASS}$	$\overline{VLUTBYPASS}$	FUNCTIONS
000	0	0	mode 1, input format 1 (DMSD2 format)
000	1	0	mode 2, input format 1 (DMSD2 format)
001	0	0	mode 1, input format 2
001	1	0	mode 2, input format 2
010	0	0	mode 5, input format 3 (DMSD2 format)
010	1	0	mode 6, input format 3 (DMSD2 format)
011	0	0	mode 5, input format 4 (parallel IN)
011	1	0	mode 6, input format 4 (parallel IN)
100	0	0	mode 9, input format 5 (parallel IN)
100	1	0	mode 10, input format 5 (parallel IN)
X	X	1	each of the above described modes will be multiplied by the factor loaded into the VLUT.

NOTE:
The modes are given in Table 1.

Then other control signals are:

INRESET	=	logic 1	:	input latches at the formatter are always transparent
	=	logic 0	:	at the end of each active video line the input latches have to be set to fixed values (Y to 16; Cr and Cb to 128; if HREF = 0)
CLK_MODE	=	logic 1	:	DMSD mode (LL27 clock of DMSD feeds the DCSC)
	=	logic 0	:	DCSC is fed by a maximum 16 MHz clock without CREF signal.

Table 4. Output enable control

IICOE	$\overline{OE}$	CONTROL LINE TO DRIVER STAGES
0	X	1 = DATAOUT in high impedance mode
1	1	1 = DATAOUT in high impedance mode
1	0	0 = DATAOUT working

NOTES:
1. IICOE : D5; output enable control of I^2C-bus (enables $\overline{OE}$)
2. OE : pin 61; output enable (fast switch)

SYSTEM I/O INTERFACES

Input signals

Table 5. Format 0 (4:1:1, semi-parallel, DMSD2 decoder family format)

DATAIN1 - Y	luminance signal, 8 bit
sampling frequency	12 to 16 MHz
Level	0 IRE; black, quantization level 16 100 IRE; white, quantization level 235
DATAIN3 - U, V	multiplexed color difference signals 4-bit; corresponds to UV7 to UV4 of DMSD2
Sampling frequency	1/4 of the Y signal
Level	bottom peak; quantization level 16 top peak; quantization level 240 colorless; quantization level 128
DATAIN2	not used

Table 6. Timing of Format 0; pin (DATAIN) and bit (U,V) numbers are indicated except clock

Y; 7 to 0	Y	Y	Y	Y	Y	Y	Y
DATAIN 37	U7	U5	U3	U1	U7	U5	U3
DATAIN 36	U6	U4	U2	U0	U6	U4	U2
DATAIN 35	V7	V5	V3	V1	V7	V5	V3
DATAIN 34	V6	V4	V2	V0	V6	V4	V2
Clock A	1	2	3	4	5	6	7

NOTE:
Clock_A is the internal sampling clock of the system. The clock rate of the DMSD and the DCSC is twice that of Clock_A in this mode.

Table 7. Format 1 (4:1:1, semi-parallel, customized format)

DATAIN1 - Y	luminance signal; 8-bit
Sapling frequency	12 to 16 MHz
Level	0 IRE; black; quantization level 16 100 IRE; white; quantization level 235
DATAIN3 - Cr, Cb	multiplexed color difference signals, 8 bit
Sampling frequency	1/4 of the Y signal
Level	bottom peak; quantization level 16 top peak; quantization level 240 colorless; quantization level 128
DATAIN2	not used

Table 8. Timing of Format 1; the indices show the clock (sample) number

Y	Y0	Y1	Y2	Y3	Y4	Y5	Y6
Cr, Cb	Cb0		Cr0		Cb4		Cr4
Clock A	0	1	2	3	4	5	6

NOTE:
Clock_A is the internal sampling clock of the system. The external CLOCK may differ from the CLK_MODE.

Table 9. Format 2 (4:2:2, semi-parallel, DMSD2 format)

DATAIN1 - Y	luminance signal; 8-bit
Sampling frequency	12 to 16 MHz
Level	0 IRE; black; quantization level 16 100 IRE; white; quantization level 235
DATAIN3 - Cr, Cb	multiplexed color difference signals, corresponds to UV7 to UV0 of DMSD2
Sampling frequency	1/2 of the Y signal
Level	bottom peak; quantization level 16 top peak; quantization level 240 colorless; quantization level 128
DATAIN2	not used

Table 10. Timing of Format 2

Y	Y0	Y1	Y2	Y3	Y4	Y5	Y6
Cr, Cb	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4	CB6
Clock A	0	1	2	3	4	5	6

NOTE:
Clock_A is the internal sampling clock of the system. The clock of the DMSD (also the clock of the DCSC) is twice that of Clock_A in this mode.

Table 11. Format 3 (4:2:2, Y-Cr-Cb, parallel)

DATAIN1 - Y	luminance signal; 8-bit
Sampling frequency	12 to 16 MHz
Level	0 IRE; black; quantization level 16 100 IRE; white; quantization level 235
DATAIN3 - Cb	color difference signal B-Y, 8-bit
Sampling frequency	1/2 of the Y signal
Level	bottom peak; quantization level 16 top peak; quantization level 240 colorless; quantization level 128
DATAIN2 - Cr	color difference signal R-Y, 8 bit
Sampling frequency	1/2 of the Y signal
Level	bottom peak; quantization level 16 top peak; quantization level 240 colorless; quantization level 128

Table 12. Timing of Format 3

Y	Y0	Y1	Y2	Y3	Y4	Y5	Y6
Cb	Cb0		Cb2		Cb4		CB6
Cr	Cr0		Cr2		Cr4		Cr6
Clock A	0	1	2	3	4	5	6

NOTE:
Clock_A is the internal sampling clock of the system. The external CLOCK may differ from the CLK_MODE.

Table 13. Format 4 (4:4:4, Y-Cr-Cb, parallel)

DATAIN2 - Cr	color difference signal R-Y, 8-bit
Sampling frequency	as the Y signal
Level	bottom peak; quantization level 16 top peak; quantization level 240 colorless; binary 128
DATAIN3 - Cb	color difference signal B-Y, 8-bit
Sampling frequency	as the Y signal
Level	bottom peak; quantization level 16 top peak; quantization level 240 colorless; quantization level 128
DATAIN1 - Y	luminance signal; 8 bit
Sampling frequency	12 to 16 MHz
Level	0 IRE; black; quantization level 16 100 IRE; white; quantization level 235

VIDEO DATA (DATAIN)

Table 14. Timing of Format 4

Y	Y0	Y1	Y2	Y3	Y4	Y5	Y6
Cb	Cb0	Cb1	Cb2	Cb3	Cb4	Cb5	CB6
Cr	Cr0	Cr1	Cr2	Cr3	Cr4	Cr5	Cr6
Clock A	0	1	2	3	4	5	6

NOTE:
Clock_A is the internal sampling clock of the system. The external CLOCK may differ from the CLK_MODE.

CONTROL DATA

Clock

The CLK-Mode signal is used to select the frequency of the system clock (denoted as CLOCK at the DCSC input) and may be chosen from two different Clock Modes.

16 MHz-Mode:
DCSC is used in any environment except that of the DMSD2 decoder family. The clock reference signal (CREF) is internally set HIGH in value.

The maximum CLOCK frequency is 16 MHz.

DMSD-Mode:
DCSC is used in a DMSD environment.

The CLOCK signal (LL27) and the CREF signal are fed by the clock generator circuit (SAA7157/SAA7197) and the line locked LL27 (denoted as CLOCK at the DCSC input) is twice the data rate of that specified for the DMSD2 family of decoders. The data rate is denoted as CLOCK_A in Tables 6, 8, 10, 12 and 14.

The data rate on the input (DATAIN) is as follows:

12.2727 MHz; 60 Hz signals (from SAA7191)
13.5 MHz; CCIR signals (from SAA7151)
14.75 MHz; 50 Hz signals (from SAA7191)
16.0 MHz; maximum frequency

Timing reference
The timing reference signal from the SAA7151/7191 is used to synchronize the multiplexer and refers to the LL27 clock. Each alternative positive slope, marked by a CREF signal, is used to obtain data.

The horizontal reference signal, HREF, indicates the active part of a line and also synchronizes the multiplexer.

CREF The clock reference signal is a clock qualifier signal distributed by the clock generator of the DMSD system. The frequency is identical to the sample rates denoted in the input and the output formats (see Video data and Operating conditions).

HREF Horizontal reference signal is the line reference signal of the YUV-bus. A positive slope marks the beginning of the active part of a line. The length of the active part corresponds to the number of samples (see Operating conditions).

Table 15. Real-time control signals

$\overline{OE}$	pin 61	= 1 :	switches the output to high-z mode
		= 0 :	output enable, output stage in use
$\overline{VLUTBYPASS}$	pin 62	= 1 :	VLUT's in use
		= 0 :	VLUT's bypassed
$\overline{RESET}$	Pin 26	= 1 :	device in use
		= 0 :	general reset
CLK_MODE	pin 59	= 1 :	DMSD mode (LL27 clock of DMSD feeds the DCSC)
		= 0 :	DCSC is fed by a clock signal with a maximum data rate of 16 MHz (without CREF signal).

Table 16. I²C-bus controls (sub-add. VLUTDATA)

VLUTDATA	SUB-ADD
RAM 1 (RED)	01H
RAM 2 (GREEN)	02H
RAM 3 (BLUE)	03H
RAM 1, 2, 3	04H

NOTE:
See also example of VLUT programming Figure 23.

Table 17. I²C-bus controls (sub-add. 00H)

FMTCNTRL	D0-D2	= 000 :	4:1:1 format, dmsd2 format
		= 001 :	4:1:1 format, customized format
		= 010 :	4:2:2 format, from DMSD2
		= 011 :	4:2:2 format, parallel
		= 100 :	4:4:4 format, parallel
		= 101 :	not used
		= 110 :	not used
		= 111 :	not used
$\overline{MATBYPASS}$	D3	= 1 :	matrix in use
		= 0 :	matrix bypassed
$\overline{INRESET}$	D4	= 1 :	input latches at the formatter are always transparent
		= 0 :	at the end of each active video line the input latches have to be set to fixed values (Y to 16; Cr, Cb to 128; if HREF = 0)
IICOE		D5 = 1 :	$\overline{OE}$ enabled
		= 0 :	switches the output to high impedance mode

OUTPUT SIGNALS

Video data

Table 18. Timing of DATAOUT (R-G-B if matrix in use)

Timing: the indices show the clock sample number							
DATAOUT1 :	R0	R1	R2	R3	R4	R5	R6
DATAOUT2 :	G0	G1	G2	G3	G4	G5	G6
DATAOUT3 :	B0	B1	B2	B3	B4	B5	B6
COCK_A	0	1	2	3	4	5	6

NOTES:
1. Clock_A is the internal sampling clock of the system. The system clock may differ from CLK-MODE.
2. OE (output enable, fast switch, active LOW) and IICOE (I^2C-bus output enable, active HIGH) will switch the DATAOUT lines in high-z or normal mode.
3. See also Figure 14.

Auxiliary data

Pipelined external reference signal HREF_OUT (delayed HREF).

The delay line (wordlength 1-bit) has the same duration as the signal processing of the video data lines.

OPERATING CONDITIONS

Electrical conditions

Start-up condition
No particular function except the external power-on-reset, e.g., for I^2C-bus interface (RESET) is intended.

Operating Time
As this device will be used in computers, it has been designed to run continuously.

Handling
Inputs and outputs are protected against electrostatic discharge during normal handling. It is desirable, however, to observe normal handling precautions appropriate to MOS devices.

Temperature Range
Refer to the characteristics

Backup
No internal backup capability (standby) is provided.

Power Down Mode
No internal power-down capability is provided.

Error condition
To inhibit operations, no information signal is available to the peripheral circuits. In the advent of an error, the system must be re-started by application of the RESET signal.

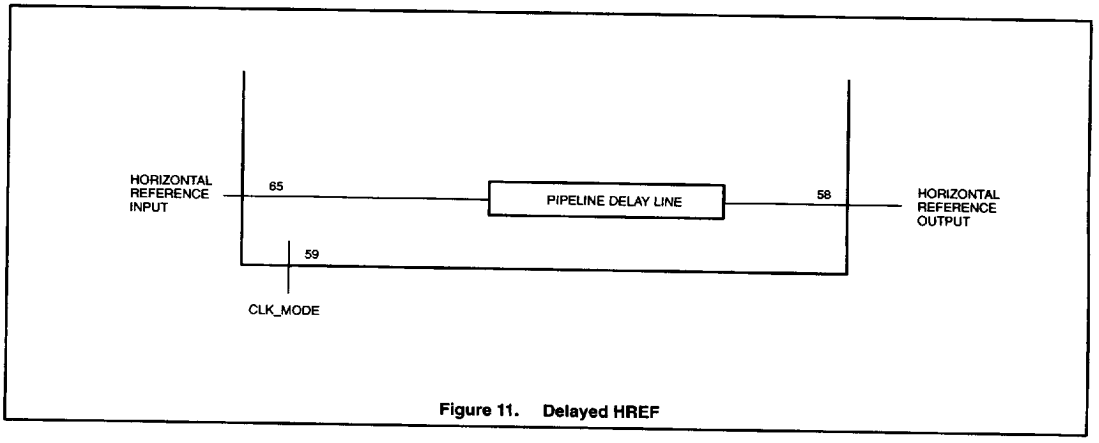


Figure 11. Delayed HREF

LIMITING VALUES

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{DD}	Supply voltage	−0.5	7	V
V_I	input voltage	−0.5	7	V
V_O	output voltage	−0.5	7	V
P_{tot}	total	—	1.5	W
T_{stg}	storage temperature range	−65	+150	C
T_{amb}	operating ambient temperature	−40	+125	C

CHARACTERISTICS

Tamb = −40 to 125°C unless otherwise specified

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V_{DD}	supply voltage		4.5	5.5	V
I_{DD}	supply current	note 1	—	165	mA
Inputs					
V_{IL}	input voltage LOW				
	SDA, SCL		−0.5	1.5	V
	any other		−0.5	0.8	V
V_{IH}	input voltage HIGH				
	SDA, SCL		3	V_{DD} +0.5	V
	any other		2	V_{DD} +0.5	V
I_L	input leakage current	note 2	—	10	µA
C_I	input capacitance		—	10	pF
outputs					
	output voltage				
V_{OH}	HIGH (any)		2.4	V_{DD}	V
V_{OL}	LOW (SDA)		0	0.4	V
	LOW (any other)		0	0.4	V
	output current				
I_{OH}	HIGH (any)		—	4	mA
I_{OL}	LOW (SDA)		—	3	mA
	LOW (any other)		—	4	mA
C_{LD}	output load capacitance		—	40	pF
I_O	output leakage current		—	10	µA

NOTES:

1. The supply current may vary between 30 and 165 mA depending upon the input data. The minimum may be achieved with $\overline{OE}$ disabled and no clock.
2. All inputs except TEST (internal pull-up resistor).

TIMING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
	propagation delay	note 2	—	26		t_{C16}
	CLOCK (DMSD-mode, LL27) :	note 3				
t_{C27}	cycle time		31	—	45	ns
	duty cycle		40	—	60	%
	CLOCK (16 MHz-mode) :	note 4				
t_{C16}	cycle time		62	—	83	ns
t_{CDL}	duty time LOW		30	—	—	ns
t_{CDH}	duty time HIGH		16	—	—	ns
	CREF					
t_{CS}	set-up time		11	—	—	ns
t_{CH}	hold time		3	—	—	ns
	HREF					
t_{HS}	set-up time		11	—	—	ns
t_{HH}	hold time		3	—	—	ns
t_{RH}	$\overline{\text{RESET}}$ hold time	4 clock periods				
	VLUTBYPASS	note 5				
t_{VS}	set-up time		8	—	—	ns
t_{VH}	hold time		0	—	—	ns
	CLK_MODE set-up time		must be set before $\overline{\text{RESET}}$			
	I^2C-bus address set-up time		must be set before $\overline{\text{RESET}}$			
	DATAIN					
t_{SU}	set-up time		11	—	—	ns
t_{HD}	hold time		3	—	—	ns
	DATAOUT					
t_{OS}	set-up time		10	—	—	ns
t_{OH}	hold time		10	—	—	ns
	HREF_OUT					
t_{OHS}	set-up time		9	—	—	ns
t_{OHH}	hold time		10	—	—	ns
t_{HZ}	output disable time (to tri-state)		—	10	15	ns
t_{ZH}	output enable time (from tri-state)			15	21	ns

NOTES:

1. Typical ratings are measured at V_{DD} = 5V and 25°C room temperature.
2. Denotes the delay in clock periods between DATAIN and DATAOUT.
3. DMSD-mode designates that the DCSC will work in a DMSD environment. The CLOCK and the clock reference signal will be fed by the SCGC (SAA7157). This is further explained in the following diagrams.
4. 16 MHz-mode indicates that the DCSC will work in any other environment. The CREF signal will be set internally to HIGH, the CLOCK signal can be any clock up to 16 MHz (see also Figure 15).
5. Must be set one clock period before DATAOUT.

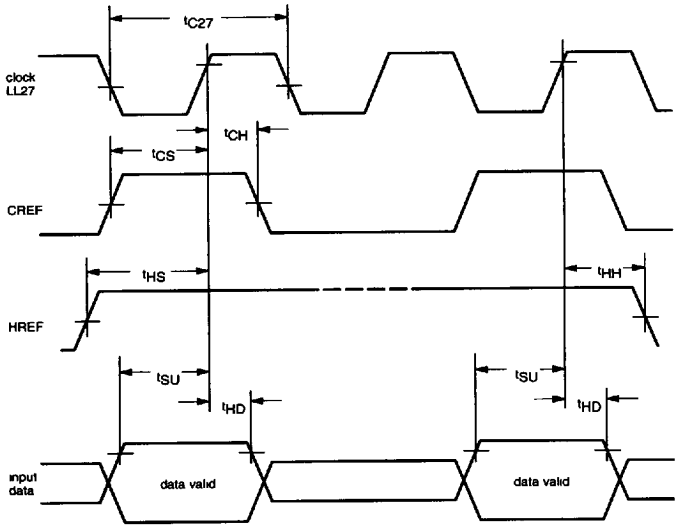


Figure 12. Timing diagram input

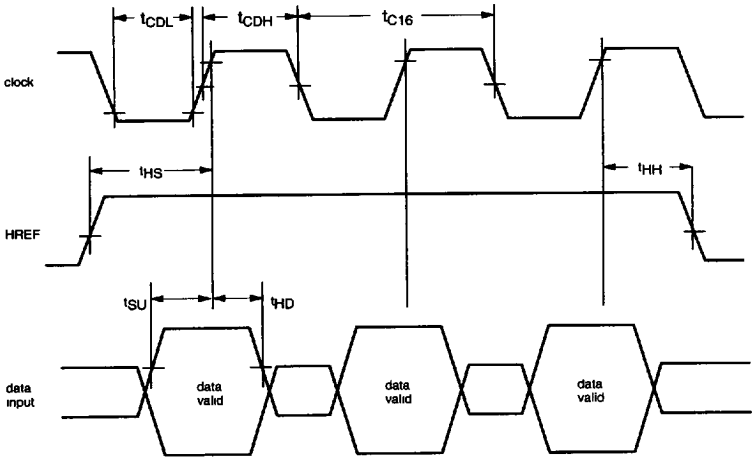


Figure 13. Timing diagram input (16 MHz mode)

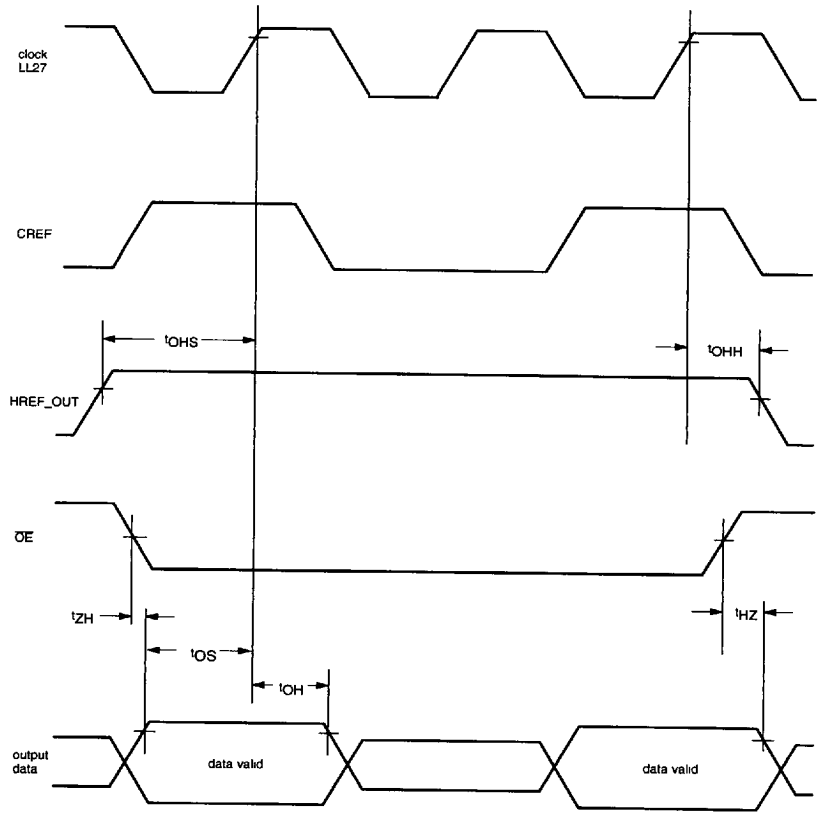
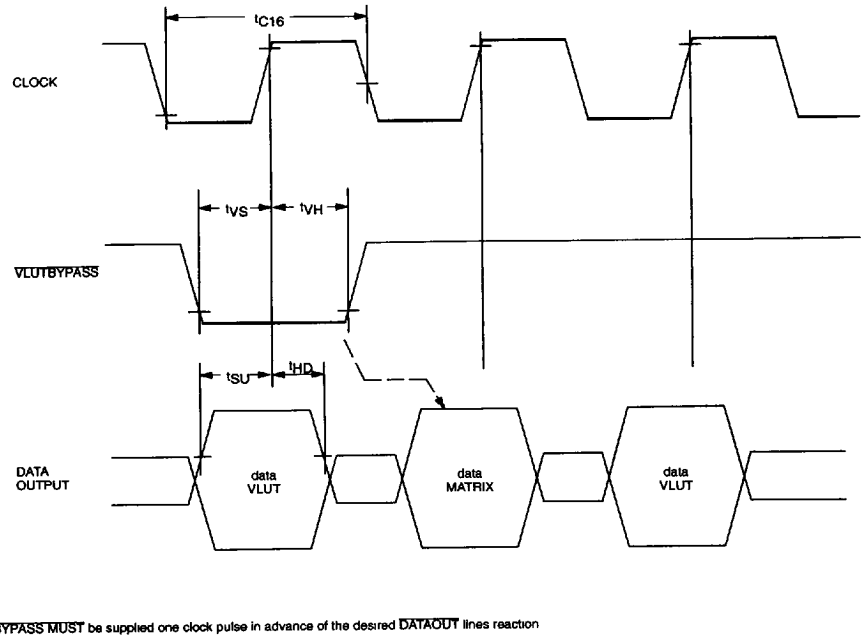


Figure 14. Timing diagram output

Error condition

To inhibit unwanted operations. no information signal is available to the peripheral circuits. In the advent of an error the system must be re-started by application of the $\overline{\text{RESET}}$ signal.



VLUTBYPASS MUST be supplied one clock pulse in advance of the desired DATAOUT lines reaction

Figure 15. Timing diagram VLUTBYPASS

SYSTEM BLOCK DESCRIPTION

Input formatter

The formatter consists of five functional blocks:

- the multiplexer, which decodes the luminance and chrominance input signals
- the filter, which interpolates the samples of the incoming signal to get an upsampled data rate as at DATAIN1
- the luminance delay line
- the timing control which creates the interval reference signals from the various inputs
- the bypass output multiplexer

The data applied at DATAIN1 to DATAIN3 is converted as follows:

FIL1 : Y luminance

FIL2 : Cr color-difference signal R-Y

FIL3 : Cb color-difference signal B-Y

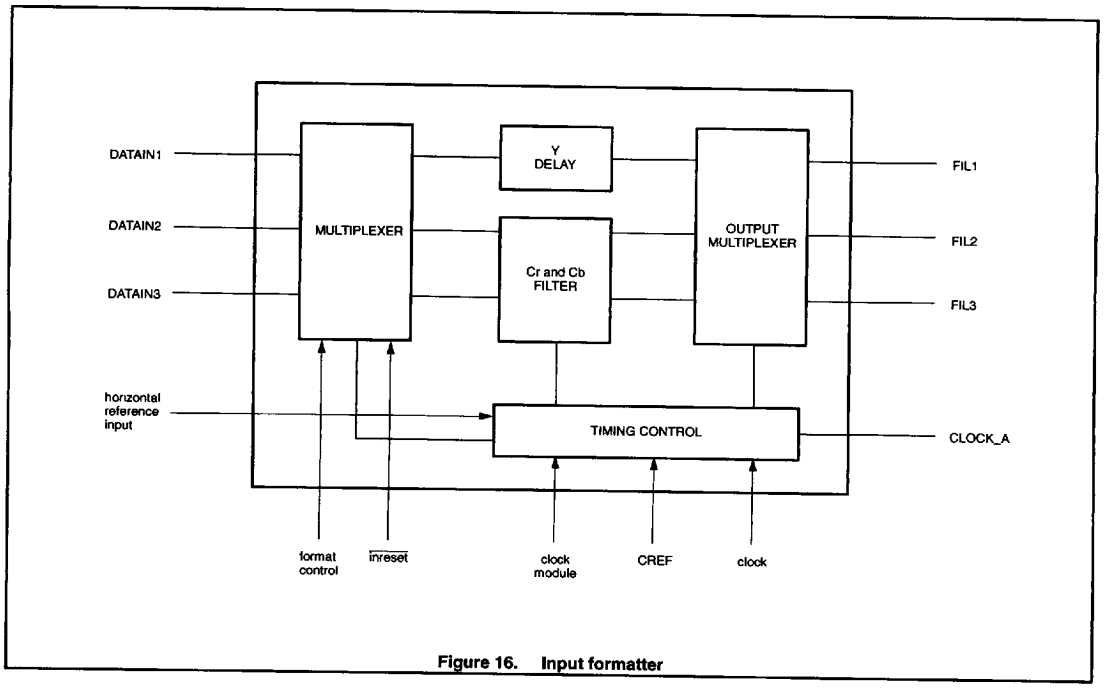


Figure 16. Input formatter

Filter and delay line

In the various functional modes the signal FMTCNTRL switches in the required filters (FMTCNTRL is described in ('Control data'). In all modes the same propagation delay will be realized, (the reference is Cb0, respective to U7 with format 0).

At all frequencies and in all formats, there is a delay line to compensate for the delay of the signal processing time needed in the chrominance section.

CHROMINANCE FILTER

The filter for the Cr and Cb signal is realized in one filter design.

Format 1, 2 4:1:1

An interpolating filter is inserted to convert the original sampling frequency of the luminance signal, i.e., four times that of the color signal. Figure 17 illustrates the frequency response of the chrominance section. .

Format 3, 4 4:2:2

An interpolating filter is inserted to convert the sampling frequency of the luminance signal, i.e., twice the color signal. Figure 18 illustrates the frequency response of the chrominance section

Format 5 4:4:4

A bypass with a specified delay is inserted.

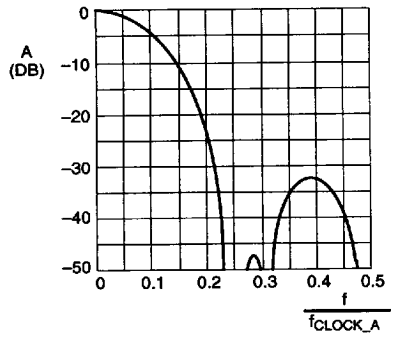


Figure 17. Frequency response of 4:1:1 filter

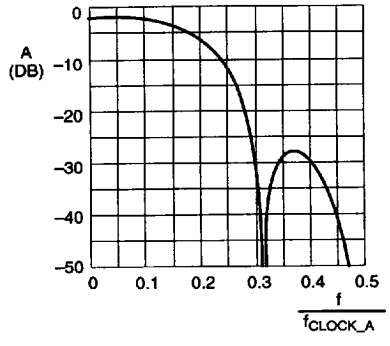


Figure 18. Frequency response of 4:2:2 filter

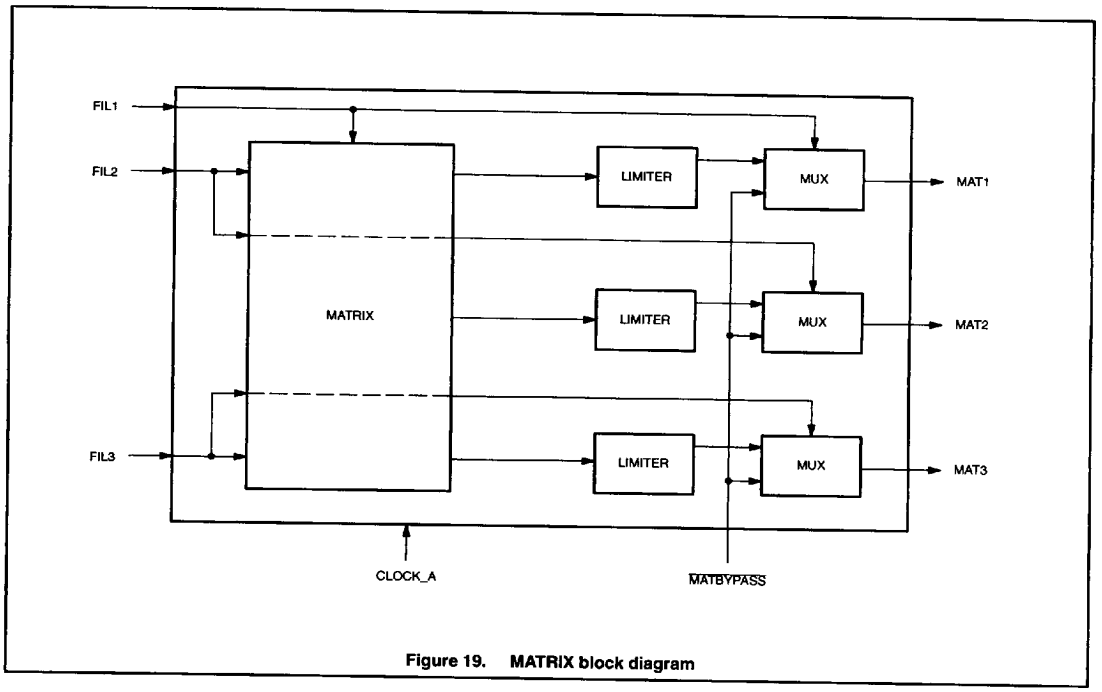


Figure 19. MATRIX block diagram

The properties of the conversion matrix are as follows:

- The conversion equations are (according to CCIR 601, with respect to the different quantization on Y, Cb and Cr);

  Red = Y + 1.371 (Cr – 0.5)

  Green = Y – 0.698 (Cr – 0.5) – 0.336 (Cb – 0.5)

  Blue = Y + 1.732 (Cb – 0.5)
- The accuracy of the signal processing is within ± 0.5% of the accuracy of a theoretical conversion.
- The input and output data lines are 8-bit.
- In the advent of non-standard input levels, the limiter reduces the possible output data values to between 0 and 255.
- $\overline{\text{MATBYPASS}}$ switches the matrix in bypass. The bypass has the same propagation delay as the matrix itself.

VIDEO LOOK-UP TABLE AND OUTPUT STAGE

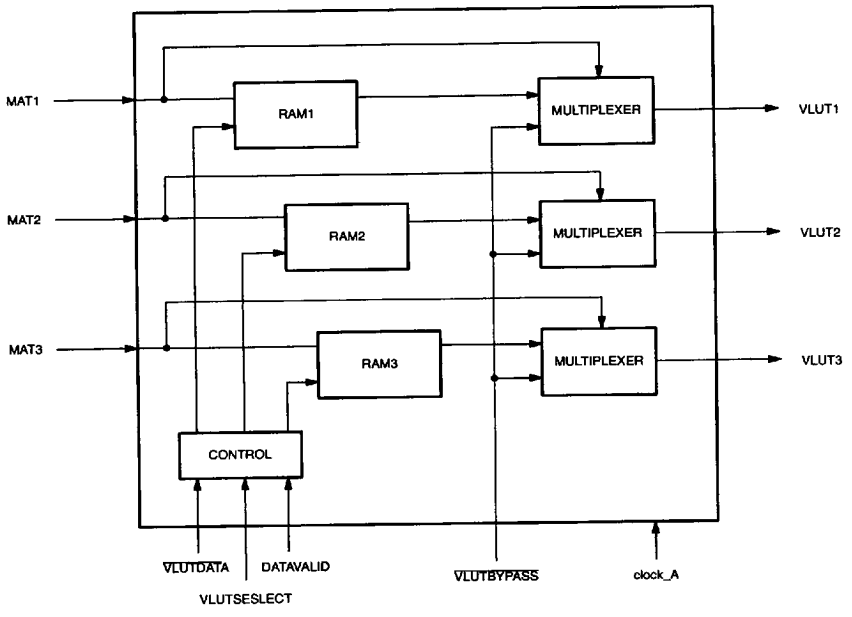


Figure 20. Block diagram video look up table.

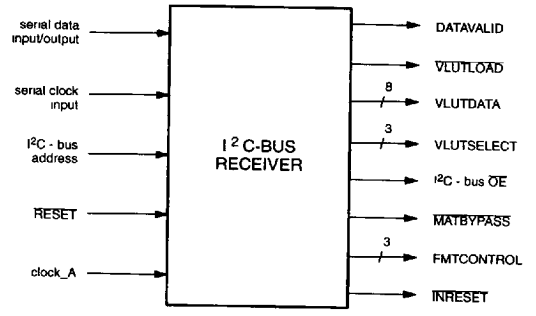


Figure 21. Block diagram of I²C-bus receiver

Functional description

The VLUTLOAD will be set to the WRITE operation if one of the four addresses are received from the RAMs. VLUTLOAD will be set to the READ operation following reception of the last databyte.

VLUTSELECT provides selection of one VLUT according to the sub-address.

VLUTDATA contains the value for the address counter (VLUT_ADDRESS; the start address of the first byte to be written into the RAM) and the data for the RAMs, validated with DATAVALID.

The databytes will be loaded by an autoincrement function. VLUTBYPASS will bypass the VLUT's in clock period time (real time switch).

In computer applications the VLUT is also known as a Color Look-Up Table (CLUT).

In the DCSC this table might be used to invert the Gamma-correction of a camera. This correction is applied to compensate for the non-linear relationship between the video voltage applied to the cathode and the light output of the phosphor of a CRT.

The Gamma-correction function (also known as Gradation) is given as;

$Y = X^{\gamma}$

The VLUTs are realized by 256 x 8-bit RAMs.

I²C-bus RECEIVER

The DCSC can be switched to different modes via the I²C-bus receiver.

The I²C-bus receiver is also used to feed the VLUT RAMs with data.

I²C-bus Receiver Functional Description

Following power-up, all internal control signals are at undefined values. The I²C-bus receiver must be reset by the external RESET signal. Following RESET the control signals are set to:

FMTCNTRL	:=	100	format 4:4:4
MATBYPASS	:=	0	matrix bypassed
INRESET	:=	0	input data set to fixed values
IICOE	:=	1	OE enabled

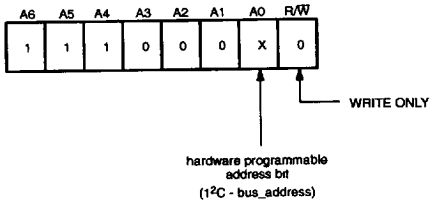


Figure 22. The address for the DCSC

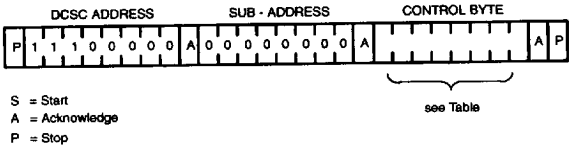


Figure 23. The address of the control byte is 00_{HEX}

In this example the control signals are set to:

FMTCNTRL	:=	2	Format 3	:	4:2:2 DMSD
$\overline{\text{MATBYPASS}}$	:=	1	matrix in use		
$\overline{\text{INRESET}}$	:=	0	input DATA at fixed values during HREF = 0		
IICOE	:=	1	$\overline{\text{OE}}$ enabled		

Table 19. Levels of the color bar signal

CONDITION	E'_R	E'_G	E'_B	Y	C_R	C_B	R	G	B
White	1.0	1.0	1.0	235	128	128	235	235	235
Black	0	0	0	16	128	128	16	16	16
Red	1.0	0	0	82	240	90	236	17	16
Green	0	1.0	0	145	34	54	16	236	17
Blue	0	0	1.0	41	110	240	16	16	235
Yellow	1.0	1.0	0	210	146	16	235	235	16
Cyan	0	1.0	1.0	170	16	166	16	235	236
Magenta	1.0	0	1.0	106	222	202	235	15	234

NOTE:
The color bar signal is described in CCR 601, Rep. 629-2, Table 1. It can be used to check the nominal levels (at least for black and white) between the functional blocks of the DCSC.

Table 20. Control byte formats

D7	D6	D5	D4	D3	D2	D1	D0	Functions
X	X	X	X	X	0	0	0	input formatter at format 0 Filter switched to 4:1:1 filter
X	X	X	X	X	0	0	1	input formatter at format 1 Filter switched to 4:1:1 filter
X	X	X	X	X	0	1	0	input formatter at format 2 Filter switched to 4:2:2 filter
X	X	X	X	X	0	1	1	input formatter at format 3 Filter switched to 4:2:2 filter
X	X	X	X	X	1	0	0	input formatter at format 4 Filter switched to bypass
X	X	X	X	0	X	X	X	matrix bypassed
X	X	X	X	1	X	X	X	matrix in use
X	X	X	0	X	X	X	X	input data at fixed values
X	X	X	1	X	X	X	X	input data to formatter
X	X	0	X	X	X	X	X	output stages 3-State
X	X	1	X	X	X	X	X	OE enabled

D0-D2 FMTCONTROL

D3 $\overline{\text{MATBYPASS}}$

D4 $\overline{\text{INRESET}}$

D5 IICOE

D6 not used

D7 not used

Table 21. Sub-addresses VLUTDATA:

SUB-ADDRESS	VLUT-ADDRESS	DATA BYTES
01	XX	VLUTDATA RAM 1 (RED)
02	XX	VLUTDATA RAM 2 (GREEN)
03	XX	VLUTDATA RAM 3 (BLUE)
04	XX	VLUTDATA RAM 1,2,3

NOTE:
addresses in HEX representation

VLUTDATA

Four sub-addresses are implemented into the different VLUT RAMs. RAM can be addressed individually or together. The memory of each VLUT RAM can be addressed, e.g. if only parts of the data has to be changed.

I²C-bus receiver timing examples

The exact timing of the signals are described in the I²C-bus specification. The addresses indicated in Figure 25 are in HEX representation.

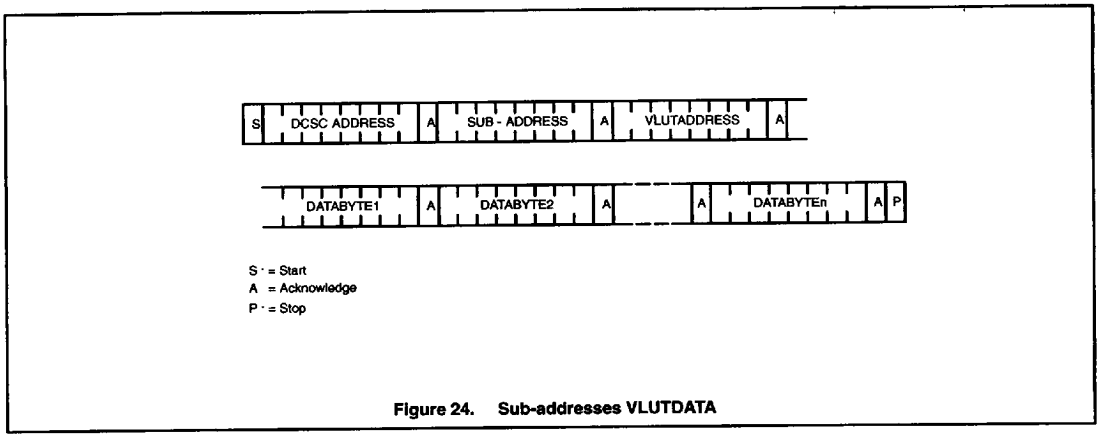


Figure 24. Sub-addresses VLUTDATA

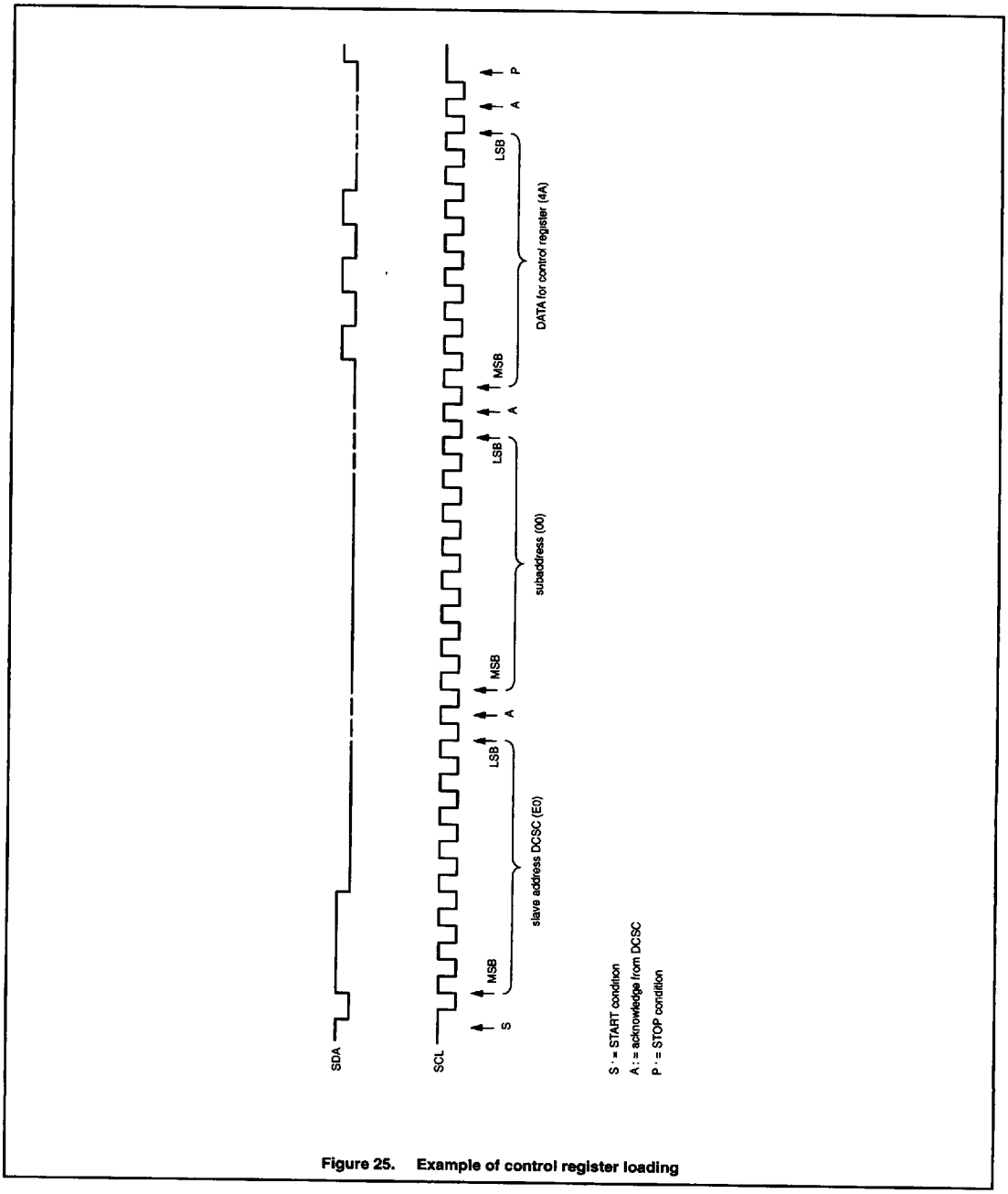


Figure 25. Example of control register loading

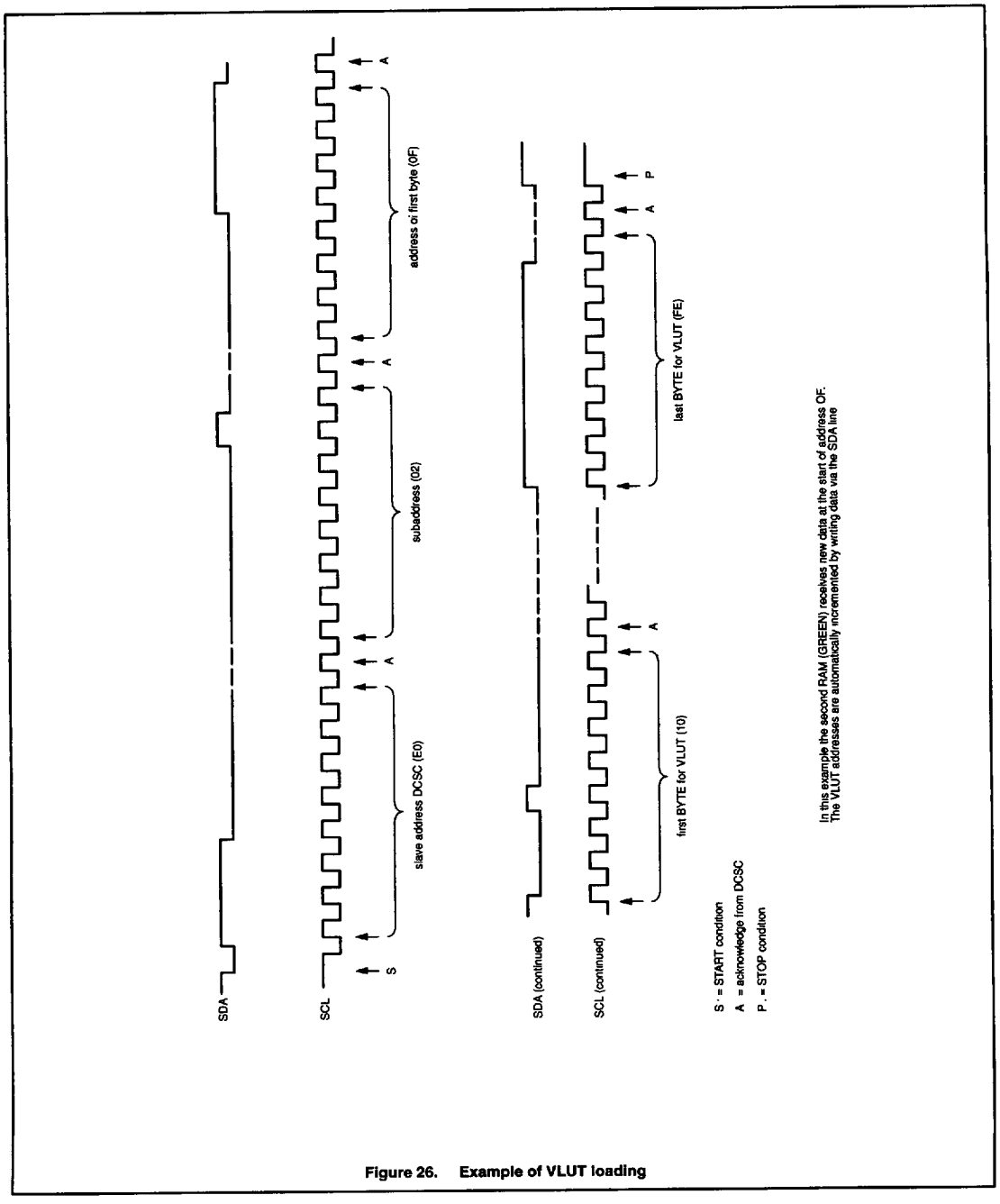


Figure 26. Example of VLUT loading

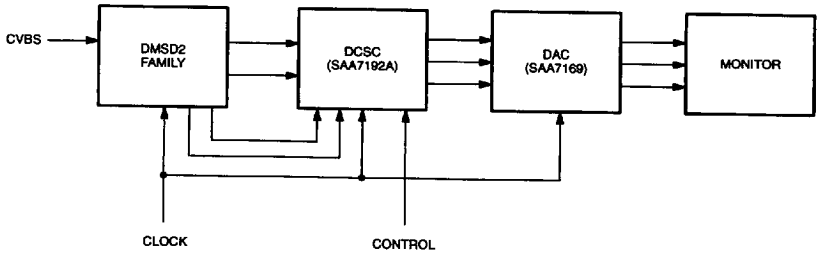


Figure 27. Application with DMSD2

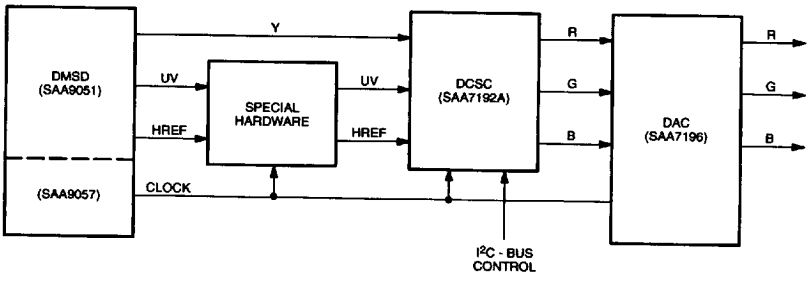


Figure 28. Application with SAA9051

APPLICATION

The application is simple since the DCSC is designed to operate in conjunction with the DMSD2 decoder family.

Additional hardware is required to convert the level formats to permit the DCSC to be used with the older 7-bit version of the DMSD.

Due to the differing data formats between the SAA9051 and the SAA7192, the color difference U and V signals must be converted from two's-complement to unipolar representation and the MSBs of the UV data must be inverted. Differing chrominance amplitudes are small and are not taken into account.

Additionally, the DATAIN10 (LSB of the Y-data) should be connected to ground and the DATAIN34 and DATAIN36 (LSBs of the UV data) should be connected to ground via a resistor to avoid noise at the LSBs.

GLOSSARY

B	color component of a video signal (BLUE)
C	coded color components of a video signal (TV)
Cb	coded color difference signal (digital B-Y)
CCIR	Comite Consultatif International de Radiocommunication (International Radio Consultative Committee)
CDS-System	Chip Design System
CGC	Clock Generation Circuit
CLUT	Color Look Up Table (personal computer graphics)
Cr	coded color difference signal (digital R-Y)
CREF	Clock Reference Signal; indicates the valid data samples of the DMSD
CVBS	Composite Video Burst Synchron signal (TV)
DCSC	Digital Color Space Converter; converts the YUV signal to RGB
DIN	Deutches Institut fuer Normung, Berlin
DMSD	family of Digital Multi-standard Decoders, decodes YUV out of the CVBS signal
G	color component of a video signal (GREEN)
HDTV	High Definition Television
HREF	Horizontal Line Reference Signal
I^2C-bus	Inter-IC-Bus (Valvo network concept between controllers)
IRT	Institut fuer Rundfunk Technik (Muenchen)
IIC-DVP/SE	Philips Components RHW Hamburg, Department Industrial-ICs Video Products System Engineering
MIC-SE	Philips Components RHW Hamburg, Department MOS-ICs System Engineering (now called IIC-DVP-SE)
RGB	components of a video signal (red, green, blue)
R	color component of a video signal (RED)
SCL	clock line of the I^2C-bus
SDA	data line of the I^2C-bus
SRC	Sample Rate Converter
Semiparallel	Chrominance data (multiplexed color difference) parallel to luminance data
SERInet	Signetics Elcoma Research ISA Network (Philips computer interconnection network)
VLUT	Video Look Up Table. RAM to multiply video data with a factor
Y	luminance signal (brightness of a video signal)
YUV Bus	Component bus of the DMSD family
U	color difference signal (coded video signal B-Y)
V	color difference signal (coded video signal R-Y)