PD - 94342A

International
IOR Rectifier

RADIATION HARDENED POWER MOSFET SURFACE-MOUNT (SMD-2)

IRHNA67260

200V, N-CHANNEL

R6 TECHNOLOGY

Product Summary

Part Number	Radiation Level	$R_{DS(on)}$	I_D
IRHNA67260	100K Rads (Si)	0.028Ω	63A
IRHNA63260	300K Rads (Si)	0.028Ω	63A
IRHNA64260	600K Rads (Si)	0.028Ω	63A
IRHNA68260	1000K Rads (Si)	0.028Ω	63A

SMD-2

International Rectifier's R6™ technology provides superior power MOSFETs for space applications. These devices have improved immunity to Single Event Effect (SEE) and have been characterized for useful performance with Linear Energy Transfer (LET) up to 90MeV/(mg/cm²).

Their combination of very low $R_{DS(on)}$ and faster switching times reduces power loss and increases power density in today's high speed switching applications such as DC-DC converters and motor controllers. These devices retain all of the well established advantages of MOSFETs such as voltage control, ease of paralleling and temperature stability of electrical parameters.

Features:

- Low $R_{DS(on)}$
- Fast Switching
- Single Event Effect (SEE) Hardened
- Low Total Gate Charge
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Surface Mount
- Ceramic Package
- Light Weight

Absolute Maximum Ratings

Pre-Irradiation

	Parameter		Units
I_D @ V_{GS} = 12V, T_C = 25°C	Continuous Drain Current	63	A
I_D @ V_{GS} = 12V, T_C = 100°C	Continuous Drain Current	40	
I_{DM}	Pulsed Drain Current ①	252	
P_D @ T_C = 25°C	Max. Power Dissipation	250	W
	Linear Derating Factor	2.0	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	246	mJ
I_{AR}	Avalanche Current ①	63	A
E_{AR}	Repetitive Avalanche Energy ①	25	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J T_{STG}	Operating Junction Storage Temperature Range	-55 to 150	°C
	Pckg. Mounting Surface Temp.	300 (for 5s)	
	Weight	3.3 (Typical)	g

For footnotes refer to the last page

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	200	—	—	V	V_{GS} = 0V, I_D = 1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Temperature Coefficient of Breakdown Voltage	—	0.17	—	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.028	Ω	V_{GS} = 12V, I_D = 40A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 1.0mA
g_{fs}	Forward Transconductance	40	—	—	S (℧)	V_{DS} = 25V, I_{DS} = 40A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	10	μA	V_{DS} =160V ,V_{GS}=0V
		—	—	25		V_{DS} = 160V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	240	nC	V_{GS} = 12V, I_D = 63A V_{DS} = 100V
Q_{gs}	Gate-to-Source Charge	—	—	70		
Q_{gd}	Gate-to-Drain ('Miller') Charge	—	—	60		
$t_{d(on)}$	Turn-On Delay Time	—	—	40	ns	V_{DD} = 100V, I_D = 63A, V_{GS} = 12V, R_G = 2.35Ω
t_r	Rise Time	—	—	60		
$t_{d(off)}$	Turn-Off Delay Time	—	—	70		
t_f	Fall Time	—	—	30		
$L_S + L_D$	Total Inductance	—	2.8	—	nH	Measured from the center of drain pad to center of source pad
C_{iss}	Input Capacitance	—	8120	—	pF	V_{GS} = 0V, V_{DS} = 25V f = 100KHz
C_{oss}	Output Capacitance	—	949	—		
C_{rss}	Reverse Transfer Capacitance	—	13	—		
R_g	Internal Gate Resistance	—	1.1	—	Ω	f = 0.73MHz, open drain

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	63	A	
I_{SM}	Pulse Source Current (Body Diode) ①	—	—	252		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	T_j = 25°C, I_S = 63A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	—	640	ns	T_j = 25°C, I_F = 63A, di/dt ≤ 100A/μs V_{DD} ≤ 25V ④
Q_{RR}	Reverse Recovery Charge	—	—	11.7	μC	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R_{thJC}	Junction-to-Case	—	—	0.5	°C/W	

Note: Corresponding Spice and Saber models are available on International Rectifier Web site.

For footnotes refer to the last page

Radiation Characteristics

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

	Parameter	Up to 600K Rads(Si)[1]		1000K Rads (Si)[2]		Units	Test Conditions
		Min	Max	Min	Max		
BV_{DSS}	Drain-to-Source Breakdown Voltage	200	—	200	—	V	V_{GS} = 0V, I_D = 1.0mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0	4.0	1.5	4.0		V_{GS} = V_{DS}, I_D = 1.0mA
I_{GSS}	Gate-to-Source Leakage Forward	—	100	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	—	-100	—	-100		V_{GS} = -20 V
I_{DSS}	Zero Gate Voltage Drain Current	—	10	—	25	µA	V_{DS}= 160V, V_{GS} =0V
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-3)	—	0.029	—	0.029	Ω	V_{GS} = 12V, I_D =40A
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (SMD-2)	—	0.028	—	0.028	Ω	V_{GS} = 12V, I_D =40A
V_{SD}	Diode Forward Voltage ④	—	1.2	—	1.2	V	V_{GS} = 0V, I_S = 63A

1. Part numbers IRHNA67260, IRHNA63260 and IRHNA64260
2. Part number IRHNA68260

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Single Event Effect Safe Operating Area

Ion	LET	Energy	Range	VDS (V)							
	(MeV/(mg/cm2))	(MeV)	(µm)	@VGS= 0V	@VGS= -5V	@VGS= -10V	@VGS= -15V	@VGS= -17V	@VGS= -18V	@VGS= -19V	@VGS= -20V
Xe	59	825	66	200	200	200	200	170	160	-	-
Xe	43	2441	205	200	200	200	200	200	190	180	150

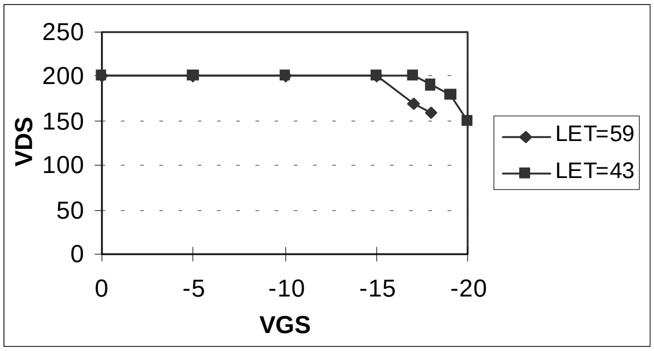


Fig a. Single Event Effect, Safe Operating Area

For footnotes refer to the last page

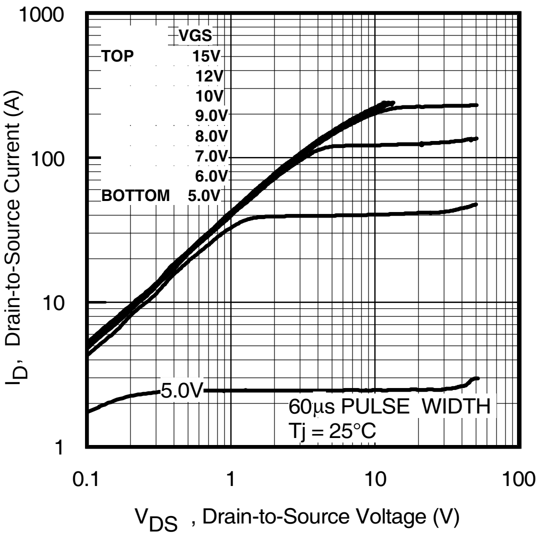


Fig 1. Typical Output Characteristics

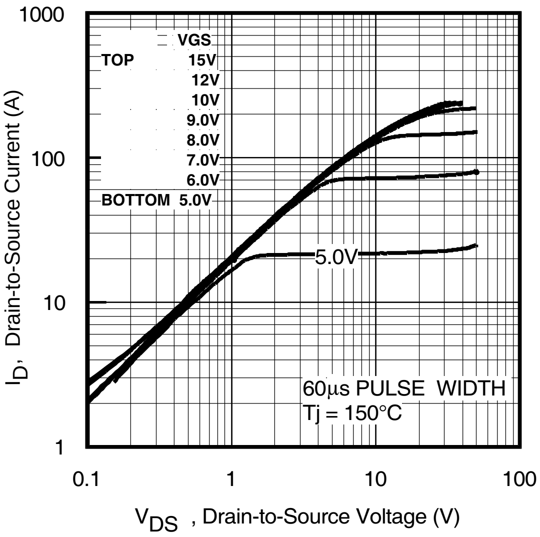


Fig 2. Typical Output Characteristics

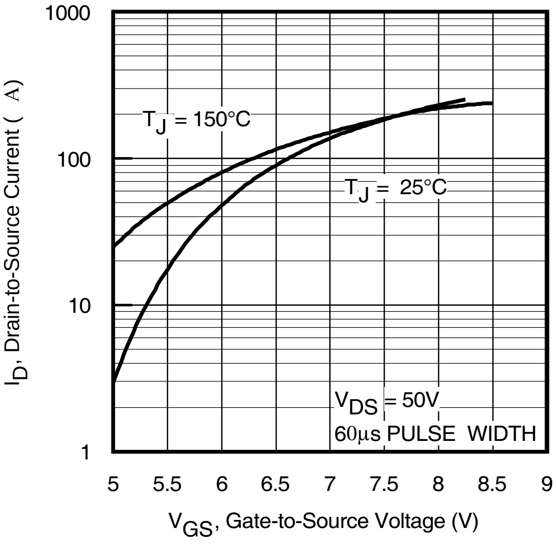


Fig 3. Typical Transfer Characteristics

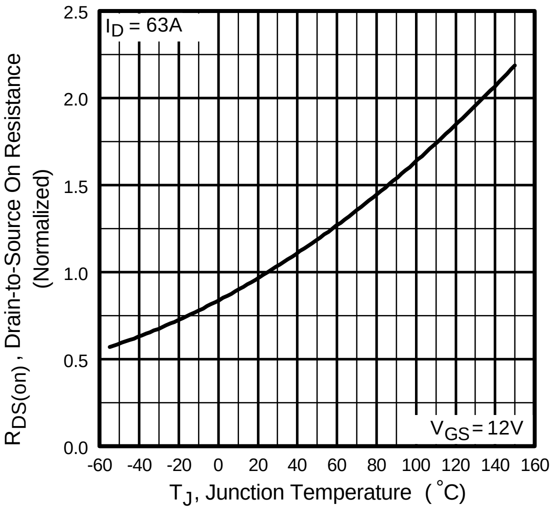


Fig 4. Normalized On-Resistance Vs. Temperature

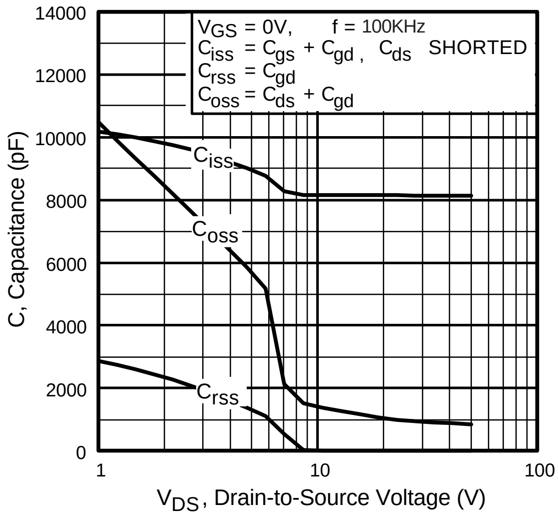


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

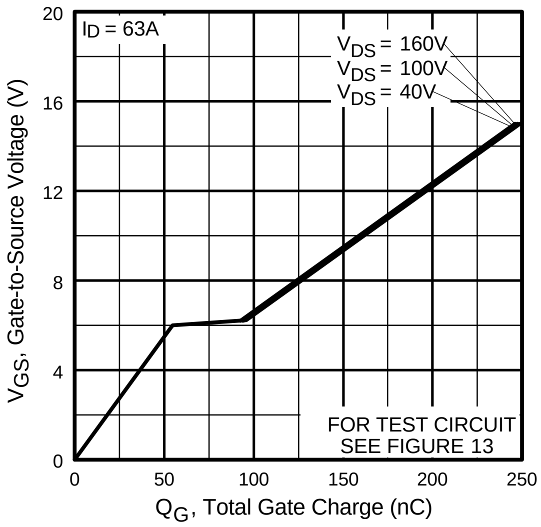


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

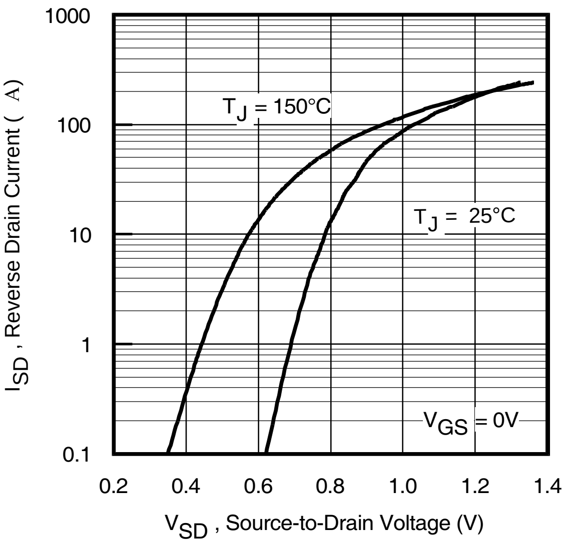


Fig 7. Typical Source-Drain Diode Forward Voltage

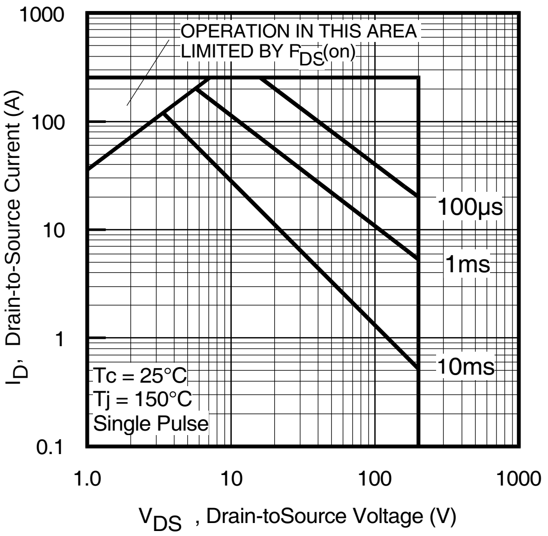


Fig 8. Maximum Safe Operating Area

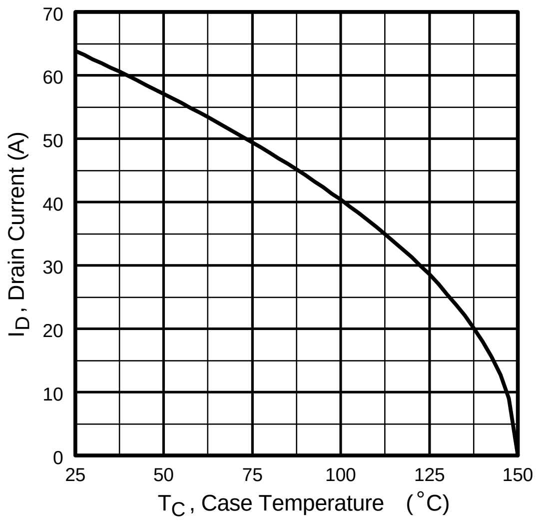


Fig 9. Maximum Drain Current Vs. Case Temperature

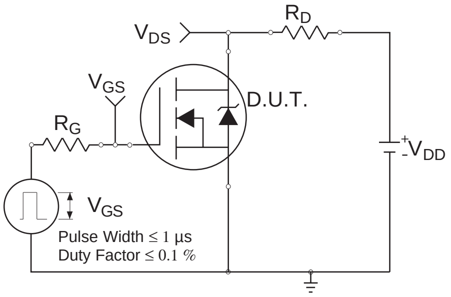


Fig 10a. Switching Time Test Circuit

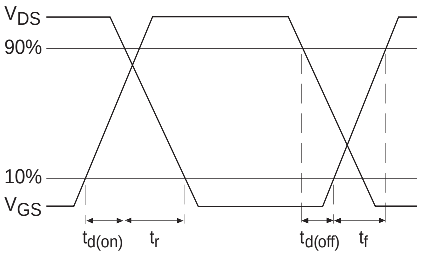


Fig 10b. Switching Time Waveforms

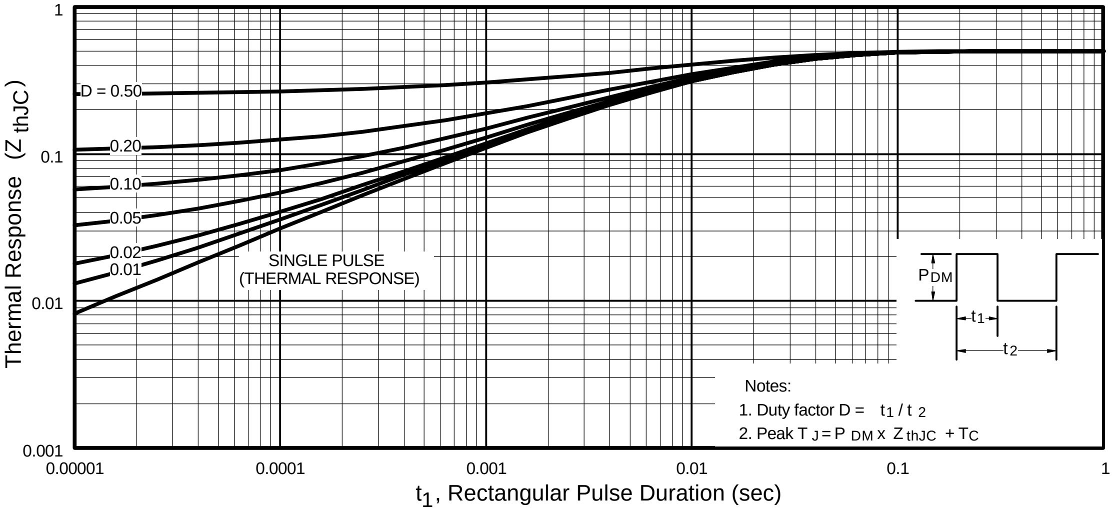


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

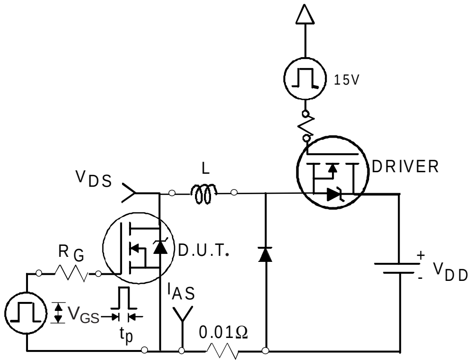


Fig 12a. Unclamped Inductive Test Circuit

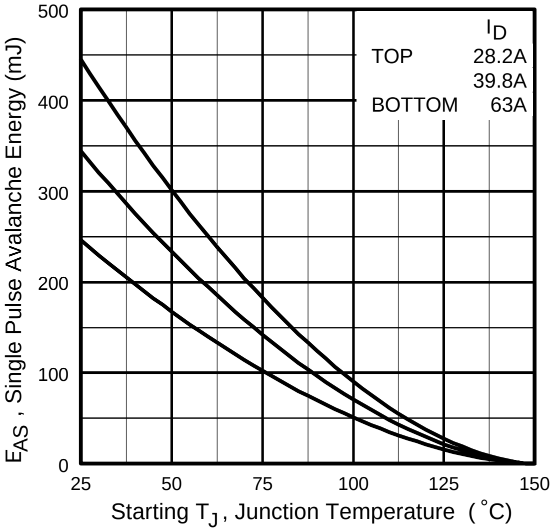


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

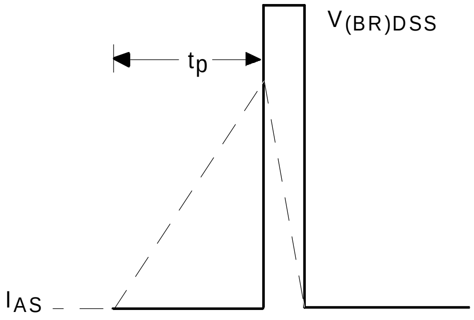


Fig 12b. Unclamped Inductive Waveforms

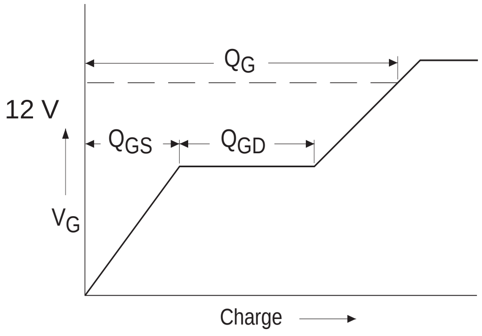


Fig 13a. Basic Gate Charge Waveform

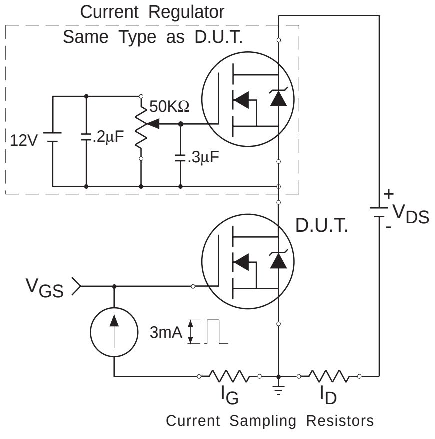


Fig 13b. Gate Charge Test Circuit

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.

② V_{DD} = 25V, starting T_J = 25°C, L= 0.124 mH
Peak I_L = 63A, V_{GS} = 12V

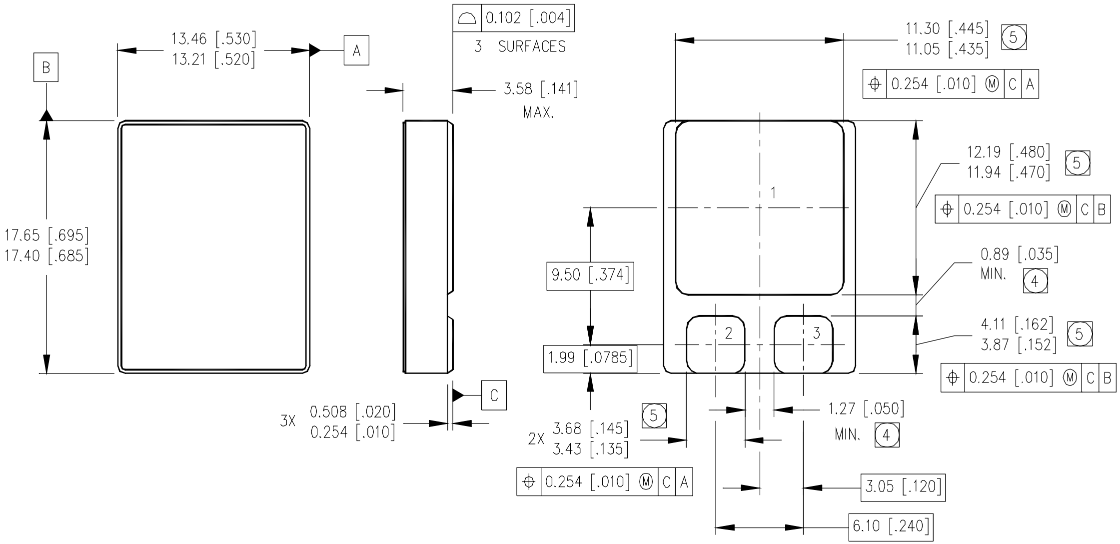
③ $I_{SD} \leq$ 63A, di/dt ≤ 875A/µs,
$V_{DD} \leq$ 200V, $T_J \leq$ 150°C

④ Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

⑤ **Total Dose Irradiation with V_{GS} Bias.**
12 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, method 1019, condition A.

⑥ **Total Dose Irradiation with V_{DS} Bias.**
160 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, method 1019, condition A.

Case Outline and Dimensions — SMD-2



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

④ DIMENSION INCLUDES METALLIZATION FLASH.
⑤ DIMENSION DOES NOT INCLUDE METALLIZATION FLASH.

PAD ASSIGNMENTS

1 = DRAIN
2 = GATE
3 = SOURCE

International
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