

International IR Rectifier

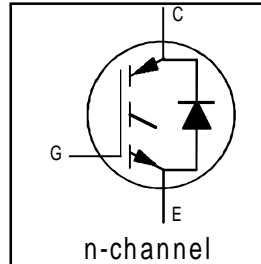
PD - 94255

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

IRG4BC10SD-S IRG4BC10SD-L Standard Speed CoPack IGBT

Features

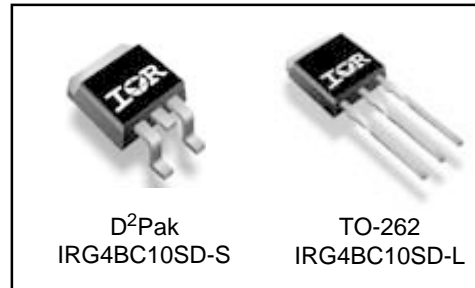
- Extremely low voltage drop 1.1Vtyp. @ 2A
- S-Series: Minimizes power dissipation at up to 3 KHz PWM frequency in inverter drives, up to 4 KHz in brushless DC drives.
- Very Tight Vce(on) distribution
- IGBT co-packaged with HEXFRED™ ultrafast, ultra-soft-recovery anti-parallel diodes for use in bridge configurations
- Industry standard D²Pak & TO-262 packages



$V_{CES} = 600V$
$V_{CE(on)} \text{ typ.} = 1.10V$
@ $V_{GE} = 15V, I_C = 2.0A$

Benefits

- Generation 4 IGBT's offer highest efficiencies available
- IGBT's optimized for specific application conditions
- HEXFRED diodes optimized for performance with IGBT's. Minimized recovery characteristics require less/no snubbing
- Lower losses than MOSFET's conduction and Diode losses



D²Pak
IRG4BC10SD-S

TO-262
IRG4BC10SD-L

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
$I_C @ T_C = 25^\circ C$	Continuous Collector Current	14	A
$I_C @ T_C = 100^\circ C$	Continuous Collector Current	8.0	
I_{CM}	Pulsed Collector Current ①	18	
I_{LM}	Clamped Inductive Load Current ②	18	
$I_F @ T_C = 100^\circ C$	Diode Continuous Forward Current	4.0	
I_{FM}	Diode Maximum Forward Current	18	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	38	W
$P_D @ T_C = 100^\circ C$	Maximum Power Dissipation	15	
T_J	Operating Junction and	-55 to +150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	—	—	3.3	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	—	—	7.0	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount ⑤	—	—	80	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount, steady state)⑥	—	—	40	
Wt	Weight	—	2.0(0.07)	—	

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IRG4BC10SD-S/L

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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage ^③	600	—	—	V	$V_{GE} = 0V, I_C = 250\mu A$
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.64	—	V/°C	$V_{GE} = 0V, I_C = 1.0mA$
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	1.58	1.8	V	$I_C = 8.0A$ $I_C = 14.0A$ $I_C = 8.0A, T_J = 150^\circ\text{C}$ $V_{GE} = 15V$ See Fig. 2, 5
		—	2.05	—		
		—	1.68	—		
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		$V_{CE} = V_{GE}, I_C = 250\mu A$
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-9.5	—	mV/°C	$V_{CE} = V_{GE}, I_C = 250\mu A$
g_{fe}	Forward Transconductance ^④	3.65	5.48	—	S	$V_{CE} = 100V, I_C = 8.0A$
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	μA	$V_{GE} = 0V, V_{CE} = 600V$ $V_{GE} = 0V, V_{CE} = 600V, T_J = 150^\circ\text{C}$
		—	—	1000		
V_{FM}	Diode Forward Voltage Drop	—	1.5	1.8	V	$I_C = 4.0A$ $I_C = 4.0A, T_J = 150^\circ\text{C}$ See Fig. 13
		—	1.4	1.7		
I_{GES}	Gate-to-Emitter Leakage Current	—	—	± 100	nA	$V_{GE} = \pm 20V$

Switching Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	15	22	nC	$I_C = 8.0A$ $V_{CC} = 400V$ $V_{GE} = 15V$ See Fig. 8
Q_{ge}	Gate - Emitter Charge (turn-on)	—	2.42	3.6		
Q_{gc}	Gate - Collector Charge (turn-on)	—	6.53	9.8		
$t_{d(on)}$	Turn-On Delay Time	—	76	—	ns	$T_J = 25^\circ\text{C}$ $I_C = 8.0A, V_{CC} = 480V$ $V_{GE} = 15V, R_G = 100\Omega$ Energy losses include "tail" and diode reverse recovery. See Fig. 9, 10, 18
t_r	Rise Time	—	32	—		
$t_{d(off)}$	Turn-Off Delay Time	—	815	1200		
t_f	Fall Time	—	720	1080		
E_{on}	Turn-On Switching Loss	—	0.31	—		
E_{off}	Turn-Off Switching Loss	—	3.28	—	mJ	
E_{ts}	Total Switching Loss	—	3.60	10.9		
E_{ts}	Total Switching Loss	—	1.46	2.6	mJ	$I_C = 5.0A$
$t_{d(on)}$	Turn-On Delay Time	—	70	—	ns	$T_J = 150^\circ\text{C}$, See Fig. 10,11, 18 $I_C = 8.0A, V_{CC} = 480V$ $V_{GE} = 15V, R_G = 100\Omega$ Energy losses include "tail" and diode reverse recovery.
t_r	Rise Time	—	36	—		
$t_{d(off)}$	Turn-Off Delay Time	—	890	—		
t_f	Fall Time	—	890	—		
E_{ts}	Total Switching Loss	—	3.83	—	mJ	
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	280	—	pF	$V_{GE} = 0V$ $V_{CC} = 30V$ $f = 1.0MHz$ See Fig. 7
C_{oes}	Output Capacitance	—	30	—		
C_{res}	Reverse Transfer Capacitance	—	4.0	—		
t_{rr}	Diode Reverse Recovery Time	—	28	42	ns	$T_J = 25^\circ\text{C}$ See Fig. 14 $T_J = 125^\circ\text{C}$
		—	38	57		
I_{rr}	Diode Peak Reverse Recovery Current	—	2.9	5.2	A	$T_J = 25^\circ\text{C}$ See Fig. 15 $T_J = 125^\circ\text{C}$
		—	3.7	6.7		
Q_{rr}	Diode Reverse Recovery Charge	—	40	60	nC	$T_J = 25^\circ\text{C}$ See Fig. 16 $T_J = 125^\circ\text{C}$
		—	70	105		
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery During t_b	—	280	—	A/ μs	$T_J = 25^\circ\text{C}$ See Fig. 17 $T_J = 125^\circ\text{C}$
		—	235	—		

Details of note ① through ④ are on the last page

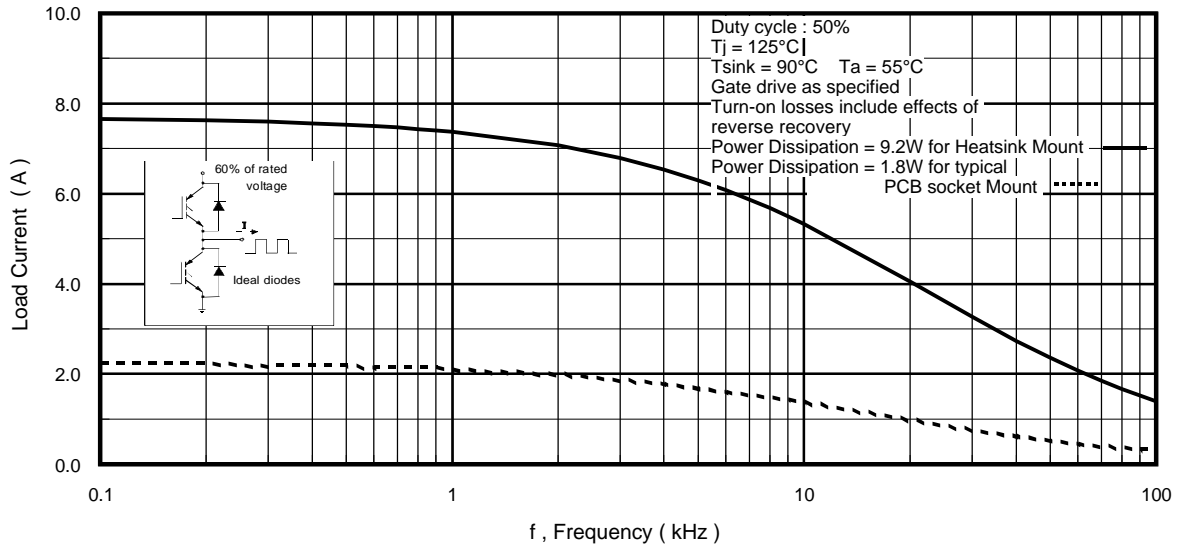


Fig. 1 - Typical Load Current vs. Frequency
 (Load Current = I_{RMS} of fundamental)

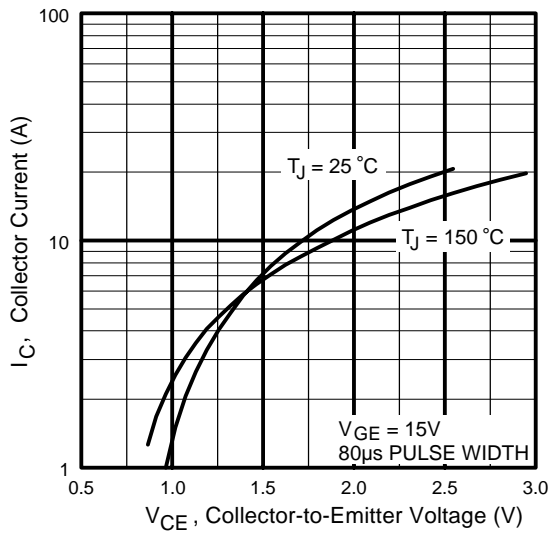


Fig. 2 - Typical Output Characteristics

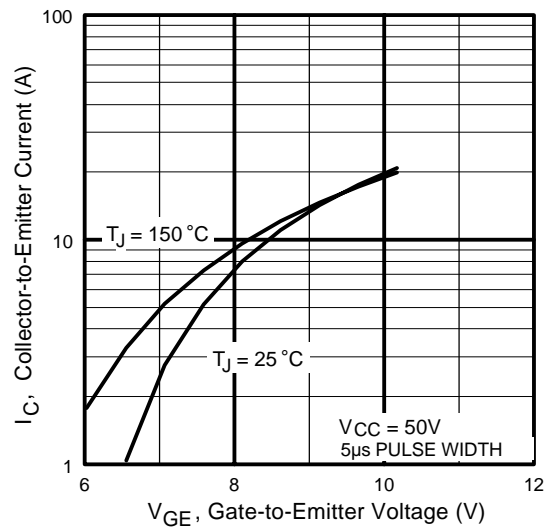


Fig. 3 - Typical Transfer Characteristics

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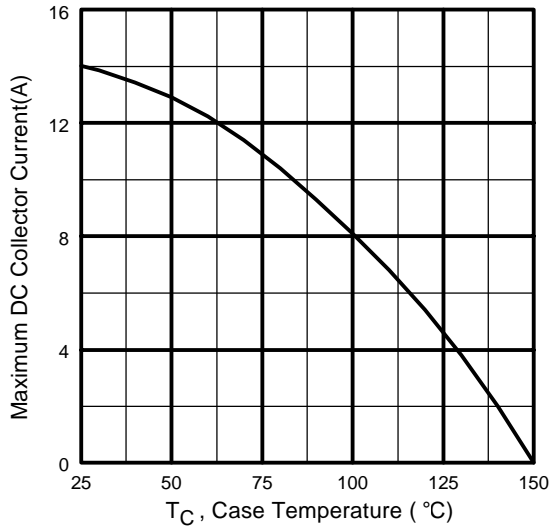


Fig. 4 - Maximum Collector Current vs. Case Temperature

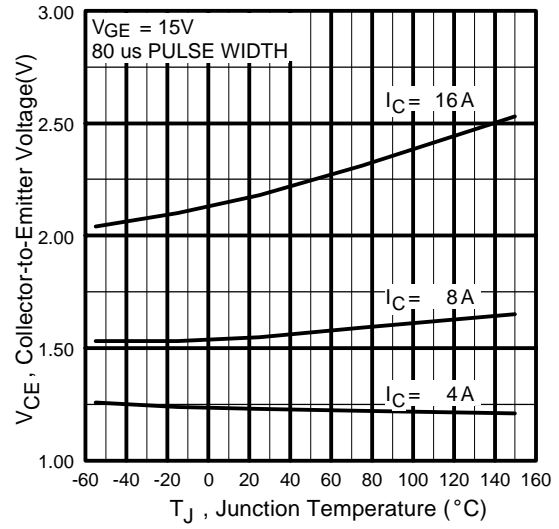


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

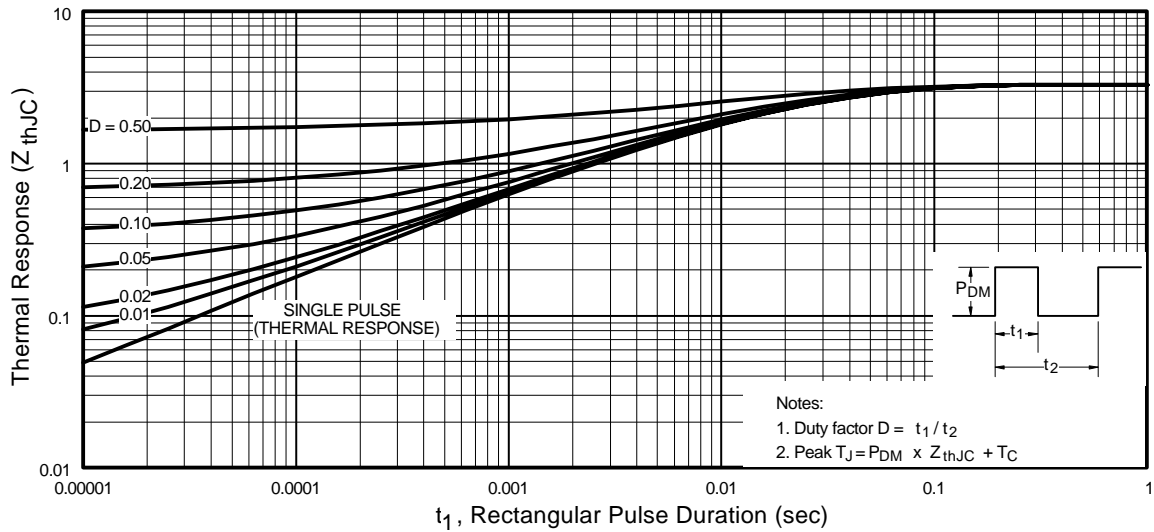


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

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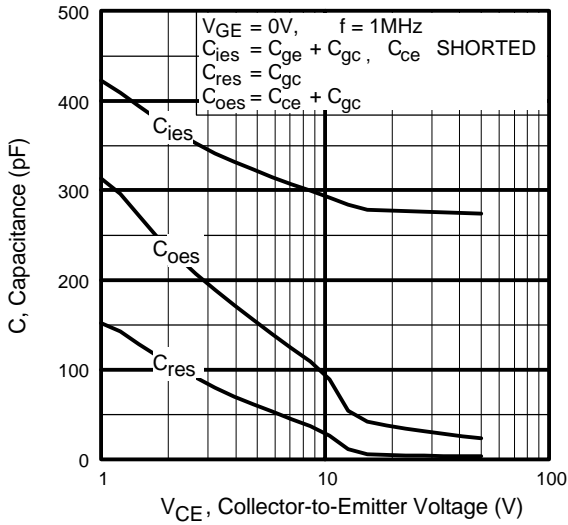


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

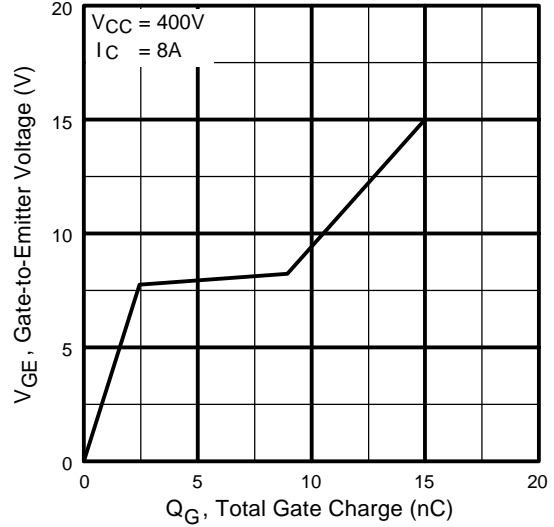


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

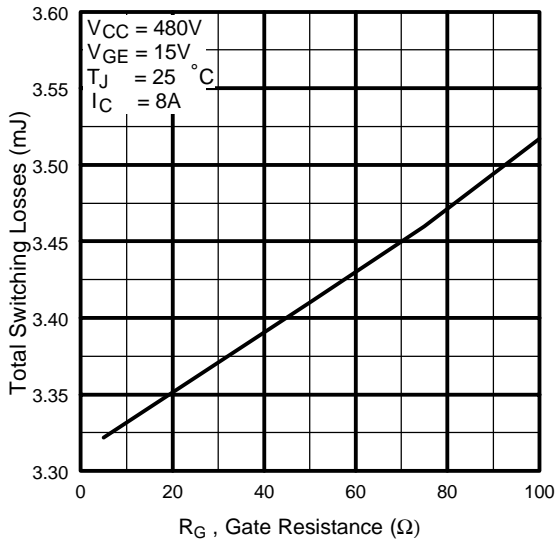


Fig. 9 - Typical Switching Losses vs. Gate Resistance

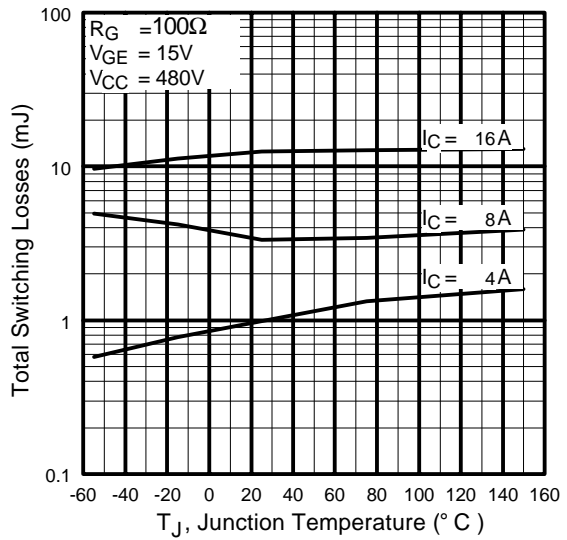


Fig. 10 - Typical Switching Losses vs. Junction Temperature

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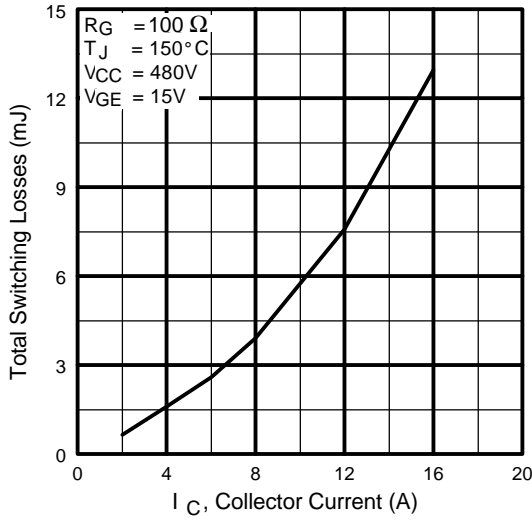


Fig. 11 - Typical Switching Losses vs. Collector Current

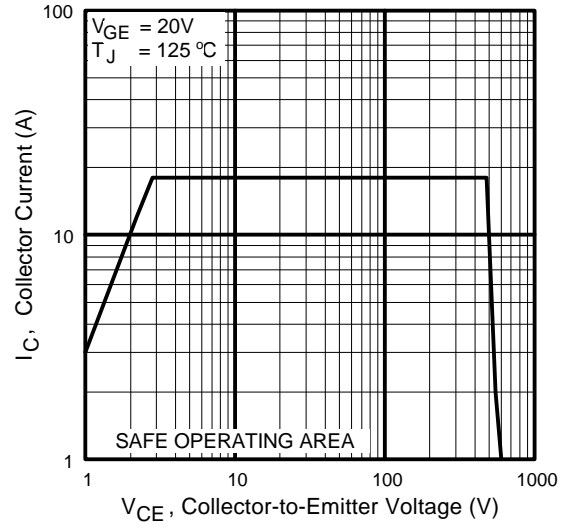


Fig. 12 - Turn-Off SOA

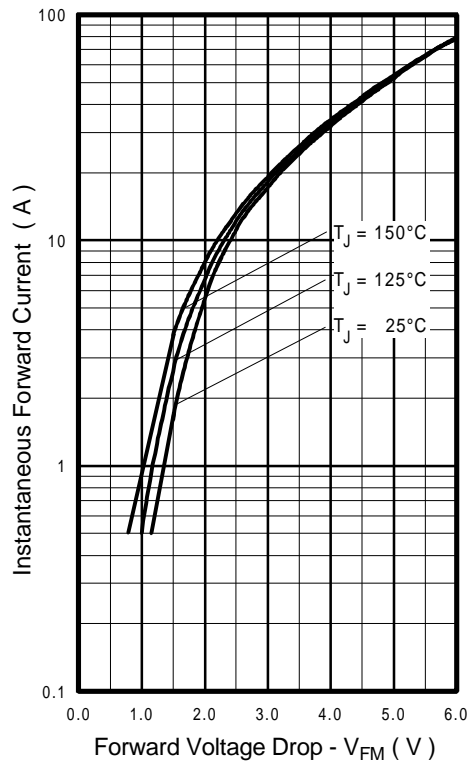


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

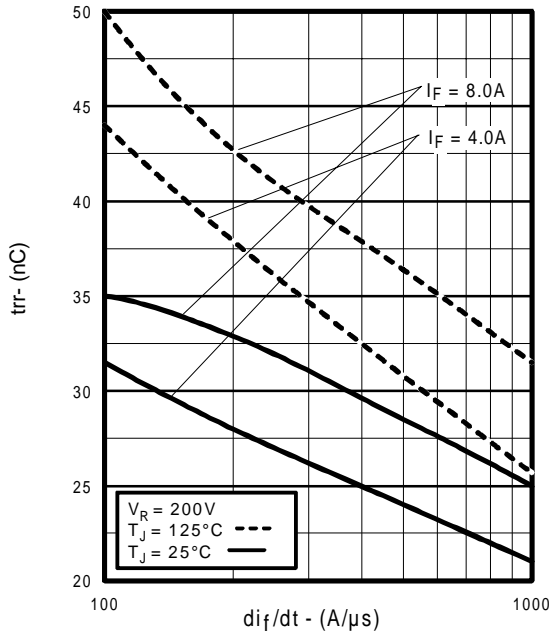


Fig. 14 - Typical Reverse Recovery vs. dI_f/dt

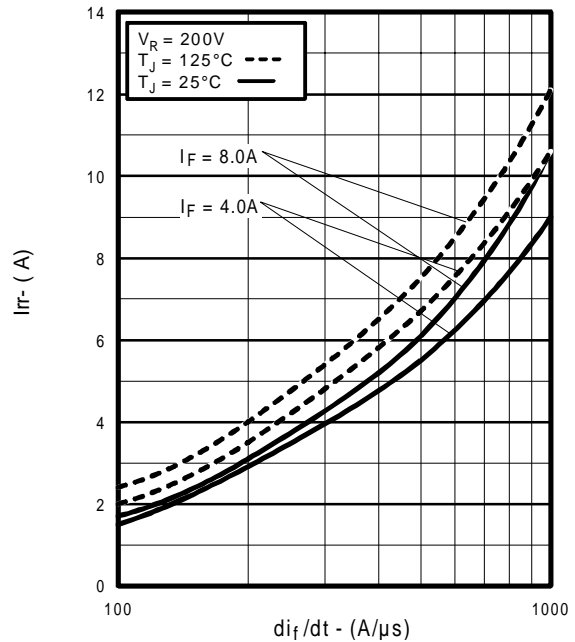


Fig. 15 - Typical Recovery Current vs. dI_f/dt

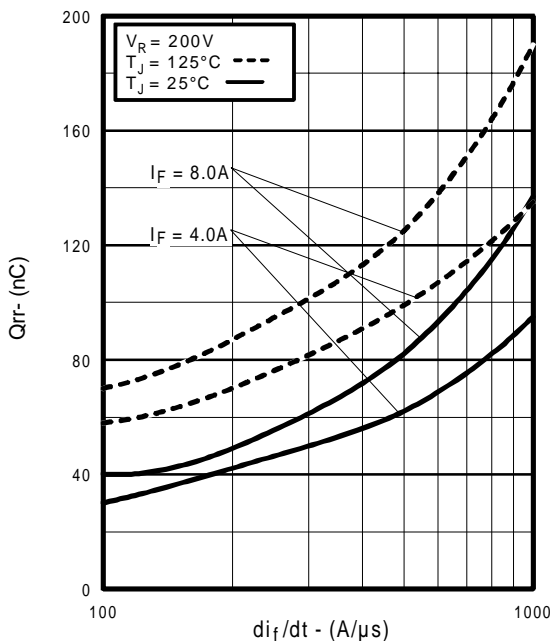


Fig. 16 - Typical Stored Charge vs. dI_f/dt

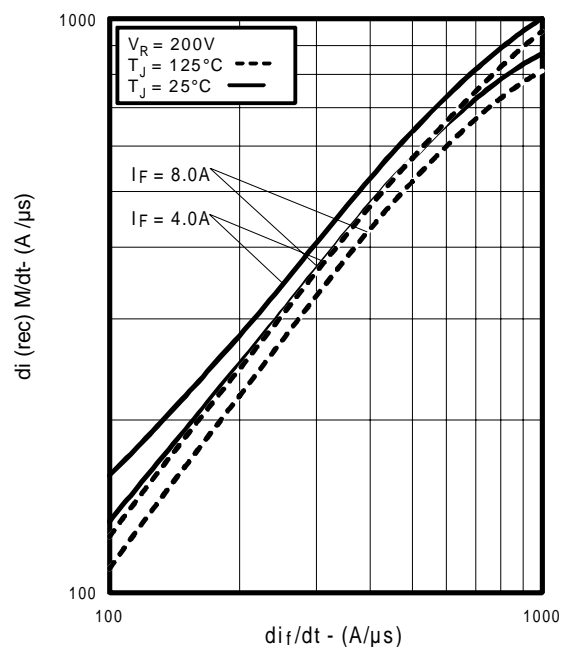


Fig. 17 - Typical $dI_{(rec)M}/dt$ vs. dI_f/dt ,

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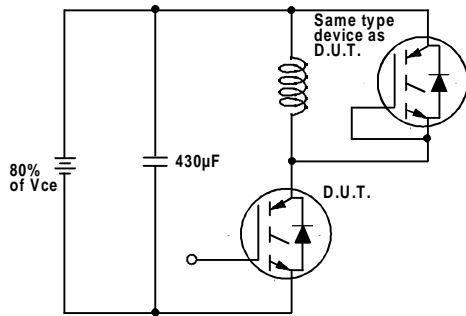


Fig. 18a - Test Circuit for Measurement of I_{LM} , E_{on} , $E_{off}(\text{diode})$, t_{rr} , Q_{rr} , I_{rr} , $t_{d(on)}$, t_r , $t_{d(off)}$, t_f

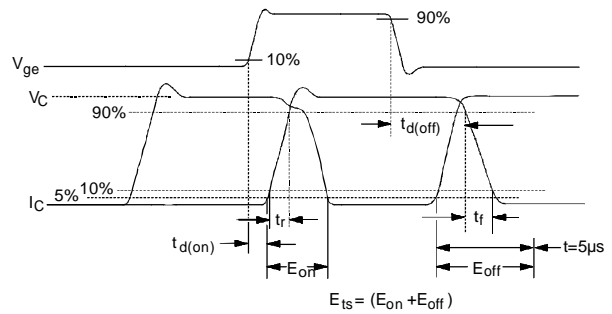


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off} , $t_{d(off)}$, t_f

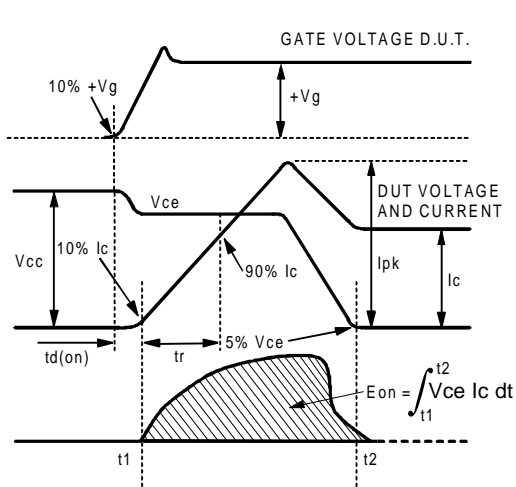


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on} , $t_{d(on)}$, t_r

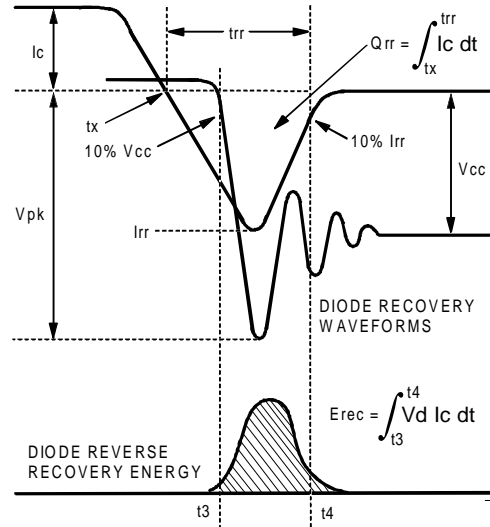


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec} , t_{rr} , Q_{rr} , I_{rr}

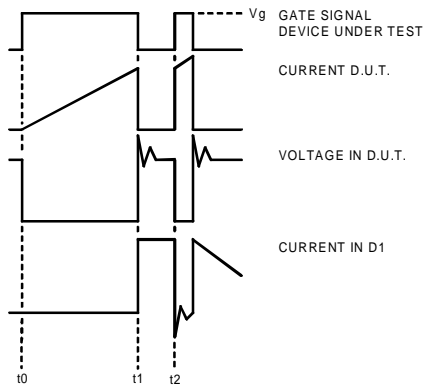


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

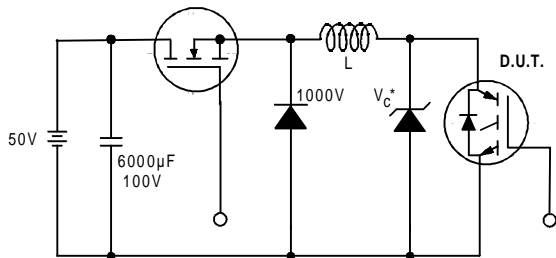


Figure 19. Clamped Inductive Load Test Circuit

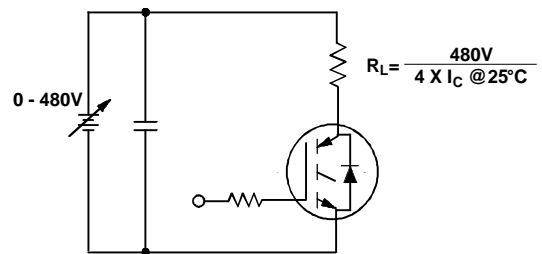
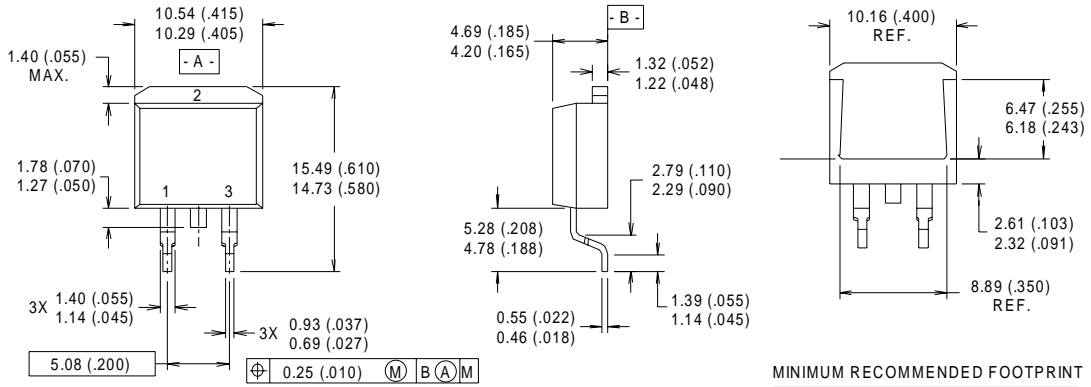


Figure 20. Pulsed Collector Current Test Circuit

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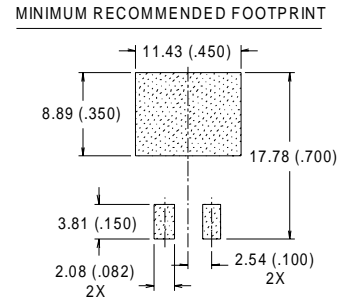


D²Pak Package Outline

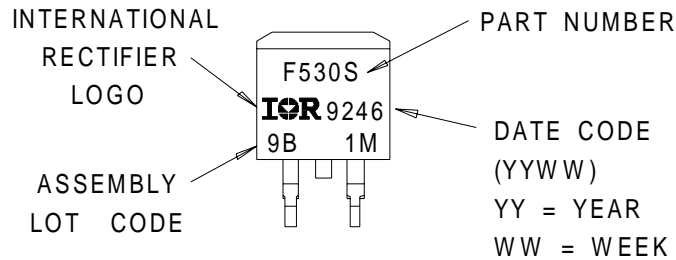


- NOTES:
- 1 DIMENSIONS AFTER SOLDER DIP.
 - 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
 - 3 CONTROLLING DIMENSION : INCH.
 - 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

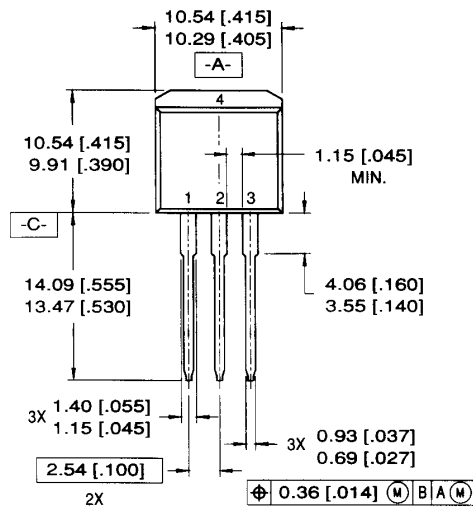
- LEAD ASSIGNMENTS
- 1 - GATE
 - 2 - DRAIN
 - 3 - SOURCE



D²Pak Part Marking Information



TO-262 Package Outline



LEAD ASSIGNMENTS

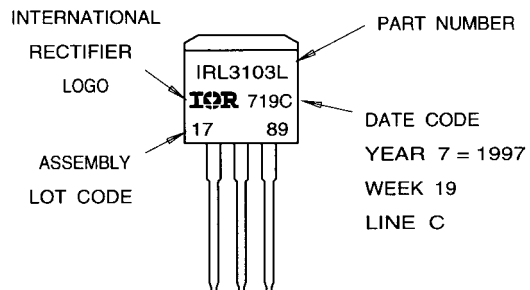
- | | |
|-----------|------------|
| 1 = GATE | 3 = SOURCE |
| 2 = DRAIN | 4 = DRAIN |

NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

TO-262 Part Marking Information

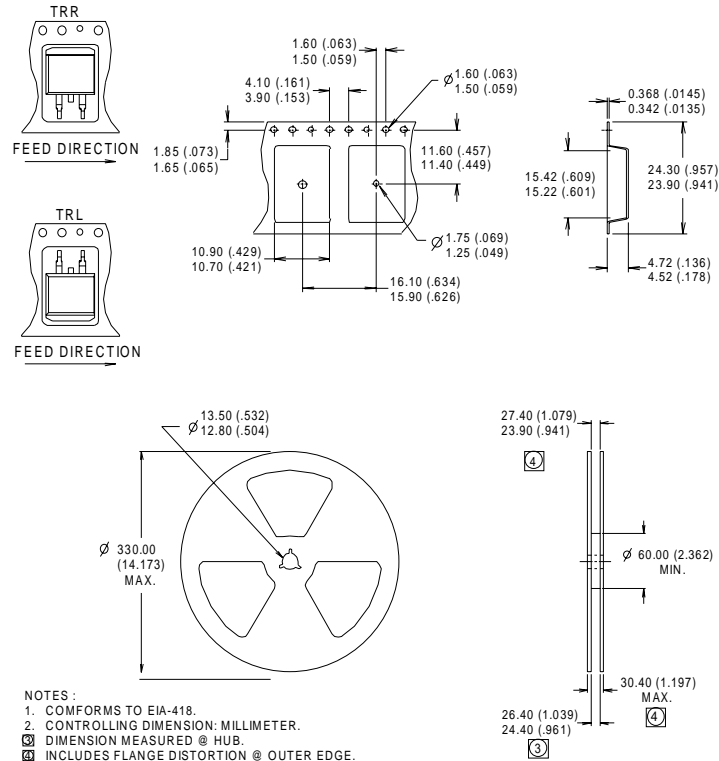
EXAMPLE: THIS IS AN IRL3103L
 LOT CODE 1789
 ASSEMBLED ON WW 19, 1997
 IN THE ASSEMBLY LINE "C"



IRG4BC10SD-S/L

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D²Pak Tape & Reel Information



Notes:

- ① Repetitive rating: $V_{GE}=20V$; pulse width limited by maximum junction temperature (figure 20)
- ② $V_{CC}=80\%(V_{CES})$, $V_{GE}=20V$, $L=10\mu H$, $R_G = 100W$ (figure 19)
- ③ Pulse width $\leq 80\mu s$; duty factor $\leq 0.1\%$.
- ④ Pulse width $5.0\mu s$, single shot.
- ⑤ This only applies to TO-262 package.
- ⑥ This applies to D²Pak, when mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

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