ESS Technology, Inc.

ES4228/ES4227
Internet Set-Top Box Solution
Product Brief

DESCRIPTION

The ES4228 MPEG video/audio decoder works as the central processing unit for Internet set-top box applications, while the ES4227 companion chip integrates all of the necessary discrete components for Internet set-top boxes. The high level of flexibility and versatility provided by the ES4228/ES4227 chipset makes it the most cost-effective, high-performance solution for the Internet set-top box market.

The ES4228 includes a programmable internal RISC processor core that makes it adaptable for use in embedded systems applications such as set-top boxes. The ES4227 companion chip supplies proper video sync capabilities and performs NTSC- and PAL-based video encoding and decoding as necessary to provide broadcast quality video to the television screen.

The ES4227 is a mixed-signal chip that includes a high quality NTSC/PAL encoder, two programmable 16-bit sigma-delta audio DACs, a PLL clock synthesizer, two microphone A/D converters, an I/O expansion port, and an echo/surround sound circuit.

The ES4228 controls the ES4227 through a proprietary bus, the Device Serial Communication (DSC) bus. The ES4227 gets video input and audio input from the ES4228. Video format is 8-bit YUV, and audio format is I^2S.

Command and register accesses are issued through the DSC interface from the ES4228 to the ES4227 through the DSC interface for accessing the internal registers of the ES4227. The DSC interface port is comprised of three interface signals, the strobe (DSC_S), data (DSC_D), and clock (DSC_C).

The DSC port is selected when the DSC strobe goes high and latches the data at the rising edge of the clock. Each 16-bit DSC transfer is comprised of an address followed by data.

The digital video encoder of the ES4227 uses three 9-bit video DACs to generate composite and S-video analog signals. One video DAC handles the composite video output, while the other two handle the S-video outputs. Color space conversions are provided to match the input data to the required output format, then the data is filtered to meet the selected video standards.

The programmable audio DACs of the ES4227 offer differential audio outputs. These outputs ensure further noise reduction while providing a dual audio output with a signal-to-noise ratio better than 90 dB. The expansion I/O port is address-mapped to the ES4228. Four pins of the port can be configured as edge-triggered interrupts, supporting critical functions such as handling remote control and modem interrupt requests, DVD/SVCD loader resets and modem board resets.

The ES4228 is available in an industry-standard 208-pin Plastic Quad Flat Pack (PQFP) package, while the ES4227 is available in an industry-standard 100-pin PQFP package.

ES4228 FEATURES

- Single-chip MPEG-2 video/audio decoder and system parser in 208-pin PQFP package.
- 640 x 480 NTSC and 640 x 576 PAL television video resolutions supported.
- Software-configurable for Internet e-mail and web browser functions.
- Karaoke, On-Screen Display (OSD), Playback Control (PBC) for Video CD 2.0 and 3.0 and trick mode functions supported.
- VideoCD 1.1, 2.0, Interactive 3.0, Super VCD and Audio CD compatible (SVCD and DVD configurations only).
- SmartScale™ video scaling supports both X-axis and Y-axis interpolationa and bidirectional NTSC to PAL and PAL to NTSC conversion.
- SmartZoom ™supports 4X picture enlargement and reduction
- SmartStream™ supports video bit stream error concealment.

ES4227 FEATURES

- Multi-standard TV encoder in 100-pin PQFP package supports CCIR601 non-square operation, NTSC/PAL formats, simultaneous composite and S-video output, and interlaced operation.
- Two programmable 16-bit sigma-delta audio DACs accept I^2S format data, and provide dual audio output with SNR better than 90 dB.
- Dual microphone input and vocal assist hardware support provided.
- PLL clock synthesizer based on 27 MHz crystal input generates required clocks for video encoder, audio DAC, echo and surround sound, and video processor.
- Device Serial Communication (DSC) port for command issued/ register access.
- Digitally controlled echo with up to 130 ms delay.

SOFTWARE SUPPORT

- Software stack support for the POP3, SMTP and SNMP Internet e-mail protocols defined by RFC 821, RFC 1157and RFC 2449.
- Software stack support provided for the HTTP Web browsing protocol defined by RFC 1945, RFC 2068 and RFC 2616.
- Software stack support provided for the TCP/IP Internet protocols defined by RFC 791 and RFC 793.
- Software stack support provided for RTP payload format for MPEG-1/2 and H.261 video streaming protocols defined by RFC 2032, RFC 2038 and RFC 2250.
- Character generation and software support for English, Big 5/GB Chinese and Japanese fonts.
- Software support for infrared remote control and wireless keyboard.

ES4228 PINOUT

Figure 1 shows the ES4228 device pinout.

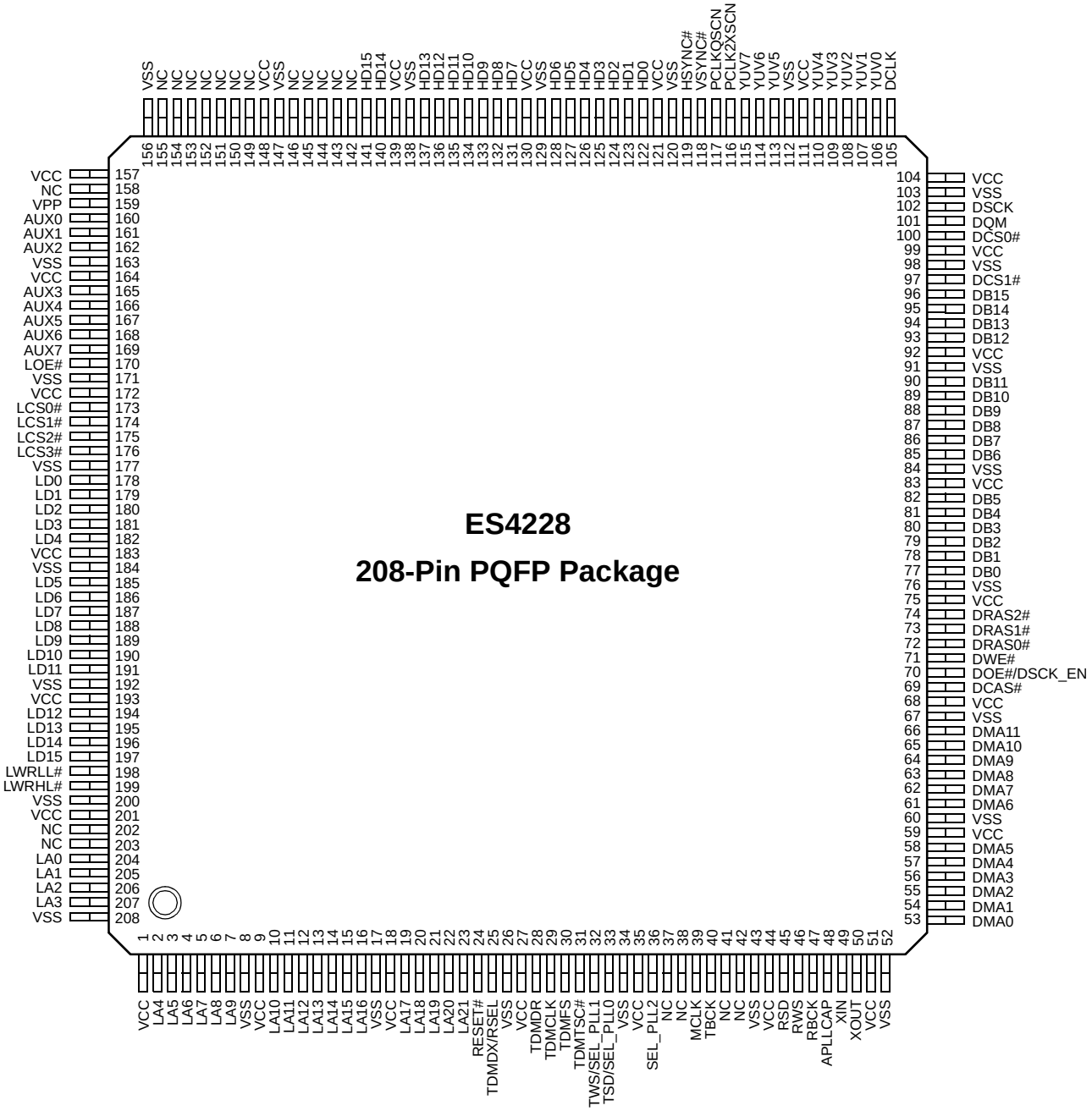

Figure 1 ES4228 Device Pinout

ES4228 PIN DESCRIPTION

Table 1 lists the pin descriptions for the ES4228.

Table 1 ES4228 Pin Descriptions List

<table>
<tr><th>Name</th><th>Number</th><th>I/O</th><th>Description</th></tr>
<tr><td>VCC</td><td>1, 9, 18, 27, 35, 44, 51, 59, 68, 75, 83, 92, 99, 104, 111, 121, 130, 139, 148, 157, 164, 172, 183, 193, 201</td><td>I</td><td>3.45 V power supply.</td></tr>
<tr><td>LA[21:0]</td><td>23:19, 16:10, 7:2, 207:204</td><td>O</td><td>Device address output.</td></tr>
<tr><td>VSS</td><td>8, 17, 26, 34, 43, 52, 60, 67, 76, 84, 91, 98, 103, 112, 120, 129, 138, 147, 156, 163, 171, 177, 184, 192, 200, 208</td><td>I</td><td>Ground.</td></tr>
<tr><td>RESET#</td><td>24</td><td>I</td><td>Reset input, active low.</td></tr>
<tr><td>TDMDX</td><td rowspan="2">25</td><td>O</td><td>TDM transmit data.</td></tr>
<tr><td>RSEL</td><td>I</td><td>ROM Select.
<table>
<tr><th>RSEL</th><th>Selection</th></tr>
<tr><td>0</td><td>8-bit ROM</td></tr>
<tr><td>1</td><td>16-bit ROM</td></tr>
</table></td></tr>
<tr><td>TDMDR</td><td>28</td><td>I</td><td>TDM receive data.</td></tr>
<tr><td>TDMCLK</td><td>29</td><td>I</td><td>TDM clock input.</td></tr>
<tr><td>TDMFS</td><td>30</td><td>I</td><td>TDM frame sync.</td></tr>
<tr><td>TDMTSC#</td><td>31</td><td>O</td><td>TDM output enable, active low.</td></tr>
<tr><td>TWS</td><td rowspan="2">32</td><td>O</td><td>Audio transmit frame sync.</td></tr>
<tr><td>SEL_PLL1</td><td>I</td><td>Refer to the description and matrix for SEL_PLL0 pin 33.</td></tr>
<tr><td>TSD</td><td rowspan="2">33</td><td>O</td><td>Audio transmit serial data port.</td></tr>
<tr><td>SEL_PLL0</td><td>I</td><td>System and DSCK output clock frequency selection at reset time. The matrix below lists the available clock frequencies and their respecitve PLL bit settings.
<table>
<tr><th>SEL_PLL2</th><th>SEL_PLL1</th><th>SEL_PLL0</th><th>Clock Output</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>VCO doesn’t work.</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>27 MHz</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Bypass mode</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>54 MHz</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>121.5 MHz</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>81 MHz</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>94.5 MHz</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>108 MHz</td></tr>
</table></td></tr>
<tr><td>SEL_PLL2</td><td>36</td><td>I</td><td>Refer to the description and matrix for SEL_PLL0 pin 33.</td></tr>
<tr><td>MCLK</td><td>39</td><td>I/O</td><td>Audio master clock for audio DAC.</td></tr>
<tr><td>TBCK</td><td>40</td><td>I/O</td><td>Audio transmit bit clock.</td></tr>
<tr><td>RSD</td><td>45</td><td>I</td><td>Audio receive serial data.</td></tr>
<tr><td>RWS</td><td>46</td><td>I</td><td>Audio receive frame sync.</td></tr>
<tr><td>RBCK</td><td>47</td><td>I</td><td>Audio receive bit clock.</td></tr>
<tr><td>APLLCAP</td><td>48</td><td>I</td><td>Analog PLL Capacitor.</td></tr>
<tr><td>XIN</td><td>49</td><td>I</td><td>Crystal input.</td></tr>
<tr><td>XOUT</td><td>50</td><td>O</td><td>Crystal output.</td></tr>
</table>

Table 1 ES4228 Pin Descriptions List (Continued)

Name	Number	I/O	Description
DMA[11:0]	66:61, 58:53	O	DRAM address bus.
DCAS#	69	O	DRAM column address strobe.
DOE#	70	O	DRAM output enable.
DSCK_EN		O	DRAM system clock enable.
DWE#	71	O	DRAM write enable.
DRAS[2:0]#	74:72	O	DRAM row address strobe.
DB[15:0]	96:93, 90:85 ,82:77	I/O	DRAM data bus.
DCS[1:0]#	97, 100	O	SDRAM chip select [1:0].
DQM	101	O	Data input/output mask.
DSCK	102	O	DRAM system clock to SDRAM.
DCLK	105	I	Clock input (bypass/test mode).
YUV[7:0]	115:113, 110:106	O	8-bit YUV output.
PCLK2XSCN	116	I/O	2X pixel clock.
PCLKQSCN	117	I/O	Pixel clock.
VSYNC#	118	I/O	Vertical sync.
HSYNC#	119	I/O	Horizontal sync.
HD[15:0]	141:140, 137:131, 128:122	I/O	Host data bus
VPP	159	I	5 V power supply.
AUX[7:0]	169:165, 162:160	I/O	Auxiliary ports.
LOE#	170	O	EPROM device output enable.
LCS[3:0]#	176:173	O	EPROM chip select [3:0].
LD[15:0]	197:194,191:185,182:178	I/O	EPROM device data bus.
LWRLL#	198	O	EPROM device low byte write enable.
LWRHL#	199	O	EPROM device high byte write enable.
NC	37, 38, 41, 42, 146:142, 155:149, 158, 203:202	—	No connect.

ES4227 PINOUT

Figure 2 shows the ES4227 device pinout.

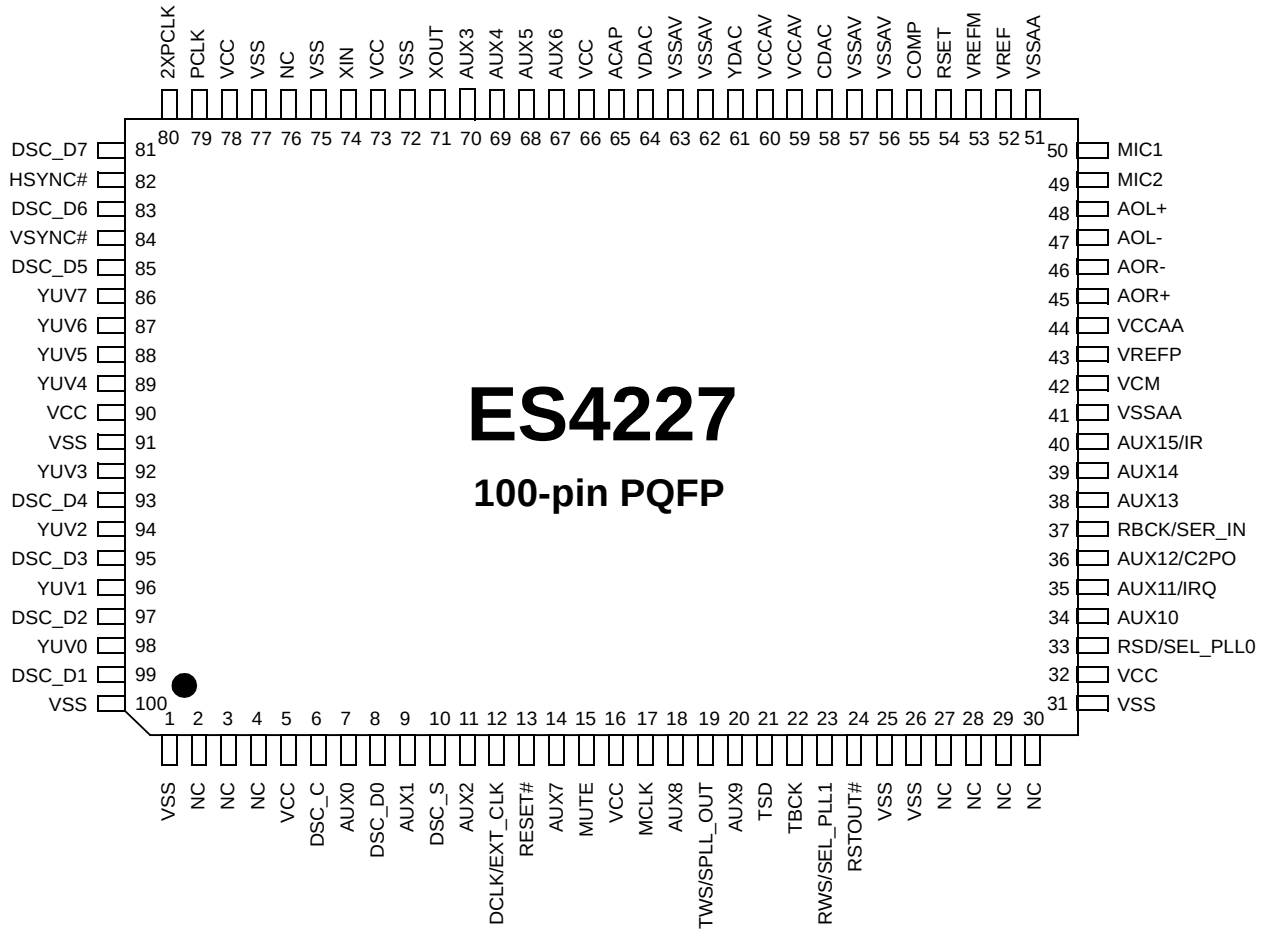

Figure 2 ES4227 Device Pinout

ES4227 PIN DESCRIPTION

Table 2 lists the pin descriptions for the ES4227.

Table 2 ES4227 Pin Descriptions List

Name	Number	I/O	Definition
VSS	1, 25:26, 31, 72, 75, 77, 91, 100	I	Ground.
VCC	5, 16, 32, 66, 73, 78, 90	I	5.0V power supply.
DSC_C	6	I	Clock for programming to access internal registers.
AUX0	7	I/O	General purpose I/O.
AUX1	9	I/O	General purpose I/O.
AUX2	11	I/O	General purpose I/O.
AUX3	70	I/O	CD loader reset.
AUX4	69	I/O	Modem DSP reset.
AUX5	68	I/O	General purpose I/O.
AUX6	67	I/O	General purpose I/O.
AUX7	14	I/O	General purpose I/O.
AUX8	18	I/O	General purpose I/O.
AUX9	20	I/O	General purpose I/O.
AUX10	34	I/O	General purpose I/O.
AUX11	35	I/O	Interrupt output to ES4228.
AUX12	36	I/O	CD loader C2PO.
AUX13	38	I/O	General purpose I/O.
AUX14	39	I/O	Interrupt input from Modem DSP.
AUX15	40	I/O	IR interrupt Input.
DSC_D[7:0]	8, 81, 83, 85, 93, 95, 97, 99	I/O	Data for programming to access internal registers.
DSC_S	10	I	Strobe for programming to access internal registers.
DCLK	12	O	Dual-purpose pin DCLK is the ES4228 clock.
EXT_CLK		I	External clock input during bypass PLL mode.
RESET#	13	I	Reset.
MUTE	15	O	Audio mute.
MCLK	17	I	Audio master clock.
TWS	19	I	Dual-purpose pin TWS is the transmit audio frame sync.
SPLL_OUT		O	SPLL_OUT is the select PLL output.
TSD	21	I	Transmit audio data input.
TBCK	22	I	Transmit audio bit clock.
RWS	23	O	Dual-purpose pin RWS is the receive audio frame sync.
SEL_PLL1		I	Pins SEL_PLL[1:0] select the PLL clock frequency for the DCLK output.
RSTOUT#	24	O	Reset output (active-low).
NC	2:4,27:30,76		No connect. Do not connect to these pins.

SEL_PLL1	SEL_PLL0	DCLK
0	0	Bypass PLL (input mode)
0	1	27 MHz (output mode) Default
1	0	32.4 MHz (output mode)
1	1	40.5 MHz (output mode)

Table 2 ES4227 Pin Descriptions List (Continued)

Name	Number	I/O	Definition
RSD	33	O	Dual-purpose pin. RSD is the receive audio data input.
SEL_PLL0		I	SEL_PLL0 along with SEL_PLL1 select the PLL clock frequency for the DCLK output. See the table for pin number 23.
RBCK	37	O	Dual-purpose pin. RBCK is the receive audio bit clock.
SER_IN		I	SER_IN is the serial input DSC mode. 0 - Parallel DSC mode. 1 - Serial DSC mode.
VSSAA	41,51	I	Audio Analog Ground.
VCM	42	I	ADC Common Mode Reference (CMR) buffer output. CMR is approximately 2.25 V. Bypass to analog ground with 47 µF electrolytic in parallel with 0.1 µF.
VREFP	43	I	DAC and ADC maximum reference. Bypass to VCMR with 10 µF in parallel with 0.1 µF.
VCCAA	44	I	Analog VCC, 5 V.
AOR+, AOR-	45, 46	O	Right channel output.
AOL-, AOL+	47, 48	O	Left channel output.
MIC2	49	I	Microphone input 2.
MIC1	50	I	Microphone input 1.
VREF	52	I	Internal resistor divider generates Common Mode Reference (CMR) voltage. Bypass to analog ground with 0.1 µF.
VREFM	53	I	DAC and ADC minimum reference. Bypass to VCMR with 10 µF in parallel with 0.1 µF.
RSET	54	I	Full scale DAC current adjustment.
COMP	55	I	Compensation pin.
VSSAV	56:57, 62:63	I	Video analog ground
CDAC	58	O	Modulated chrominance output.
VCCAV	59, 60	I	5.0V video power supply.
YDAC	61	O	Y luminance data bus for screen video port.
VDAC	64	O	Composite video output.
ACAP	65	I	Audio CAP
XOUT	71	O	27 MHz crystal output.
XIN	74	I	27 MHz crystal input.
PCLK	79	I/O	13.5 MHz pixel clock.
2XPCLK	80	I/O	Doubled 27 MHz pixel clock.
HSYNC#	82	O	Horizontal sync.
VSYNC#	84	O	Vertical sync.
YUV[7:0]	86:89, 92, 94, 96, 98	I	YUV data bus for screen video port.

SYSTEM BLOCK DIAGRAM

Figure 3 shows the ES4228/ES4227 chipset implemented in a sample system block diagram.

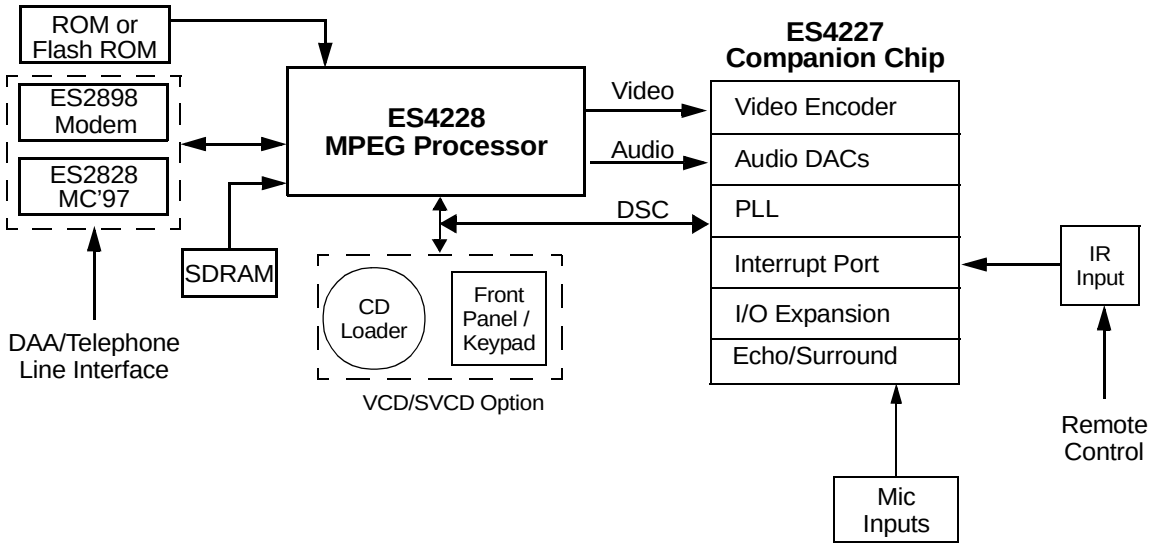

Figure 3 ES4228/ES4227 System Block Diagram

ORDERING INFORMATION

Part Number	Description	Package
ES4228	MPEG Processor	208-pin PQFP
ES4227	Video Encoder Companion Chip	100-pin PQFP

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