DAVICOM Semiconductor, Inc.

DM9103

10/100 Mbps 3-port Ethernet Switch Controller with PCI Interface

DATA SHEET

Preliminary
Version: DM9103-DS-P02
September 26, 2007

1. General Description

The DM9103 is a fully integrated, high performance, and cost-effective fast Ethernet switch controller with one general PCI bus interface, two ports 10M/100Mbps PHY, and one port MII or RMII interface.

The general PCI bus connects directly to internal host MAC with 32-bit data registers and internal memory. The host MAC has the similar functions as other 10/100Mbps PHY or MII does. This makes the DM9103 act as an extended four ports switch and to shorten the latency from PCI port to destination port.

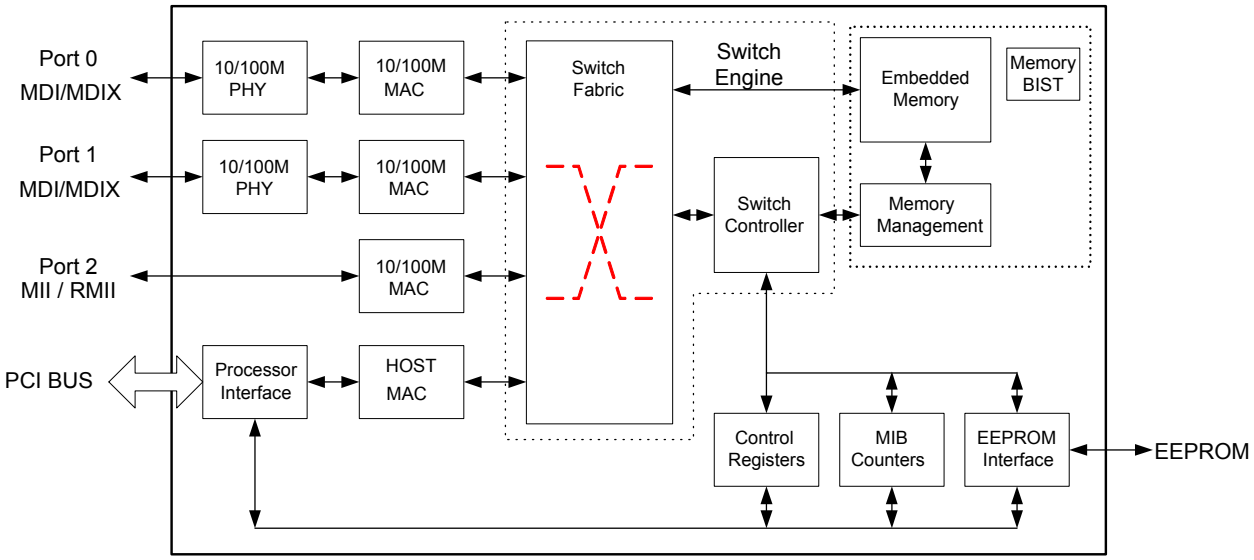
The internal memory of the DM9103 supports up to 1K uni-cast MAC address table, and provides to three ports' and PCI port's transmit and receive buffers. For efficient memory usage algorithm, if application only uses two ports solution, the another disabled port's memory resource can be shared to other two ports and PCI port.

Each port of the DM9103 provides four priority transmit queues, that can be defined by port-based, 802.1p VLAN, or IP packet ToS field automatically, to fit the various bandwidth and latency requirement of data, voice, and video applications. Each port also supports ingress and/or egress rate control to provide proper bandwidth. And up to 16 groups of 802.1Q VLAN with Tag/Un-tag functions are supported to provide efficient packet forwarding.

The TCP/UDP/IPv4 checksum generation and checking functions are also provided by PCI port to offload the processor computing loading. Besides the packet transmit and receive functions, the PCI port also provides various registers to control and get status of the DM9103 functional operation. Each port, including the PCI port, provides the MIB counters and loop-back capability and the build in memory self test (BIST) for system and board level diagnostic.

The integrated two ports PHY are compliant with IEEE 802.3u standards. The MII interface provides the flexibility to connect Ethernet PHY, and it can be configured as Reversed MII interface for SoC with MII interface. An alternative interface, the RMII interface, is also provided to connect the lower pin count Ethernet PHY or SoC with RMII interface.

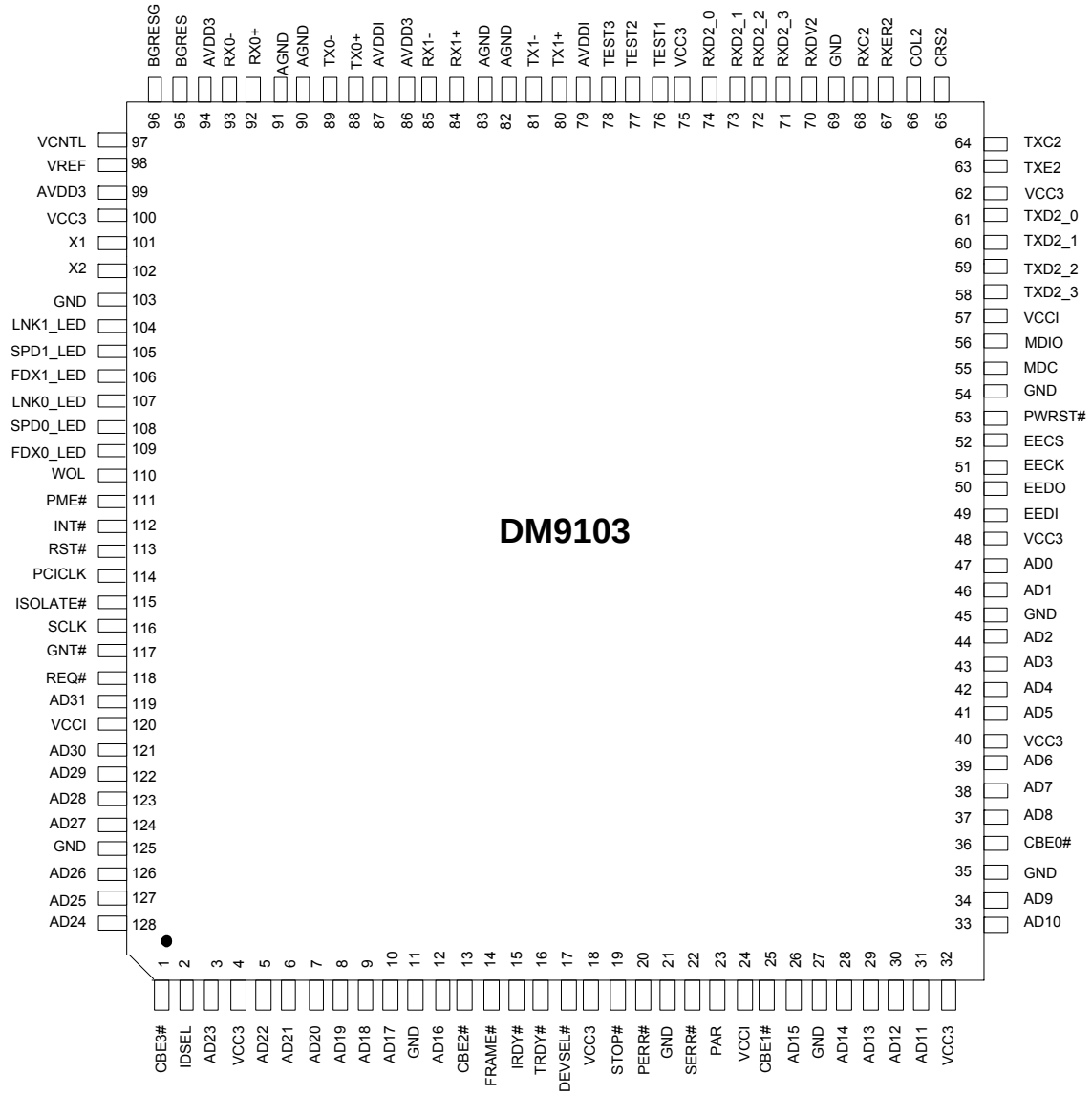
2. Block Diagram



3. Features

- Ethernet Switch with two 10/100Mb PHY, one MII/RMII, and PCI bus interface
- Support Reverse-MII
- PCI bus master architecture
- EEPROM interface for power up configurations
- Support TCP/UDP/IPv4 checksum offload
- Support HP Auto-MDIX
- Support IEEE 802.3x Flow Control in Full-duplex mode
- Support Back Pressure Flow Control in Half-duplex mode
- Per port support 4 priority queues by Port-based, 802.1P QoS, and IP TOS priority
- Support 802.1Q VLAN up-to 16 VLAN group
- Support VLAN ID tag/untag options
- Per port support bandwidth, ingress and egress rate control
- Support Broadcast Storming filter function
- Support Store and Forward switching approach
- Support up-to 1K Uni-cast MAC addresses
- Automatic aging scheme
- Support MIB counters for diagnostic
- 128-pin LQFP 1.8V internal core, 3.3V I/O with 5V tolerant

4. Pin Configuration : 128 pin LQFP



5. Pin Description

I = Input, O = Output, I/O = Input / Output, O/D = Open Drain, P = Power, PD=internal pull-low (about 50K Ohm)
# = asserted Low

5.1 PCI Bus interface

Pin No.	Pin Name	I/O	Description
2	IDSEL	I	Initialization Device Select This signal is asserted high during the Configuration Space read/write access.
14	FRAME#	I/O	Cycle Frame This signal is driven low by the DM9103 master mode to indicate the beginning and duration of a bus transaction.
15	IRDY#	I/O	Initiator Ready This signal is driven low when the master is ready to complete the current data phase of the transaction. A data phase is completed on any clock when both IRDY# and TRDY# are sampled asserted.
16	TRDY#	I/O	Target Ready This signal is driven low when the target is ready to complete the current data phase of the transaction. During a read, it indicates that valid data is asserted. During a write, it indicates that the target is prepared to accept data.
17	DEVSEL#	I/O	Device Select The DM9103 asserts the signal low when it recognizes its target address after FRAME# is asserted. As a bus master, the DM9103 will sample this signal which insures its destination address of the data transfer is recognized by a target.
19	STOP#	I/O	Stop This signal is asserted low by the target device to request the master device to stop the current transaction.
20	PERR#	I/O	Parity Error The DM9103 as a master or slave will assert this signal low to indicate a parity error on any incoming data.
22	SERR#	I/O	System Error This signal is asserted low when address parity is detected with enabled PCICS bit31 (detected parity error.) The system error asserts two clock cycles after the falling address if an address parity error is detected.
23	PAR	I/O	Parity This signal indicates even parity across AD0~AD31 and C/BE0#~C/BE3# including the PAR pin. This signal is an output for the master and an input for the slave device. It is stable and valid one clock after the address phase.
1,13,25,36	C/BE3# C/BE2# C/BE1# C/BE0#	I/O	Bus Command/Byte Enable During the address phase, these signals define the bus command or the type of bus transaction that will take place. During the data phase these pins indicate which byte lanes contain valid data. C/BE0# applies to bit7-0 and C/BE3# applies to bit31-24.

119,121,122,123,124,126,127,128, 3,5,6,7,8,9,10,12, 26,28,29,30,31,33,34,37, 38,39,41,42,43,44,46,47	AD31~AD0	I/O	Address & Data These are multiplexed address and data bus signals. As a bus master, the DM9103 will drive address during the first bus phase. During subsequent phases, the DM9103 will either read or write data expecting the target to increment its address pointer. As a target, the DM9103 will decode each address on the bus and respond if it is the target being addressed.
110	WOL	O	Issue a wake up signal when wake up event occurred.
111	PME#	O/D	Power Management Event. The DM9103 drives it low to indicate that a power management event has occurred.
112	INT#	O/D	Interrupt Request This signal will be asserted low when an interrupted condition as defined in CR5 is set, and the corresponding mask bit in CR7 is set.
113	RST#	I	System Reset When this signal is low, the DM9103 performs the internal system reset to its initial state.
114	PCICLK	I	PCI system clock PCI bus clock that provides timing for DM9103 related to PCI bus transactions.
115	ISOLATE#	I	Isolate This pin is used to isolate the DM9103 from the PCI bus.
117	GNT#	I	Bus Grant This signal is asserted low to indicate that DM9103 has been granted ownership of the bus by the central arbiter.
118	REQ#	O	Bus Request The DM9103 will assert this signal low to request the ownership of the bus.

5.2 P2 MII / RMII / Reverse MII Interfaces

5.2.1 MII Interfaces

Pin No.	Pin Name	I/O	Description
55	MDC	O,PD	MII Serial Management Data Clock
56	MDIO	I/O	MII Serial Management Data
58,59,60,61	TXD2_3~0	O,PD	Port 2 MII Transmit Data 4-bit nibble data outputs (synchronous to the TXC2)
63	TXE2	O,PD	Port 2 MII Transmit Enable
64	TXC2	I/O	Port 2 MII Transmit Clock.
65	CRS2	I/O	Port 2 MII Carrier Sense
66	COL2	I/O	Port 2 MII Collision Detect.
67	RXER2	I	Port 2 MII Receive Error
68	RXC2	I	Port 2 MII Receive Clock
70	RXDV2	I	Port 2 MII Receive Data Valid
71,72,73,74	RXD2_3~0	I	Port 2 MII Receive Data 4-bit nibble data input (synchronous to RXC2)

5.2.2 RMII Interfaces

Pin No.	Pin Name	I/O	Description
55	MDC	O,PD	MII Serial Management Data Clock
56	MDIO	I/O	MII Serial Management Data
58,59	TXD2_3~2	O	Reserved
60,61	TXD2_1~0	O,PD	RMII Transmit Data
63	TXE2	O,PD	RMII Transmit Enable.
64	TXC2	O	Reserved
65	CRS2	I	RMII CRS_DV
66	COL2	I	Reserved
67	RXER2	I	Reserved
68	RXC2	I	50MHz reference clock.
70	RXDV2	I	Reserved
71,72	RXD2_3~2	I	Reserved
73,74	RXD2_1~0	I	RMII Receive Data.

5.2.3 Reverse MII Interfaces

Pin No.	Pin Name	I/O	Description
55	MDC	O,PD	Reserved
56	MDIO	I/O	Reserved
58,59,60,61	TXD2_3~0	O,PD	Port 2 MII Transmit Data 4-bit nibble data outputs (synchronous to the TXC2)
63	TXE2	O,PD	Port 2 MII Transmit Enable
64	TXC2	O	25MHz clock output
65	CRS2	O	Port 2 carrier sense output when TXE2 or RXDV2 asserted.
66	COL2	O	Port 2 collision output when TXE2 and RXDV2 asserted.
67	RXER2	I	Port 2 MII Receive Error
68	RXC2	I	Port 2 MII Receive Clock
70	RXDV2	I	Port 2 MII Receive Data Valid
71,72,73,74	RXD2_3~0	I	Port 2 MII Receive Data 4-bit nibble data input (synchronous to RXC2)

5.3 EEPROM Interfaces

Pin No.	Pin Name	I/O	Description
49	EEDI	I,PD	EEPROM Data In
50	EEDO	O,PD	EEPROM Data Out This pin is used serially to write op-codes, addresses and data into the EEPROM.
51	EECK	O,PD	EEPROM Serial Clock This pin is used as the clock for the EEPROM data transfer.
52	EECS	O,PD	EEPROM Chip Selection.

5.4 LED Pins

Pin No.	Pin Name	I/O	Description
104	LNK1_LED	O/D	Port 1 Link / Active LED It is the combined LED of link and carrier sense signal of the internal PHY1
105	SPD1_LED	O/D	Port 1 Speed LED Its low output indicates that the internal PHY1 is operated in 100M/S, or it is floating for the 10M mode of the internal PHY1
106	FDX1_LED	O/D	Port 1 Full-duplex LED Its low output indicates that the internal PHY1 is operated in full-duplex mode, or it is floating for the half-duplex mode of the internal PHY1
107	LNK0_LED	O/D	Port 0 Link / Active LED It is the combined LED of link and carrier sense signal of the internal PHY0
108	SPD0_LED	O/D	Port 0 Speed LED Its low output indicates that the internal PHY0 is operated in 100M/S, or it is floating for the 10M mode of the internal PHY0
109	FDX0_LED	O/D	Port 0 Full-duplex LED Its low output indicates that the internal PHY0 is operated in full-duplex mode, or it is floating for the half-duplex mode of the internal PHY0

5.5 Clock Interface

Pin No.	Pin Name	I/O	Description
101	X1	I	Crystal 25MHz In
102	X2	O	Crystal 25MHz Out
116	SCLK	I	External system clock source If strap pin EECS is pulled high, this pin is used for DM9103 system clock. The frequency range is between 20MHz and 100MHz depend on application.

5.6 Network Interface

Pin No.	Pin Name	I/O	Description
80,81	TX1+/-	I/O	Port 1 TP TX These two pins are the Twisted Pair transmit in MDI mode or receive in MDIX mode.
84,85	RX1+/-	I/O	Port 1 TP RX These two pins are the Twisted Pair receive in MDI mode or transmit in MDIX mode.
88,89	TX0+/-	I/O	Port 0 TP TX These two pins are the Twisted Pair transmit in MDI mode or receive in MDIX mode.
92,93	RX0+/-	I/O	Port 0 TP RX

			These two pins are the Twisted Pair receive in MDI mode or transmit in MDIX mode.
95	BGRES	I/O	Bandgap Pin Connect a 1.4K resistor to BGGND in application.
96	BGGND	P	Bandgap Ground
97	VCNTL	I/O	1.8V Voltage control
98	VREF	O	Voltage Reference Connect a 0.1u capacitor to ground in application.

5.7 Miscellaneous Pins

Pin No.	Pin Name	I/O	Description
53	PWRST#	I	Power on Reset Low active with minimum 1ms
76	TEST1	I,PD	Tie to high in application
77	TEST2	I,PD	0: 3-port mode All ports are active in this mode. 1: 2-port mode Only 2 ports are active in this mode. Port 1 or port 2 can be disabled by strap TXEN2. In this mode, the memory resource is shared by PCI bus port and the other 2 ports.
78	TEST3	I,PD	Tie to ground in application

5.8 Power Pins

Pin No.	Pin Name	I/O	Description
4,18,32,40,48,62,75,100	VCC3	P	Digital 3.3V
24,57,120	VCCI	P	Internal 1.8V core power
11,21,27,35,45, 54,69,103,125	GND	P	Digital GND
86,94,99	AVDD3	P	Analog 3.3V power
79,87	AVDDI	P	Analog 1.8V power
82,83,90,91	AGND	P	Analog GND

5.9 Strap pins table

1: pull-high 1K~10K, 0: default floating.

5.9.1 Strap pin in 3-port mode

Pin No.	Pin Name	Description
52	EECS	Source of System Clock 0: system clock is internal 50MHz clock 1: use SCLK pin as system clock
50	EEDO	When Port 2 in force status mode 0: Port 2 in 100Mbps 1: Port 2 in 10Mbps
58	TXD2_3	When Port 2 in force status mode 0: link ON 1: link OFF
59	TXD2_2	0: Port 2 status from external PHY 1: Port 2 status in force mode
60,51	TXD2_1,EECK	00: Port 2 is MII mode (Default) 01: Port 2 is in reverse MII mode 10: Port 2 is in RMII mode and memory BIST disabled 11: Port 2 is in RMII mode
61	TXD2_0	When Port 2 in force status mod 0: Port 2 in full duplex mode 1: Port 2 I half duplex mode

5.9.2 strap pin in 2-port mode

Pin No.	Pin Name	Description
52	EECS	Source of System Clock 0: system clock is internal 50MHz clock 1: use SCLK pin as system clock
50	EEDO	When Port 2 in force status mode 0: Port 2 in 100Mbps 1: Port 2 in 10Mbps
58	TXD2_3	When Port 2 in force status mode 0: link ON 1: link OFF
59	TXD2_2	0: Port 2 status from external PHY 1: Port 2 status in force mode
60,51	TXD2_1,EECK	00: Port 2 is MII mode (Default) 01: Port 2 is in reverse MII mode 10: Port 2 is in RMII mode and memory BIST disabled 11: Port 2 is in RMII mode
61	TXD2_0	When Port 2 in force status mod 0: Port 2 in full duplex mode 1: Port 2 I half duplex mode
63	TXEN2	0: port 2 disabled 1: port 1 disabled

6. Register Set

6.1 PCI Configuration Registers

The definitions of PCI Configuration Registers are based on the PCI specification revision 2.2 and it provides the initialization and configuration information to operate the PCI interface in the DM9103. All registers can be accessed with byte, word, or double word mode. As defined in PCI specification 2.1, read accesses to reserve or unimplemented registers will return a value of "0." These registers are to be described in the following sections.

The default value of PCI configuration registers after reset.

Description	Identifier	Address Offset	Value of Reset
Identification	PCIID	00H	90131282H
Command & Status	PCICS	04H	02100000H*
Revision	PCIRV	08H	02000010H
Miscellaneous	PCILT	0CH	BIOS determine
I/O Base Address	PCIIO	10H	System allocate
Memory Base Address	PCIMEM	14H	System allocate
Reserved	-------	18H - 28H	00000000H
Subsystem Identification	PCISID	2CH	load from EEPROM
Reserved	-------	30H	00000000H
Capabilities Pointer	Cap _Ptr	34H	00000050H
Reserved	-------	38H	00000000H
Interrupt & Latency	PCIINT	3CH	System allocate bit7~0
Device Specific Configuration Register	PCIUSR	40H	00000000H**
Power Management Register	PCIPMR	50H	C0310001H**
Power Management Control & Status	PMCSR	54H	00000100H

* It is written to 02100007H by most BIOS.

** It may be changed from EEPROM in application.

Key to Default

In the register description that follows, the default column takes the form <Reset Value>

Where:

<Reset Value>:

1 Bit set to logic one

0 Bit set to logic zero

X No default value

<Access Type>:

RO = Read only

RW = Read/Write

R/C: means Read / Write & Write "1" for Clear.

6.1.1 Identification ID (xxxxxx00H - PCIID)

Bit	Default	Type	Description
16:31	9013H	RO	The field identifies the particular device. Unique and fixed number for the DM9103 is 9013H.
0:15	1282H	RO	This field identifies the manufacturer of the device. Unique and fixed number for Davicom is 1282H.

6.1.2 Command & Status (xxxxxx04H - PCICS)

Bit	Default	Type	Description
31	0	R/C	Detected Parity Error The DM9103 samples the AD[0:31], C/BE[0:3]#, and the PAR signal to check parity and to set parity errors. In slave mode, the parity check falls on command phase and data valid phase (IRDY# and TRDY# both active). In master mode, the DM9103 will check each data phase, during a memory read cycle, for parity error. During a memory write cycle, if an error occurs, the PERR# signal will be driven by the target. This bit is set by the DM9103 and cleared by writing "1". There is no effect by writing "0"
30	0	R/C	Signal For System Error This bit is set when the SERR# signal is driven by the DM9103. This system error occurs when an address parity is detected under the condition that bit 8 and bit 6 in command register below are set
29	0	R/C	Master Abort Detected This bit is set when the DM9103 terminates a master cycle with the master-abort bus transaction
28	0	R/C	Target Abort Detected This bit is set when the DM9103 terminates a master cycle due to a target-abort signal from other targets
27	0	R/C	Send Target Abort (0 for No Implementation) The DM9103 will never assert the target-abort sequence
26:25	01	R/C	DEVSEL Timing (01 Select Medium Timing) Medium timing of DEVSEL# means the DM9103 will assert DEVSEL# signal two clocks after FRAME# is sample “asserted”
24	0	R/C	Data Parity Error Detected This bit will take effect only when operating as a master and when a Parity Error Response Bit in command configuration register is set. It is set under two conditions: (i) PERR# asserted by the DM9103 in memory data read error (ii) PERR# sent from the target due to memory data write error
23	0	RO	Slave Mode Fast Back-To-Back Capable (0 for No Support) This bit is always reads "1" to indicate that the DM9103 is capable of accepting fast back-to-back transaction as a slave mode device
22	0	RO	User-Definable Feature Supported (0 for No Support)
21	0	RO	66 MHz (0 for No Capability)
20	1	RO	New Capability This bit indicates whether this function implements a list of extended capabilities.

19:10	0	RO	Reserved
9	0	RO	Master Mode Fast Back-To-Back (0 for No Support) The DM9103 does not support master mode fast back-to-back capability and will not generate fast back-to-back cycles
8	0	RW	SERR# Driver Enable/Disable This bit controls the assertion of SERR# signal output. The SERR# output will be asserted on detection of an address parity error and if both this bit and bit 6 are set
7	0	RO	Address/Data Stepping (0 for No Stepping)
6	0	RW	Parity Error Response Enable/Disable Setting this bit will enable the DM9103 to assert PERR# on the detection of a data parity error and to assert SERR# for reporting address parity error
5	0	RO	VGA Palette Snooping (0 for No Support)
4	0	RO	Memory Write and Invalid (0 for No Implementation) The DM9103 only generates memory write cycle
3	0	RO	Special Cycles (0 for No Implementation)
2	1	RW	Master Device Capability Enable/Disable When this bit is set, DM9103 has the ability of master mode operation
1	1	RW	Memory Space Access Enable/Disable This bit controls the ability of memory space access. The memory access includes memory mapped I/O access and Boot ROM access. As the system boots up, this bit will be enabled by BIOS for Boot ROM memory access. While in normal operation, using memory mapped I/O access, this bit should be set by driver before memory access cycles
0	1	RW	I/O Space Access Enable/Disable This bit controls the ability of I/O space access. It will be set by BIOS after power on

6.1.3 Revision ID (xxxxxx08H - PCIRV)

Bit	Default	Type	Description
31:8	020000H	RO	Class Code (020000H) This is the standard code for Ethernet LAN controller
7:4	0001	RO	Revision Major Number This is the silicon-major revision number that will increase for the subsequent versions of the DM9103
3:0	0000	RO	Revision Minor Number This is the silicon-minor revision number that will increase for the subsequent versions of the DM9103

6.1.4 Miscellaneous Function (xxxxxx0cH - PCILT)

Bit	Default	Type	Description
31:24	00H	RO	Built In Self Test (00H means No Implementation)
23:16	00H	RO	Header Type (00H means single function with Predefined Header Type).
15:8	00H	RW	Latency Timer For The Bus Master The latency timer is guaranteed by the system and measured by clock cycles. When the FRAME# is asserted at the beginning of a master period by the DM9103, the value will be copied into a counter and start counting down. If the FRAME# is de-asserted prior to count expiration, this value is meaningless. When the count expires before GNT# is de-asserted, the master transaction will be terminated as soon as the GNT# is removed While GNT# signal is removed and the counter is non-zero, the DM9103 will continue with its data transfers until the count expires. The system host will read MIN_GNT and MAX_LAT registers to determine the latency requirement for the device and then initialize the latency timer with an appropriate value The reset value of Latency Timer is determined by BIOS
7:0	00H	RO	Cache Line Size For Memory Read Mode Selection (00H means No Implementation For Use)

6.1.5 I/O Base Address (xxxxxx10H - PCIIO)

Bit	Default	Type	Description
31:7	Undefined	RW	PCI I/O Base Address This is the base address value for I/O accesses cycles. It will be compared to AD[31:7] in the address phase of bus command cycle for the I/O resource access
6:1	000000	RO	PCI I/O Range Indication It indicates that the minimum I/O resource size is 80h
0	1	RO	I/O Space Or Memory Space Base Indicator Determines that the register maps into the I/O space (= 1 Indicates I/O Base)

6.1.6 Memory Mapped Base Address (xxxxxx14H - PCIMEM)

Bit	Default	Type	Description
31:7	Undefined	R/W	PCI Memory Base Address This is the base address value for memory accesses cycles. It will be compared to the AD [31:7] in the address phase of bus command cycle for the Memory resource access
6:1	000000	RO	PCI Memory Range Indication It indicates that the minimum memory resource size is 80h
0	0	RO	I/O Space Or Memory Space Base Indicator Determines that the register maps into the memory space(= 0 Indicates Memory Base)

6.1.7 Subsystem Identification (xxxxxx2cH - PCISID)

Bit	Default	Type	Description
31:16	XXXXH	RO	Subsystem ID It can be loaded from EEPROM word 1
15:0	XXXXH	RO	Subsystem Vendor ID It can be loaded from EEPROM word 0

6.1.8 Capabilities Pointer (xxxxxx34H - Cap _Ptr)

Bit	Default	Type	Description
31:8	000000H	RO	Reserved
7:0	01010000	RO	Capability Pointer The Cap_ Ptr provides an offset (default is 50H) into the function's PCI Configuration Space for the location of the first term in the Capabilities Linked List. The Cap_ Ptr offset is double word aligned so the two least significant bits are always "0"s

6.1.9 Interrupt & Latency Configuration (xxxxxx3cH - PCIINT)

Bit	Default	Type	Description
31:24	28H	RO	Maximum Latency Timer that can be sustained.
23:16	14H	RO	Minimum Grant Minimum Length of a Burst Period.
15:8	01H	RO	Interrupt Pin read as 01H to indicate INTA#
7:0	XXH	RW	Interrupt Line that Is routed to the Interrupt Controller The value depends on system software.

6.1.10 Device Specific Configuration Register (xxxxxx40H- PCIUSR)

Bit	Default	Type	Description
31:30	0	RO	Reserved Bits Read As 0
29	0	RW	When set, enables port 0 or 1 Link Status Change Wake up Event
28	0	RO	Reserved Bit Read As 0
27	0	RW	When set, enables Magic Packet Wake up Event
26	0	RO	When set, indicates the port 0 or 1 Link Change and the Link Status Change Event occurred
25	0	RO	Reserved Bit Read As 0
24	0	RO	When set, indicates the Magic Packet is received and the Magic packet Event occurred
23:16	00H	RO	Reserved Bits Read As 0
15:8	00H	RW	Device Specific
7:0	00H	RO	Reserved Bits Read As 0

6.1.11 Power Management Register (xxxxxx50H~PCIPMR)

Bit	Default	Type	Description
31:27	11000	RO	PME_ Support This field indicates that the power states in which the function may assert PME#. A value of 0 for any bit indicates that the function is not capable of asserting the PME# signal while in that power state bit27 → PME# support D0 bit28 → PME# support D1 bit29 → PME# support D2 bit30 → PME# support D3(hot) bit31 → PME# support D3(cold) DM9103's bit31~27=11000 indicates PME# can be asserted from D3(hot) & D3(cold) These bits can be load from EEPROM word 7 bit [7:3]
26:25	00	RO	Reserved These two bits can be load from EEPROM word 7 bit [1:0]
24:22	011	RO	Aux_ Current This field reports the 3.3Vaux auxiliary current requirement for the PCI function. The default value of this field is 011 means 160mA and it can be loaded from EEPROM word 4 bit [15:13] if EEPROM word 4 bit [9] is 1
21	0	RO	Reserved This bit can be load from EEPROM word 7 bit [2]
20	0	RO	Reserved
19	0	RO	PME# Clock "0" indicates that no PCI clock is required for the function to generate PME#
18:16	010	RO	Version A default value of 010 indicates that this function complies with the Revision 1.1 of the PCI Power Management Interface Specification This value can be loaded from EEPROM word 4 bit [12:10] if EEPROM word 4 bit [9] is 1
15:8	00H	RO	Next Item Pointer The offset into the function's PCI Configuration Space pointing to the location of next item in the function's capability list is "00H"
7:0	01H	RO	Capability Identifier When "01H" indicates the linked list item as being the PCI Power Management Registers

6.1.12 Power Management Control/Status (xxxxxx54H~PMCSR)

Bit	Default	Type	Description
31:16	0000H	RO	Reserved
15	0	RW/C	PME_ Status This bit is set when the function would normally assert the PME# signal independent of the state of the PME_ En bit. Writing a "1" to this bit will clear it. This bit defaults to "0" if the function does not support PME# generation from D3 (cold).If the function supports PME# from D3 (cold) then this bit is sticky and must be explicitly cleared by the operating system whenever the operating system is initially loaded.
14:9	000000	RO	Reserved It means that the DM9103 does not support reporting power consumption.
8	1	RW	PME_ En Write "1" to enables the function to assert PME#, write "0" to disable PME# assertion This bit defaults to "0" if the function does not support PME# generation from D3 (cold) If the function supports PME# from D3(cold) then this bit is sticky and must be explicitly cleared by the operating system each time the operating system is initially loaded.
7:2	000000	RO	Reserved
1:0	00	RW	This two bits field is both used to determine the current power state of a function and to set the function into a new power state. The definitions given below 00: D0 11: D3 (hot)

6.2 PCI Control and Status Registers (CR)

The DM9103 implements 32 control and status registers, which can be accessed by the host. These CRs are double long word aligned. All CRs are set to their default values by hardware or software reset unless otherwise specified. All Control and Status Registers with their definitions and offset from IO or memory Base Address are shown below:

Register	Description	Offset from CSR Base Address	Default value after reset
CR0	System Control Register	00H	DE000000H
CR1	Transmit Descriptor Poll Demand	08H	FFFFFFFFH
CR2	Receive Descriptor Poll Demand	10H	FFFFFFFFH
CR3	Receive Descriptor Base Address Register	18H	00000000H
CR4	Transmit Descriptor Base Address Register	20H	00000000H
CR5	Network Status Report Register	28H	FC000000H
CR6	Network Operation Mode Register	30H	02040000H
CR7	Interrupt Mask Register	38H	FFFE0000H
CR8	Reserved	40H	00000000H
CR9	External Management Access Register	48H	000083F0H
CR10	Reserved	50H	FFFFFFFFH
CR11	Reserved	58H	FFFE0000H
CR12	Reserved	60H	FFFFFFXXH
CR13	Reserved	68H	XXXXXX00H
CR14	Reserved	70H	Unpredictable
CR15	Watchdog And Jabber Timer Register	78H	00000000H
CR16	SWITCH Control Register	80H	00000000H
CR17	Per Port Index Register	88H	00000000H
CR18	Per Port Control Register	90H	00000000H
CR19	Per Port Status Data Register	98H	00000000H
CR20	Per Port VLAN Tag Byte Register	A0H	00000001H
CR21	Per Port MIB counter Index Register	A8H	00000000H
CR22	MIB counter Data Register	B0H	00000000H
CR23	VLAN priority Map Register	B8H	0000FA50H
CR24-27	Port-based VLAN mapping table registers x 4	C0H-D8H	0F0F0F0FH
CR28-31	TOS Priority Map Register x 4	E0H-F8H	XXXXXXXXH

Key to Default

In the register description that follows, the default column takes the form:
<Reset Value>, <Access Type>
Where:
<Reset Value>:

1	Bit set to logic one
0	Bit set to logic zero
X	No default value

<Access Type>:
RO = Read only
RW = Read/Write
RW/C = Read/Write and Clear
WO = Write only
RO/C = Read only and cleared after read.

Reserved bits are shaded and should be written with 0.
Reserved bits are undefined on read access.

6.2.1 System Control Register (CR0)

Bit	Name	Default	Description
31:24	Reserved	DEH,RO	Reserved
25:22	Reserved	00,RO	Reserved
21	MRM	0,RW	Memory Read Multiple When set, the DM9103 will use memory read multiple command (C/BE3~0 1100) when it initialize the memory read burst transaction as a master device When reset, it will use memory read command (C/BE3 ~ 0 = 0110) for the same master operation
20	Reserved	0,RW	Reserved
19:1	Reserved	0,RO	Reserved
0	SR	0,RW	Software Reset When set, the DM9103 will make a internal reset cycle. All consequent action to DM9103 should wait at least 32 PCI clock cycles for its self-cleared.

6.2.2 Transmit Descriptor Poll Demand (CR1)

Bit	Name	Default	Description
31:0	TDP	FFFFFFFFH ,WO	Transmit Descriptor Polling Command Writing any value to this port will force DM9103 to poll the transmit descriptor. If the acting descriptor is not available, transmit process will return to suspend state. If the descriptor shows buffer available, transmit process will begin the data transfer.

6.2.3 Receive Descriptor Poll Demand (CR2)

Bit	Name	Default	Description
31:0	RDP	FFFFFFFFH ,WO	Receive Descriptor Polling Command Writing any value to this port will force DM9103 to poll the receive descriptor. If the acting descriptor is not available, receive process will return to suspend state. If the descriptor shows buffer available, receive process will begin the data transfer.

6.2.4 Receive Descriptor Base Address (CR3)

Bit	Name	Default	Description
31:0	RDBA	00000000H, RW	Receive Descriptor Base Address This register defines base address of receive descriptor-chain. The receive descriptor- polling command, after CR3 is set, will make DM9103 to fetch the descriptor at the Base-Address. This is a working register, so the value of reading is unpredictable.

6.2.5 Transmit Descriptor Base Address (CR4)

Bit	Name	Default	Description
31:0	TDBA	00000000H,RW	Transmit Descriptor Base Address This register defines base address of transmit descriptor-chain. The transmit descriptor- polling command after CR4 is set to make DM9103 fetch the descriptor at the Base-Address. This is a working register, so the value of reading is unpredictable.

6.2.6 Network Status Report Register (CR5)

Note: Bits [13:0] can be cleared by written 1 to them respectively.

Bit	Name	Default	Description
31:26	Reserved	000000,RO	Reserved
25:23	SBEB	000,RO	System Bus Error Bits These bits are read only and used to indicate the type of system bus fatal error. Valid only when System Bus Error is set. The mapping bits are shown below Bit25 Bit24 Bit23 Bus Error Type 0 0 0 Parity error 0 0 1 Master abort 0 1 0 Slave abort 0 1 1 Reserved 1 X X Reserved
22:20	TXPS	000,RO	Transmit Process State These bits are read only and used to indicate the state of transmit process The mapping table is shown below Bit22 Bit21 Bit20 Process State 0 0 0 Transmit process stopped 0 0 1 Fetch transmit descriptor 0 1 0 Move Setup Frame from the host memory 0 1 1 Move data from host memory to transmit FIFO 1 0 0 Close descriptor by clearing owner bit of descriptor 1 0 1 Waiting end of transmit 1 1 0 Transmit end and Close descriptor by writing status 1 1 1 Transmit process suspend
19:17	RXPS	000,RO	Receive Process State These bits are read only and used to indicate the state of receive process. The mapping table is shown below Bit19 Bit18 Bit17 Process State 0 0 0 Receive process stopped 0 0 1 Fetch receive descriptor 0 1 0 Wait for receive packet under buffer available 0 1 1 Move data from receive FIFO to host memory 1 0 0 Close descriptor by clearing owner bit of descriptor 1 0 1 Close descriptor by writing status 1 1 0 Receive process suspended due to buffer unavailable 1 1 1 Purge the current frame from received FIFO because of the unavailable received buffer

16	NIS	0,RW	Normal Interrupt Summary Normal interrupt includes any of the three conditions: CR5<0> – TXCI: Transmit Complete Interrupt CR5<2> – TXDU: Transmit Buffer Unavailable CR5<6> – RXCI: Receive Complete Interrupt
15	AIS	0,RW	Abnormal Interrupt Summary Abnormal interrupt includes any interrupt condition as shown below, excluding Normal Interrupt conditions. They are TXPS (bit1), TXFU (bit5), RXDU (bit7), RXPS (bit8), SBE (bit13).
14	Reserved	0,RW	Reserved
13	SBE	0,RW	System Bus Error The PCI system bus errors will set this bit. The type of system bus error is shown in CR5<25:23>.
12	LINKS	0,RO	Link Change Status This bit is set to indicate that the link status changed in port 0 or 1 PHYceiver
11	Reserved	0,RO	Reserved
10:9	Reserved	0,RO	Reserved
8	RXPS	0,RW	Receive Process Stopped This bit is set to indicate that the receive process enters the stopped state.
7	RXDU	0,RW	Receive Buffer Unavailable This bit is set when the DM9103 fetches the next receive descriptor that is still owned by the host. Receive process will be suspended until a new frame enters or the receive polling command is set.
6	RXCI	0,RW	Receive Complete Interrupt This bit is set when a received frame is fully moved into host memory and receive status has been written to descriptor. Receive process is still running and continues to fetch next descriptor.
5	TXFU	0,RW	Transmit FIFO Underrun This bit is set when transmit FIFO has underrun condition during the packet transmission. It may happen due to the heavy load on bus, cause transmit buffer unavailable before end of packet. In this case, transmit process is placed in the suspend state and underrun error TDES0<1> is set.
4	Reserved	0,RO	Reserved
3	Reserved	0,RO	Reserved
2	TXDU	0,RW	Transmit Buffer Unavailable This bit is set when the DM9103 fetches the next transmit descriptor that is still owned by the host. Transmit process will be suspended until the transmission polling command is set.
1	TXPS	0,RW	Transmit Process Stopped This bit is set to indicate transmit process enters the stopped state.
0	TXCI	0,RW	Transmit Complete Interrupt This bit is set when a frame is fully transmitted and transmit status has been written to descriptor (the TDES1<31> is also asserted). Transmit process is still running and continues to fetch next descriptor.

6.2.7 Network Operation Mode Register (CR6)

Bit	Name	Default	Description
31	Reserved	0,RO	Must be Zero
30:29	Reserved	0,RO	Reserved
28:25	Reserved	0001,RO	0001: normal mode 0011: memory test mode (CR13/14 enable)
24:23	Reserved	00,RO	Must be Zero
22	Reserved	0,RO	Reserved
21	Reserved	0,RO	Reserved
20	Reserved	0,RW	Reserved
19	Reserved	0,RW	Reserved
18	Reserved	0,RO	Reserved
17	MII_CNTL	0,RW	MII Management Pin Control Set this bit to enable CR9 bit 16~19 to control MII management pin (MDC,MDIO)
16	1PKT	0,RW	One Packet Mode When this bit is set, only one packet is stored at TX FIFO
15:14	Reserved	0,RO	Reserved
13	TXSC	0,RW	Transmit Start/Stop Command When set, the transmit process will begin by fetching the transmit descriptor for available packet data to be transmitted (running state). If the fetched descriptor is owned by the host, transmit process will enter the suspend state and transmit buffer unavailable (CR5<2>) is set. Otherwise it will begin to move data from host to FIFO and transmit out after reaching threshold value. When reset, the transmit process is placed in the stopped state after completing the transmission of the current frame.
12	Reserved	0,RO	Reserved
11:10	LBM	0,RW	Loop-back Mode These bits decide two loop-back modes, MAC and PHY, besides normal operation. These loop-back modes expect transmitted data back to receive path and ignore collision detection. Bit11 Bit10 Loop-back Mode 0 0 Normal 0 1 Internal loop-back 1 X Reserved
9	Reserved	0,RO	Reserved
8	Reserved	0,RO	Must be Zero
7	PAM	0,RW	Pass All Multicast When set, any packet with a multicast destination address is received by the DM9103. The packet with a physical address will also be filtered based on the filter mode setting
6	PM	0,RW	Promiscuous Mode When set, any incoming valid frame is received by the DM9103, and no matter what the destination address is. The DM9103 is initialized to this mode after reset operation.
5	Reserved	0,RW	Must be Zero.

4	IAFM	0,RO	Inverse Address Filtering Mode It is set to indicate the DM9103 operate in a Inverse Filtering Mode. This is a only bit and mapped from the setup frame together with CR6<2>, CR6<0> setting. That is it is valid only during perfect filtering mode.
3	PBF	0,RW	Pass Bad Frame When set, the DM9103 is indicated to receive the bad frames including runt packets, truncated frames caused by the FIFO overflow. The bad frame also has to pass the address filtering if the DM9103 is not set in promiscuous mode.
2	HOFM	0,RO	Hash-only Filter Mode This is a read-only bit and mapped from the set-up frame together with bit4,0 of CR6.It is set to indicate the DM9103 operate in a Hash-only Filtering Mode.
1	RXRC	0,RW	Receive Start/Stop Command When set, the receive process will begin by fetching the receive descriptor for available buffer to store the new-coming packet (placed in the running state). If the fetched descriptor is owned by the host (no descriptor is owned by the DM9103), the receive process will enter the suspend state and receive buffer unavailable CR5<7> sets. Otherwise it runs to wait for the packet's income. When reset, the receive process is placed in the stopped state after completing the reception of the current frame.
0	HPFM	0,RO	Hash/Perfect Filter Mode This is a read only bit and mapped from the setup frame together with CR6<4>, CR6<2>. When reset, the DM9103 does a perfect address filter of incoming frames according to the addresses specified in the setup frame. When set, the DM9103 does a imperfect address filtering for the incoming frame with a multicast address according to the hash table specified in the setup frame. The filtering mode (perfect/imperfect) for the frame with a physical address will depend on CR6<2>.

6.2.8 Interrupt Mask Register (CR7)

Bit	Name	Default	Description
16	NISE	0,RW	Normal Interrupt Summary Enable This bit is set to enable the interrupt for Normal Interrupt Summary. Normal interrupt includes three conditions: CR5<0> – TXCI: Transmit Complete Interrupt CR5<2> – TXDU: Transmit Buffer Unavailable CR5<6> – RXCI: Receive Complete Interrupt
15	AISE	0,RW	Abnormal Interrupt Summary Enable This bit is set to enable the interrupt for Abnormal Interrupt Summary. Abnormal interrupt includes all interrupt conditions as shown below, excluding Normal Interrupt conditions. They are TXPS(bit1), TXFU(bit5), RXDU(bit7), RXPS(bit8), SBE(bit13).
14	Reserved	0,RW	Reserved
13	SBEE	0,RW	System Bus Error Enable When set together with CR7<15>, CR5<13>, it enables the interrupt for System Bus Error. The type of system bus error is shown in CR5<24:23>.
12	LINKE	0,RW	Link Change Interrupt Enable When this bit and CR7<16>, CR5<12> are set together, it will enable the interrupt of link status changed from port 0 or 1 PHYceiver.
11	Reserved	0,RW	Reserved
10:9	Reserved	0,RO	Reserved
8	RXPSE	0,RW	Receive Process Stopped Enable When set together with CR7<15> and CR5<8>. This bit is set to enable the interrupt of receive process stopped condition.
7	RXDUE	0,RW	Receive Buffer Unavailable Enable When this bit and CR7<15>, CR5<7> are set together, it will enable the interrupt of receive buffer unavailable condition.
6	RXCIE	0,RW	Receive Complete Interrupt Enable When this bit and CR7<16>, CR5<6> are set together, it will enable the interrupt of receive process complete condition.
5	TXFUE	0,RW	Transmit FIFO Underrun Enable When set together with CR7<15>, CR5<5>, it will enable the interrupt of transmit FIFO underrun condition.
4	Reserved	0,RO	Reserved
3	Reserved	0,RO	Reserved
2	TXDUE	0,RW	Transmit Buffer Unavailable Enable When this bit and CR7<16>, CR5<2> are set together, the interrupt of transmit buffer unavailable is enabled.
1	TXPSE	0,RW	Transmit Process Stopped Enable When this bit is set together with CR7<15> and CR5<1>, it will enable the interrupt of the transmit process to stop.
0	TXCIE	0,RW	Transmit Complete Interrupt Enable When this bit and CR7<16>, CR5<0> are set, the transmit interrupt is enabled.

6.2.9 Reserved (CR8)

6.2.10 Management Access Register (CR9)

Bit	Name	Default	Description
31:22	Reserved	0,RO	Reserved
21	LES	0,RO	Load EEPROM status It is set to indicate the load of EEPROM is in progress.
20	RLM	0,RW	Reload EEPROM Set to reload the content of EEPROM.
19	MDIN	0,RO	MII Management Data_In This is a read-only bit to indicate the MDIO input data, when bit 18 MRW is set.
18	MRW	0,RW	MII Management Read/Write Mode Selection This bit defines the Read/Write Mode for PHY MII management register access. 1 for read and 0 for write.
17	MDOUT	0,RW	MII Management Data_Out This bit is used to generate the output data signal for PHY MII management register access.
16	MDCLK	0,RW	MII Management Clock This bit is used to generate the output clock signal for PHY MII management register access.
15	Reserved	1,RO	Reserved.
14	Reserved	0,RO	Reserved.
13:12	Reserved	0,RO	Reserved.
11	ERS	0,RW	EEPROM Selected This bit is used to enable EEPROM access.
10:8	Reserved	011,RW	Reserved
7:4	Reserved	FH,RO	Reserved
3	CRDOUT	0,RW	Data_Out from EEPROM This bit reflects the status of EEDI pin when the EEPROM access is enabled.
2	CRDIN	0,RW	Data_In to EEPROM This bit maps to EEDO pin when the EEPROM access is enabled.
1	CRCLK	0,RW	Clock to EEPROM This bit maps EECK pin when the EEPROM access is enabled
0	CRCS	0,RW	Chip_Select to EEPROM This bit maps to EECS pin when the EEPROM access is enabled

6.2.11 Reserved (CR10)

6.2.12 Reserved (CR11)

6.2.13 Reserved (CR12)

6.2.14 (Reserved CR13)

6.2.15 (Reserved CR14)

6.2.16 Checksum Offload Control Register (CR15)

Bit	Name	Default	Description
31	TXSUMC	0,WO	in transmit, generate IP/TCP/UDP chksum depend-on TX desc. control
30	IPSUM	0,WO	in transmit, generate IP chksum to all packets
29	TCPSUM	0,WO	in transmit, generate TCP chksum to all packets
28	UDPSUM	0,WO	in transmit, generate UDP chksum to all packets
27	RXSUM	0,WO	In receiving, report IP/TCP/UDP checksum status to RDES0
26:0	Reserved	0,RO	Reserved

6.12.17 Switch Control Register (CR16)

Bit	Name	Default	Description
31:16	RESERVED	0,RW	Reserved
15	TOS6	0,RW	Full ToS Using Enable 1: check most significant 6-bit of TOS 0: check most significant 3-bit only of TOS
14	RESERVED	0,RO	Reserved
13	UNICAST	0,RW	Unicast packet can across VLAN boundary
12	VIDFF	0,RW	Replace VIDFF If the received packet is a tagged VLAN with VID equal to “FFF”, its VLAN field is replaced with VLAN tag defined in CR20 bit 15~0.
11	VID1	0,RW	Replace VID01 If the received packet is a tagged VLAN with VID equal to “001”, its VLAN field is replaced with VLAN tag defined in CR20 bit 15~0.
10	VID0	0,RW	Replace VID0 If the received packet is a tagged VLAN with VID equal to “000”, its VLAN field is replaced with VLAN tag defined in CR20 bit 15~0.
9	PRI	0,RW	Replace priority field in the tag with value define in CR20 bit 15~13.
8	VLAN	0,RW	VLAN mode enable 1: 802.1Q base VLAN mode enable 0: port-base VLAN
7	MEM_BIST	0,RO	Address Memory Test BIST Status 0: OK 1: Fail
6	RST_SW	0,RW	Reset Switch Core and auto clear after 10us
5	RST_ANLG	0,RW	Reset Analog PHY Core and auto clear after 10us

4:3	SNF_PORT	00,RW	Sniffer Port Number Define the port number to act as the sniffer port
2	CRC_DIS	PE0,RW	CRC Checking Disable When set, the received CRC error packet also accept to receive memory
1:0	AGE	PE0,RW	Address Table Aging 00: no aging 01: 64sec 10: 128sec 11: 256sec

6.2.18 Per Port Index Register (CR17)

Bit	Name	Default	Description
31:8	Reserved	0,RO	Reserved
7:6	MONITOR	00,RW	Reserved, 00 in application.
5	BLOCK	0,RW	1: for write CR20[31:16] BLOCK mode
4:2	Reserved	0,RO	Reserved
1:0	INDEX	0,RW	Port index for register CR17~22 Write the port number to this register before write/read register CR17~22. Note that the processor port INDEX number is 3

6.2.19 Per Port Control Register (CR18)

Bit	Name	Default	Description
31	TAG_OUT	0,RW	Output Packet Tagging Enable The transmitted packets contain VLAN tagged field
30	PRI_DIS	0,RO	Priority Queue Disable Only one transmit queue is supported in this port.
29	WFQUE	0,RW	Weighted Fair Queuing 1: The priority weight for queue 3,2,1, and 0 is 8,4,2, and 1 respectively. 0: The queue 3 has the highest priority, and the next priorities are queue 2,1, and 0 respectively.
28	TOS_PRI	0,RW	Priority ToS over VLAN If a IP packet with VLAN tag, the priority of this packet is decode from ToS field.
27	TOS_OFF	0,RW	ToS Priority Classification Disable The priority information from ToS field of IP packet is ignored.
26	PRI_OFF	0,RW	802.1 p Priority Classification Disable The priority information from VLAN tag field is ignored.
25:24	P_PRI	0,RW	Port Base priority The priority queue number in port base. 00= queue 0, 01=queue 1, 10=queue 2, 11=queue 3

23:20	BSTH	0,RW	Broadcast Storm Threshold These bits define the bandwidth threshold that received broadcast packets over the threshold are discarded 0000: no broadcast storm control 0001: 8K packets/sec 0010: 16K packets/sec 0011: 64K packets/sec 0100: 5% 0101: 10% 0110: 20% 0111: 30% 1000: 40% 1001: 50% 1010: 60% 1011: 70% 1100: 80% 1101: 90% 111X: no broadcast storm control
19:16	BW CTRL	0,RW	Received packet length counted. Bandwidth table below. These bits define the bandwidth threshold that transmitted or received packets over the threshold are discarded 000X: none 0000: none 0001: 64Kbps 0010: 128Kbps 0011: 256Kbps 0100: 512Kbps 0101: 1Mbps 0110: 2Mbps 0111: 4Mbps 1000: 8Mbps 1001: 16Mbps 1010: 32Mbps 1011: 48Mbps 1100: 64Mbps 1101: 72Mbps 1110: 80Mbps 1111: 88Mbps

15:12	INGRESS	0,RW	Ingress Rate Control These bits define the bandwidth threshold that received packets over the threshold are discarded. 0000: none 0001: 64Kbps 0010: 128Kbps 0011: 256Kbps 0100: 512Kbps 0101: 1Mbps 0110: 2Mbps 0111: 4Mbps 1000: 8Mbps 1001: 16Mbps 1010: 32Mbps 1011: 48Mbps 1100: 64Mbps 1101: 72Mbps 1110: 80Mbps 1111: 88Mbps
11:8	EGRESS	0,RW	Egress Rate Control These bits define the bandwidth threshold that transmitted packets over the threshold are discarded. 0000: none 0001: 64Kbps 0010: 128Kbps 0011: 256Kbps 0100: 512Kbps 0101: 1Mbps 0110: 2Mbps 0111: 4Mbps 1000: 8Mbps 1001: 16Mbps 1010: 32Mbps 1011: 48Mbps 1100: 64Mbps 1101: 72Mbps 1110: 80Mbps 1111: 88Mbps
7	RESERVED	0,RO	Reserved
6	PARTI_EN	0,RW	Enable Partition Detection
5	NO_DIS_RX	0,RW	Not Discard RX Packets when Ingress Bandwidth Control When received packets bandwidth reach Ingress bandwidth threshold, the packets over the threshold are not discarded but with flow control.
4	FLOW_DIS	0,RW	Flow control in full duplex mode, or back pressure in half duplex mode enable 0 – enable 1 – disable
3	BANDWIDTH	0,RW	Bandwidth Control 0: Control with Ingress and Egress separately in bit 15~12 and bit 11~8. 1: Control with Ingress or Egress in bit 19~16

2	BP_DIS	0,RW	Broadcast packet filter 0 – accept broadcast packets 1 – reject broadcast packets
1	MP_DIS	0,RW	Multicast packet filter 0 – accept multicast packets 1 – reject multicast packets
0	MP_STORM	0,RW	Broadcast Storm Control 0 – only broadcast packet 1 – also multicast packet

6.2.20 Per Port Status Data Register (CR19)

Bit	Name	Default	Description
31	LOOPBACK	0,RW	Loop-back mode
30	MONI_TX	0,RW	TX Packet Monitored The transmitted packets are also forward to sniffer port.
29	MONI_RX	0,RW	RX Packet Monitored The received packets are also forward to sniffer port
28	DIS_BMP	0,RW	Broad/Multicast Not Monitored The received broadcast or multicast packets are not forward to sniffer port.
27	Reserved	0,RO	reserved
26	TX_DIS	0,RW	Packet Transmit Disabled All packets can not be forward to this port.
25	RX_DIS	0,RW	Packet receive Disabled All received packets are discarded.
24	ADR_DIS	0,RW	Address Learning Disabled The Source Address (SA) field of packet is not learned to address table.
23~6	Reserved	0,RO	reserved
5	LP_FCS	0,RO	Link Partner Flow Control Enable Status
4	BIST	0,RO	BIST status 1: SRAM BIST fail 0: SRAM BIST pass
3	Reserved	0,RO	reserved
2	SPEED2	RO	PHY Speed Status 0: 10Mbps, 1:100Mbps
1	FDX2	RO	PHY Duplex Status 0: half-duplex, 1:full-duplex
0	LINK2	RO	PHY Link Status 0: link fail, 1: link OK

6.2.21 Per Port VLAN Tag Byte Register (CR20)

Bit	Name	Default	Description
31:28	BLK_UKP	0,RW	Ports of Unknown Packet Be Blocked The packets with DA field not found in address table are not forward to the assigned ports. These bits can be written if CR17.5=1
27:24	BLK_BP	0,RW	Ports of Broadcast Packet Be Blocked The received broadcast packets are not forward to the assigned ports. These bits can be written if CR17.5=1
23:20	BLK_MP	0,RW	Ports of Multicast Packet Be Blocked The received multicast packets are not forward to the assigned ports. These bits can be written if CR17.5=1
19:16	BLK_UP	0,RW	Ports of Unicast Packet Be Blocked The received unicast packets are not forward to the assigned ports. Note that the assigned port definition: bit 0 for port 0, bit 1 for port 1, bit 2 for port 2, and bit 3 for processor port. These bits can be written if CR17.5=1
15:13	PRI	0,RW	Port VLAN Tag [15:13]
12	CFI	0,RW	Port VLAN Tag[12]
11:0	VID118	0,RW	Port VLAN VID[11:0]

6.2.22 Per Port MIB counter Index Register (CR21)

Bit	Name	Default	Description
31:8	reserved	0,RO	Reserved
7	READY	0,RO	MIB counter data is ready When this register is written with INDEX data, this bit is cleared and the MIB counter reading is in progress. After end of read MIB counter, the MIB data is loaded into CR22, and this bit is set to indicate that the MIB data is ready, and then the MIB data of this INDEX is cleared.
6:5	reserved	0,RO	Reserved
4:0	INDEX	0,RW	MIB counter index 00H: RX Byte Counter 01H: RX Uni-cast Packet Counter 02H: RX Multi-cast Packet Counter 03H: RX Discard Packet Counter 04H: RX Error Packet Counter 05H: TX Byte Counter 06H: TX Uni-cast Packet Counter 07H: TX Multi-cast Packet Counter 08H: TX Discard Packet Counter 09H: TX Error Packet Counter

6.2.23 MIB counter Data Register (CR22)

Bit	Name	Default	Description
31:0	MIB_DATA	0,RO	MIB counter data

6.2.24 VLAN priority Map Register (CR23)

Define the 3-bit of priority field VALN mapping to 2-bit priority queue number

Bit	Name	Default	Description
31:12	Reserved	0,RO	Reserved
15:14	TAG7	3,RW	VLAN priority tag value = 07h
13:12	TAG6	3,RW	VLAN priority tag value = 06h
11:10	TAG5	2,RW	VLAN priority tag value = 05h
9:8	TAG4	2,RW	VLAN priority tag value = 04h
7:6	TAG3	1,RW	VLAN priority tag value = 03h
5:4	TAG2	1,RW	VLAN priority tag value = 02h
3:2	TAG1	0,RW	VLAN priority tag value = 01h
1:0	TAG0	0,RW	VLAN priority tag value = 00h

6.2.25 Port-based VLAN mapping table register 0 (CR24)

Define the port member in VLAN group

There are 16 VLAN groups that defined in (CR24) – (CR27)

Group 0 defined in CR24 Bit 3:0 , group 1 defined in CR24 Bit 11:8, … and group 15 defined in CR27 Bit 27:24.

.

Bit	Name	Default	Description
31:28	RESERVED	0,RO	Reserved
27:24	GROUP3	F,RW	Group 3 member:Port 3(uP),2~0
23:20	RESERVED	0,RO	Reserved
19:16	GROUP2	F,RW	Group 2 member:Port 3(uP) 2~0
15:12	RESERVED	0,RO	Reserved
11:8	GROUP1	F,RW	Group 1 member:Port 3(uP)2~0
7:4	RESERVED	0,RO	Reserved
3:0	GROUP0	F,RW	Group 0 member : Port 3(uP)2~0

6.2.26 Port-based VLAN mapping table register 1 (CR25)

Bit	Name	Default	Description
31:28	RESERVED	0,RO	Reserved
27:24	GROUP7	F,RW	Group 7 member:Port 3(uP)2~0
23:20	RESERVED	0,RO	Reserved
19:16	GROUP6	F,RW	Group 6 member:Port 3(uP)2~0
15:12	RESERVED	0,RO	Reserved
11:8	GROUP5	F,RW	Group 5 member:Port 3(uP)2~0
7:4	RESERVED	0,RO	Reserved
3:0	GROUP4	F,RW	Group 4 member : Port3(uP) 2~0

6.2.27 Port-based VLAN mapping table register 2 (CR26)

Bit	Name	Default	Description
31:28	RESERVED	0,RO	Reserved
27:24	GROUP11	F,RW	Group 11 member:Port 3(uP) 2~0
23:20	RESERVED	0,RO	Reserved
19:16	GROUP10	F,RW	Group 10 member:Port 3(uP) 2~0
15:12	RESERVED	0,RO	Reserved
11:8	GROUP9	F,RW	Group 9 member:Port 3(uP) 2~0
7:4	RESERVED	0,RO	Reserved
3:0	GROUP8	F,RW	Group 8 member : Port 3(uP) 2~0

6.2.28 Port-based VLAN mapping table register 3 (CR27)

Bit	Name	Default	Description
31:28	RESERVED	0,RO	Reserved
27:24	GROUP15	F,RW	Group 15 member:Port 3(uP) 2~0
23:20	RESERVED	0,RO	Reserved
19:16	GROUP14	F,RW	Group 14 member:Port 3(uP) 2~0
15:12	RESERVED	0,RO	Reserved
11:8	GROUP13	F,RW	Group 13 member:Port 3(uP) 2~0
7:4	RESERVED	0,RO	Reserved
3:0	GROUP12	F,RW	Group 12 member : Port 3(uP) 2~0

6.2.29 TOS Priority Map Register 0 (CR28)

Define the 6-bit or 3-bit of ToS field mapping to 2-bit priority queue number.
In 6-bit type, the CR16 bit 15 is "1", CR28 bit [1:0] define the mapping for ToS value 0, CR28 bit [3:2] define the mapping for ToS value 1, … and so on, till CR31 bit [31:30] define ToS value 63.
In 3-bit type, CR28 bit [1:0] define the mapping for ToS value 0, CR28 bit [3:2] define the mapping for ToS value 1, … and so on, till CR28 bit [15:14] define ToS value 7.

Bit	Name	Default	Description
31:30	TOSF	0,RW	If bit 15 of CR16 =1 :TOS[7:2]=0Fh
29:28	TOSE	0,RW	If bit 15 of CR16 =1 :TOS[7:2]=0Eh
27:26	TOSD	0,RW	If bit 15 of CR16 =1 :TOS[7:2]=0Dh
25:24	TOSC	0,RW	If bit 15 of CR16 =1 :TOS[7:2]=0Ch
23:22	TOSB	0,RW	If bit 15 of CR16 =1 :TOS[7:2]=0Bh
21:20	TOSA	0,RW	If bit 15 of CR16 =1 :TOS[7:2]=0Ah
19:18	TOS9	0,RW	If bit 15 of CR16 =1 :TOS[7:2]=09h
17:16	TOS8	0,RW	If bit 15 of CR16 =1 :TOS[7:2]=08h
15:14	TOS7	0/3,RW	If bit 15 of CR16 =1 :TOS[7:2]=07h, otherwise TOS]7:5]=07h
13:12	TOS6	0/3,RW	If bit 15 of CR16 =1 :TOS[7:2]=06h, otherwise TOS]7:5]=06h
11:10	TOS5	0/2,RW	If bit 15 of CR16 =1 :TOS[7:2]=05h, otherwise TOS]7:5]=05h
9:8	TOS4	0/2,RW	If bit 15 of CR16 =1 :TOS[7:2]=04h, otherwise TOS]7:5]=04h
7:6	TOS3	0/1,RW	If bit 15 of CR16 =1 :TOS[7:2]=03h, otherwise TOS]7:5]=03h
5:4	TOS2	0,/1RW	If bit 15 of CR16 =1 :TOS[7:2]=02h, otherwise TOS]7:5]=02h
3:2	TOS1	0,RW	If bit 15 of CR16 =1 :TOS[7:2]=01h, otherwise TOS]7:5]=01h
1:0	TOS0	0,RW	If bit 15 of CR16 =1 :TOS[7:2]=00h, otherwise TOS]7:5]=00h

6.2.30 TOS Priority Map Register 1 (CR29)

Bit	Name	Default	Description
31:30	TOS1F	1,RW	If bit 15 of CR16 =1 :TOS[7:2]=1Fh
29:28	TOS1E	1,RW	If bit 15 of CR16 =1 :TOS[7:2]=1Eh
27:26	TOS1D	1,RW	If bit 15 of CR16 =1 :TOS[7:2]=1Dh
25:24	TOS1C	1,RW	If bit 15 of CR16 =1 :TOS[7:2]=1Ch
23:22	TOS1B	1,RW	If bit 15 of CR16 =1 :TOS[7:2]=1Bh
21:20	TOS1A	1,RW	If bit 15 of CR16 =1 :TOS[7:2]=1Ah
19:18	TOS19	1,RW	If bit 15 of CR16 =1 :TOS[7:2]=19h
17:16	TOS18	1,RW	If bit 15 of CR16 =1 :TOS[7:2]=18h
15:14	TOS17	1,RW	If bit 15 of CR16 =1 :TOS[7:2]=17h
13:12	TOS16	1,RW	If bit 15 of CR16 =1 :TOS[7:2]=16h
11:10	TOS15	1,RW	If bit 15 of CR16 =1 :TOS[7:2]=15h
9:8	TOS14	1,RW	If bit 15 of CR16 =1 :TOS[7:2]=14h
7:6	TOS13	1,RW	If bit 15 of CR16 =1 :TOS[7:2]=13h
5:4	TOS12	1,RW	If bit 15 of CR16 =1 :TOS[7:2]=12h
3:2	TOS11	1,RW	If bit 15 of CR16 =1 :TOS[7:2]=11h
1:0	TOS10	1,RW	If bit 15 of CR16 =1 :TOS[7:2]=10h

6.2.31 TOS Priority Map Register 2 (CR30)

Bit	Name	Default	Description
31:30	TOS2F	2,RW	If bit 15 of CR16 =1 :TOS[7:2]=2Fh
29:28	TOS2E	2,RW	If bit 15 of CR16 =1 :TOS[7:2]=2Eh
27:26	TOS2D	2,RW	If bit 15 of CR16 =1 :TOS[7:2]=2Dh
25:24	TOS2C	2,RW	If bit 15 of CR16 =1 :TOS[7:2]=2Ch
23:22	TOS2B	2,RW	If bit 15 of CR16 =1 :TOS[7:2]=2Bh
21:20	TOS2A	2,RW	If bit 15 of CR16 =1 :TOS[7:2]=2Ah
19:18	TOS29	2,RW	If bit 15 of CR16 =1 :TOS[7:2]=29h
17:16	TOS28	2,RW	If bit 15 of CR16 =1 :TOS[7:2]=28h
15:14	TOS27	2,RW	If bit 15 of CR16 =1 :TOS[7:2]=27h
13:12	TOS26	2,RW	If bit 15 of CR16 =1 :TOS[7:2]=26h
11:10	TOS25	2,RW	If bit 15 of CR16 =1 :TOS[7:2]=25h
9:8	TOS24	2,RW	If bit 15 of CR16 =1 :TOS[7:2]=24h
7:6	TOS23	2,RW	If bit 15 of CR16 =1 :TOS[7:2]=23h
5:4	TOS22	2,RW	If bit 15 of CR16 =1 :TOS[7:2]=22h
3:2	TOS21	2,RW	If bit 15 of CR16 =1 :TOS[7:2]=21h
1:0	TOS20	2,RW	If bit 15 of CR16 =1 :TOS[7:2]=20h

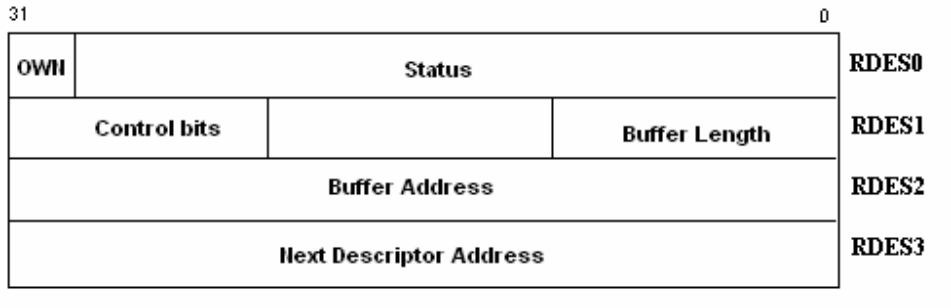
6.2.32 TOS Priority Map Register 3 (CR31)

Bit	Name	Default	Description
31:30	TOS3F	3,RW	If bit 15 of CR16 =1 :TOS[7:2]=3Fh
29:28	TOS3E	3,RW	If bit 15 of CR16 =1 :TOS[7:2]=3Eh
27:26	TOS3D	3,RW	If bit 15 of CR16 =1 :TOS[7:2]=3Dh
25:24	TOS3C	3,RW	If bit 15 of CR16 =1 :TOS[7:2]=3Ch
23:22	TOS3B	3,RW	If bit 15 of CR16 =1 :TOS[7:2]=3Bh
21:20	TOS3A	3,RW	If bit 15 of CR16 =1 :TOS[7:2]=3Ah
19:18	TOS39	3,RW	If bit 15 of CR16 =1 :TOS[7:2]=39h
17:16	TOS38	3,RW	If bit 15 of CR16 =1 :TOS[7:2]=38h
15:14	TOS37	3,RW	If bit 15 of CR16 =1 :TOS[7:2]=37h
13:12	TOS36	3,RW	If bit 15 of CR16 =1 :TOS[7:2]=36h
11:10	TOS35	3,RW	If bit 15 of CR16 =1 :TOS[7:2]=35h
9:8	TOS34	3,RW	If bit 15 of CR16 =1 :TOS[7:2]=34h
7:6	TOS33	3,RW	If bit 15 of CR16 =1 :TOS[7:2]=33h
5:4	TOS32	3,RW	If bit 15 of CR16 =1 :TOS[7:2]=32h
3:2	TOS31	3,RW	If bit 15 of CR16 =1 :TOS[7:2]=31h
1:0	TOS30	3,RW	If bit 15 of CR16 =1 :TOS[7:2]=30h

6.3 Descriptor List

Refer to Section 9.1 “PCI Bus Buffer Management” for the description of the descriptor list.

6.3.1 Receive Descriptor Format



6.3.1.1 Receive Status Register (RDES0)

Bit	Name	Default	Description
31	OWN	0,RO	Owner bit of received status
30	RAU	0,RO	Received address unmatched
29:16	FL	0,RO	Frame Length
15	ES	0,RO	Error Summary
14	DUE	0,RO	Descriptor Unavailable Error
13:12	RESERVED	0,RO	Reserved
11	RF	0,RO	Runt Frame
10	MF	0,RO	Multicast Frame
9	BD	0,RO	Begin Descriptor
8	ED	0,RO	End Descriptor
7:6	RESERVED	0,RO	Reserved
5	FT	0,RO	Frame Type or IP packet
4	TCP	0,RO	TCP packet
3	PLE	0,RO	Physical Layer Error or UDP packet
2	AE	0,RO	Alignment Error
1	CRCE	0,RO	CRC Error
0	FOE	0,RO	FIFO Overflow Error

6.3.1.2 Receive Descriptor Control and Buffer Size Register (RDES1)

Bit	Name	Default	Description
31:25	RESERVED	0,RW	Reserved
24	CHAIN	0,RW	Chain Mode Must be set to 1 in application
23:12	RESERVED	0,RW	Reserved
10:0	BL	0,RW	Buffer Length

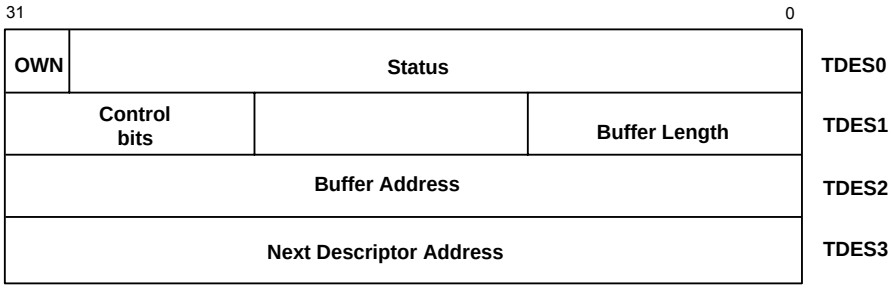
6.3.1.3 Buffer Starting Address Register (RDES2)

Bit	Name	Default	Description
31:0	N_BUF	0,RW	Buffer start address, bit 1~0 should be set 0

6.3.1.4 Next descriptor Address Register (RDES3)

Bit	Name	Default	Description
31:0	N_ADR	0,RW	Next descriptor address, bit 2~0 should be set 0

6.3.2 Transmit Descriptor Format



6.3.2.1 Transmit Status Register (TDES0)

Bit	Name	Default	Description
31	OWN	0,RO	Owner bit of transmit status
30:16	RESERVED	0,RO	Reserved
15	ES	0,RO	Error Summary
14:10	RESERVED	0,RO	Reserved
9	LC	0,RO	Late Collision
8	EC	0,RO	Excessive collision
7	RESERVED	0,RO	Reserved
6:3	CC	0,RO	Collision Count
2	RESERVED	0,RO	Reserved
1	FUE	0,RO	FIFO Underrun Error
0	DF	0,RO	Deferred

6.3.2.2 Transmit buffer control and buffer size Register (TDES1)

Bit	Name	Default	Description
31:11	CI	0,RW	Completion Interrupt
30	ED	0,RW	Ending Descriptor
29	BD	0,RW	Begin Descriptor
28	FB1	0,RW	Filtering Mode Bit 1
27	SF	0,RW	Setup Frame
26	CAD	0,RW	CRC Append Disable
25	RESERVED	0,RW	Reserved
24	CHAIN	0,RW	Chain Mode Must be set to 1 in application
23	RESERVED	0,RW	Reserved
22	FB0	0,RW	Filtering Mode Bit 0
21	IP	0,RW	IP Packet Checksum Generation
20	TCP	0,RW	TCP Packet Checksum Generation
19	UDP	0,RW	UDP Packet Checksum Generation
18:11	RESERVED	0,RW	Reserved
10:0	BL	0,RW	Buffer Length

Bit	Name	Default	Description
31:0	BUFADR	0,RW	Buffer start address bit 31:00

6.3.2.4 Next descriptor Address Register (TDES3)

Bit	Name	Default	Description
31:0	NADR	0,RO	Next descriptor address, bit 2~0 should be set 0.

7. PCI mode EEPROM Format

The first 48 words of Configuration EEPROM are loaded into the DM9103 after power-on-reset for the settings of the power management, system ID and Ethernet address. The format of the EEPROM is as followed

name	Word offset	Description
Subsystem Vendor ID	0	The content will be transferred into the PCI configuration space 2CH bit 15~0.
Subsystem ID	1	The content will be transferred into the PCI configuration space 2CH bit 31~16.
RESERVED	2~3	Reserved
Auto_Load_Control	4	Bit3~0: "1010" to enable auto-load of PCI Vendor_ID & Device_ID.
PCI Vendor ID	5	When Word[4] bit 3~0="1010", this word will be loaded to PCI Configuration space address 0 bit 15~0
PCI Device ID	6	When Word[4] bit 3~0="1010", this word will be loaded to PCI Configuration space address 0 bit 31~16
PMC	7	Bit2~0: Directly mapping to bit[21,26:25] of the PCIPMR Bit7~3: Directly mapping to bit[31:27] of the PCIPMR. Bit 15~8: Reserved
RESERVED	8~9	Reserved
Ethernet Address	10~12	Word 10 low byte for address 0 Word 10 high byte for address 1 Word 11 low byte for address 2 Word 11 high byte for address 3 Word 12 low byte for address 4 Word 12 high byte for address 5
RESERVED	13~15	Reserved
Control	16	Bit 1:0=01: Accept setting of WORD 17,18 Bit 3:2=01: Accept setting of WORD 19~26 Bit 5:4=01: Accept setting of WORD 27~30 Bit 7:6=01: Accept setting of WORD 31 Bit 9:8=01: Accept setting of WORD 32~39 Bit 11:10=01: Accept setting of WORD 40~47 Bit 15:12 =01: Reserved
Switch Control 1	17	When word 16 bit 1:0 is "01", after power on reset: This word will be loaded to CR16 bit 15~0
Switch Control 2	18	When word 16 bit 1:0 is "01", after power on reset: This word will be loaded to CR16 bit 31~16
Port 0 Control 1	19	When word 16 bit 3:2 is "01", after power on reset: This word will be loaded to port 0 CR18 bit 15~0
Port 0 Control 2	20	When word 16 bit 3:2 is "01", after power on reset: This word will be loaded to port 0 CR18 bit 31~16
Port 1 Control 1	21	When word 16 bit 3:2 is "01", after power on reset: This word will be loaded to port 1 CR18 bit 15~0
Port 1 Control 2	22	When word 16 bit 3:2 is "01", after power on reset: This word will be loaded to port 1 CR18 bit 31~16
Port 2 Control 1	23	When word 16 bit 3:2 is "01", after power on reset: This word will be loaded to port 2 CR18 bit 15~0

Port 2 Control 2	24	When word 16 bit 3:2 is “01”, after power on reset: This word will be loaded to port 2 CR18 bit 31~16
uP Port Control 1	25	When word 16 bit 3:2 is “01”, after power on reset: This word will be loaded to port 3 CR18 bit 15~0
uP Port Control 2	26	When word 16 bit 3:2 is “01”, after power on reset: This word will be loaded to port 3 CR18 bit 31~16
Port 0 VLAN Tag	27	When word 16 bit 5:4 is “01”, after power on reset: This word will be loaded to port 0 CR20 bit 15~0
Port 1 VLAN Tag	28	When word 16 bit 5:4 is “01”, after power on reset: This word will be loaded to port 1 CR20 bit 15~0
Port 2 VLAN Tag	29	When word 16 bit 5:4 is “01”, after power on reset: This word will be loaded to port 2 CR20 bit 15~0
uP Port VLAN Tag	30	When word 16 bit 5:4 is “01”, after power on reset: This word will be loaded to port 3 CR20 bit 15~0
VLAN Priority Map	31	When word 16 bit 7:6 is “01”, after power on reset: This word will be loaded to CR23 bit 15~0
Port VLAN Group 0,1	32	When word 16 bit 9:8 is “01”, after power on reset: This word will be loaded to CR24 bit 15~0
Port VLAN Group 2,3	33	When word 16 bit 9:8 is “01”, after power on reset: This word will be loaded to CR24 bit 31~16
Port VLAN Group 4,5	34	When word 16 bit 9:8 is “01”, after power on reset: This word will be loaded to CR25 bit 15~0
Port VLAN Group 6,7	35	When word 16 bit 9:8 is “01”, after power on reset: This word will be loaded to CR25 bit 31~16
Port VLAN Group 8,9	36	When word 16 bit 9:8 is “01”, after power on reset: This word will be loaded to CR26 bit 15~0
Port VLAN Group 10,11	37	When word 16 bit 9:8 is “01”, after power on reset: This word will be loaded to CR26 bit 31~16
Port VLAN Group 12,13	38	When word 16 bit 9:8 is “01”, after power on reset: This word will be loaded to CR27 bit 15~0
Port VLAN Group 14,15	39	When word 16 bit 9:8 is “01”, after power on reset: This word will be loaded to CR27 bit 31~16
ToS Priority Map 0	40	When word 16 bit 11:10 is “01”, after power on reset: This word will be loaded to CR28 bit 15~0
ToS Priority Map 1	41	When word 16 bit 11:10 is “01”, after power on reset: This word will be loaded to CR28 bit 31~16
ToS Priority Map 2	42	When word 16 bit 11:10 is “01”, after power on reset: This word will be loaded to CR29 bit 15~0
ToS Priority Map 3	43	When word 16 bit 11:10 is “01”, after power on reset: This word will be loaded to CR29 bit 31~16
ToS Priority Map 4	44	When word 16 bit 11:10 is “01”, after power on reset: This word will be loaded to CR30 bit 15~0
ToS Priority Map 5	45	When word 16 bit 11:10 is “01”, after power on reset: This word will be loaded to CR30 bit 31~16
ToS Priority Map 6	46	When word 16 bit 11:10 is “01”, after power on reset: This word will be loaded to CR31 bit 15~0
ToS Priority Map 7	47	When word 16 bit 11:10 is “01”, after power on reset: This word will be loaded to CR31 bit 31~16

8. PHY Registers

MII Register Description

ADD	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00H	CONTROL	Reset	Loop back	Speed select	Auto-N Enable	Power Down	Isolate	Restart Auto-N	Full Duplex	Coll. Test	Reserved						
		0	0	1	1	0	0	0	1	0	000_0000						
01H	STATUS	T4 Cap.	TX FDX Cap.	TX HDX Cap.	10 FDX Cap.	10 HDX Cap.	Reserved				Pream. Supr.	Auto-N Compl.	Remote Fault	Auto-N Cap.	Link Status	Jabber Detect	Extd Cap.
		0	1	1	1	1	0000				1	0	0	1	0	0	1
02H	PHYID1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
03H	PHYID2	1	0	1	1	1	0	Model No.						Version No.			
								01011						0000			
04H	Auto-Neg. Advertise	Next Page	FLP Rcv Ack	Remote Fault	Reserved		FC Adv	T4 Adv	TX FDX Adv	TX HDX Adv	10 FDX Adv	10 HDX Adv	Advertised Protocol Selector Field				
05H	Link Part. Ability	LP Next Page	LP Ack	LP RF	Reserved		LP FC	LP T4	LP TX FDX	LP TX HDX	LP 10 FDX	LP 10 HDX	Link Partner Protocol Selector Field				
06H	Auto-Neg. Expansion	Reserved											Pardet Fault	LP Next Pg Able	Next Pg Able	New Pg Rcv	LP AutoN Cap.
10H	Specified Config.	BP 4B5B	BP SCR	BP ALIGN	BP_ADPOK	Reserve dr	TX	Reserve d	Reserved	Force 100LNK	Reserved	Reserved	RPDCTR-EN	Reset St. Mch	Pream. Supr.	Sleep mode	Remote LoopOut
11H	Specified Conf/Stat	100 FDX	100 HDX	10 FDX	10 HDX	Reserve d	Reverse d	Reverse d	PHY ADDR [4:0]					Auto-N. Monitor Bit [3:0]			
12H	10T Conf/Stat	Rsvd	LP Enable	HBE Enable	SQUE Enable	JAB Enable	Reserve d	Reserved									Polarity Reverse
13H	PWDOR	Reserved							PD10DRV	PD100I	PDchip	PDcrm	PDaeq	PDdrv	PDecli	PDeclo	PD10
14H	Specified config	TSTSE1	TSTSE2	FORCE_TXSD	FORCE_FEF	Reserved				MDIX_CNTL	AutoNeg_dlpbk	Mdix_fixValue	Mdix_down	MonSel1	MonSel0	Reserve d	PD_value
16H	RCVER	Receiver Error Counter															
17H	DIS_connect	Reversed								Disconnect_counter							

Key to Default

In the register description that follows, the default column takes the form:
<Reset Value>, <Access Type> / <Attribute(s)>
Where:
<Reset Value>:

- 1 Bit set to logic one
- 0 Bit set to logic zero
- X No default value

<Access Type>:
RO = Read only, RW = Read/Write
<Attribute (s)>:
SC = Self clearing, P = Value permanently set

8.1 Basic Mode Control Register (BMCR) – 00H

Bit	Bit Name	Default	Description
15	Reset	0, RW/SC	Reset 1=Software reset 0=Normal operation This bit sets the status and controls the PHY registers to their default states. This bit, which is self-clearing, will keep returning a value of one until the reset process is completed
14	Loopback	0, RW	Loopback Loop-back control register 1 = Loop-back enabled 0 = Normal operation When in 100Mbps operation mode, setting this bit may cause the descrambler to lose synchronization and produce a 720ms "dead time" before any valid data appears at the MII receive outputs
13	Speed selection	1, RW	Speed Select 1 = 100Mbps 0 = 10Mbps Link speed may be selected either by this bit or by auto-negotiation. When auto-negotiation is enabled and bit 12 is set, this bit will return auto-negotiation selected medium type
12	Auto-negotiation enable	1, RW	Auto-negotiation Enable 1 = Auto-negotiation is enabled, bit 8 and 13 will be in auto-negotiation status
11	Power down	0, RW	Power Down While in the power-down state, the PHY should respond to management transactions. During the transition to power-down state and while in the power-down state, the PHY should not generate spurious signals on the MII 1=Power down 0=Normal operation
10	Isolate	0,RW	Isolate Force to 0 in application.
9	Restart Auto-negotiation	0,RW/SC	Restart Auto-negotiation 1 = Restart auto-negotiation. Re-initiates the auto-negotiation process. When auto-negotiation is disabled (bit 12 of this register cleared), this bit has no function and it should be cleared. This bit is self-clearing and it will keep returning to a value of 1 until auto-negotiation is initiated by the DM9103. The operation of the auto-negotiation process will not be affected by the management entity that clears this bit 0 = Normal operation
8	Duplex mode	1,RW	Duplex Mode 1 = Full duplex operation. Duplex selection is allowed when Auto-negotiation is disabled (bit 12 of this register is cleared). With auto-negotiation enabled, this bit reflects the duplex capability selected by auto-negotiation 0 = Normal operation

7	Collision test	0,RW	Collision Test 1 = Collision test enabled. When set, this bit will cause the COL signal to be asserted in response to the assertion of TX_EN in internal MII interface. 0 = Normal operation
6-0	Reserved	0,RO	Reserved Read as 0, ignore on write

8.2 Basic Mode Status Register (BMSR) – 01H

Bit	Bit Name	Default	Description
15	100BASE-T4	0,RO/P	100BASE-T4 Capable 1 = DM9103 is able to perform in 100BASE-T4 mode 0 = DM9103 is not able to perform in 100BASE-T4 mode
14	100BASE-TX full-duplex	1,RO/P	100BASE-TX Full Duplex Capable 1 = DM9103 is able to perform 100BASE-TX in full duplex mode 0 = DM9103 is not able to perform 100BASE-TX in full duplex mode
13	100BASE-TX half-duplex	1,RO/P	100BASE-TX Half Duplex Capable 1 = DM9103 is able to perform 100BASE-TX in half duplex mode 0 = DM9103 is not able to perform 100BASE-TX in half duplex mode
12	10BASE-T full-duplex	1,RO/P	10BASE-T Full Duplex Capable 1 = DM9103 is able to perform 10BASE-T in full duplex mode 0 = DM9103 is not able to perform 10BASE-TX in full duplex mode
11	10BASE-T half-duplex	1,RO/P	10BASE-T Half Duplex Capable 1 = DM9103 is able to perform 10BASE-T in half duplex mode 0 = DM9103 is not able to perform 10BASE-T in half duplex mode
10-7	Reserved	0,RO	Reserved Read as 0, ignore on write
6	MF preamble suppression	1,RO	MII Frame Preamble Suppression 1 = PHY will accept management frames with preamble suppressed 0 = PHY will not accept management frames with preamble suppressed
5	Auto-negotiation Complete	0,RO	Auto-negotiation Complete 1 = Auto-negotiation process completed 0 = Auto-negotiation process not completed
4	Remote fault	0, RO	Remote Fault 1 = Remote fault condition detected (cleared on read or by a chip reset). Fault criteria and detection method is DM9103 implementation specific. This bit will set after the RF bit in the ANLPAR (bit 13, register address 05) is set 0 = No remote fault condition detected
3	Auto-negotiation ability	1,RO/P	Auto Configuration Ability 1 = DM9103 is able to perform auto-negotiation 0 = DM9103 is not able to perform auto-negotiation
2	Link status	0,RO	Link Status 1 = Valid link is established (for either 10Mbps or 100Mbps operation) 0 = Link is not established The link status bit is implemented with a latching function, so that

			the occurrence of a link failure condition causes the link status bit to be cleared and remain cleared until it is read via the management interface
1	Jabber detect	0, RO	Jabber Detect 1 = Jabber condition detected 0 = No jabber This bit is implemented with a latching function. Jabber conditions will set this bit unless it is cleared by a read to this register through a management interface or a DM9103 reset. This bit works only in 10Mbps mode
0	Extended capability	1,RO/P	Extended Capability 1 = Extended register capable 0 = Basic register capable only

8.3 PHY ID Identifier Register #1 (PHYID1) – 02H

The PHY Identifier Registers #1 and #2 work together in a single identifier of the DM9103. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), a vendor's model number, and a model revision number. DAVICOM Semiconductor's IEEE assigned OUI is 00606E.

Bit	Bit Name	Default	Description
15-0	OUI_MSB	<0181h>	OUI Most Significant Bits This register stores bit 3 to 18 of the OUI (00606E) to bit 15 to 0 of this register respectively. The most significant two bits of the OUI are ignored (the IEEE standard refers to these as bit 1 and 2)

8.4 PHY ID Identifier Register #2 (PHYID2) – 03H

Bit	Bit Name	Default	Description
15-10	OUI_LSB	<101110>, RO/P	OUI Least Significant Bits Bit 19 to 24 of the OUI (00606E) are mapped to bit 15 to 10 of this register respectively
9-4	VNDR_MDL	<001011>, RO/P	Vendor Model Number Five bits of vendor model number mapped to bit 9 to 4 (most significant bit to bit 9)
3-0	MDL_REV	<0000>, RO/P	Model Revision Number Five bits of vendor model revision number mapped to bit 3 to 0 (most significant bit to bit 4)

8.5 Auto-negotiation Advertisement Register (ANAR) – 04H

This register contains the advertised abilities of this DM9103 device as they will be transmitted to its link partner during Auto-negotiation.

Bit	Bit Name	Default	Description
15	NP	0,RO/P	Next page Indication 0 = No next page available 1 = Next page available The DM9103 has no next page, so this bit is permanently set to 0
14	ACK	0,RO	Acknowledge 1 = Link partner ability data reception acknowledged 0 = Not acknowledged The DM9103's auto-negotiation state machine will automatically control this bit in the outgoing FLP bursts and set it at the appropriate time during the auto-negotiation process. Software should not attempt to write to this bit.
13	RF	0, RW	Remote Fault 1 = Local device senses a fault condition 0 = No fault detected
12-11	Reserved	X, RW	Reserved Write as 0, ignore on read
10	FCS	0, RW	Flow Control Support 1 = Controller chip supports flow control ability 0 = Controller chip doesn't support flow control ability
9	T4	0, RO/P	100BASE-T4 Support 1 = 100BASE-T4 is supported by the local device 0 = 100BASE-T4 is not supported The DM9103 does not support 100BASE-T4 so this bit is permanently set to 0
8	TX_FDX	1, RW	100BASE-TX Full Duplex Support 1 = 100BASE-TX full duplex is supported by the local device 0 = 100BASE-TX full duplex is not supported
7	TX_HDX	1, RW	100BASE-TX Support 1 = 100BASE-TX half duplex is supported by the local device 0 = 100BASE-TX half duplex is not supported
6	10_FDX	1, RW	10BASE-T Full Duplex Support 1 = 10BASE-T full duplex is supported by the local device 0 = 10BASE-T full duplex is not supported
5	10_HDX	1, RW	10BASE-T Support 1 = 10BASE-T half duplex is supported by the local device 0 = 10BASE-T half duplex is not supported
4-0	Selector	<00001>, RW	Protocol Selection Bits These bits contain the binary encoded protocol selector supported by this node <00001> indicates that this device supports IEEE 802.3 CSMA/CD

8.6 Auto-negotiation Link Partner Ability Register (ANLPAR) – 05H

This register contains the advertised abilities of the link partner when received during Auto-negotiation.

Bit	Bit Name	Default	Description
15	NP	0, RO	Next Page Indication 0 = Link partner, no next page available 1 = Link partner, next page available
14	ACK	0, RO	Acknowledge 1 = Link partner ability data reception acknowledged 0 = Not acknowledged The DM9103's auto-negotiation state machine will automatically control this bit from the incoming FLP bursts. Software should not attempt to write to this bit
13	RF	0, RO	Remote Fault 1 = Remote fault indicated by link partner 0 = No remote fault indicated by link partner
12-11	Reserved	0, RO	Reserved Read as 0, ignore on write
10	FCS	0, RO	Flow Control Support 1 = Controller chip supports flow control ability by link partner 0 = Controller chip doesn't support flow control ability by link partner
9	T4	0, RO	100BASE-T4 Support 1 = 100BASE-T4 is supported by the link partner 0 = 100BASE-T4 is not supported by the link partner
8	TX_FDX	0, RO	100BASE-TX Full Duplex Support 1 = 100BASE-TX full duplex is supported by the link partner 0 = 100BASE-TX full duplex is not supported by the link partner
7	TX_HDX	0, RO	100BASE-TX Support 1 = 100BASE-TX half duplex is supported by the link partner 0 = 100BASE-TX half duplex is not supported by the link partner
6	10_FDX	0, RO	10BASE-T Full Duplex Support 1 = 10BASE-T full duplex is supported by the link partner 0 = 10BASE-T full duplex is not supported by the link partner
5	10_HDX	0, RO	10BASE-T Support 1 = 10BASE-T half duplex is supported by the link partner 0 = 10BASE-T half duplex is not supported by the link partner
4-0	Selector	<00000>, RO	Protocol Selection Bits Link partner's binary encoded protocol selector

8.7 Auto-negotiation Expansion Register (ANER)- 06H

Bit	Bit Name	Default	Description
15-5	Reserved	0, RO	Reserved Read as 0, ignore on write
4	PDF	0, RO/LH	Local Device Parallel Detection Fault PDF = 1: A fault detected via parallel detection function. PDF = 0: No fault detected via parallel detection function
3	LP_NP_ABLE	0, RO	Link Partner Next Page Able LP_NP_ABLE = 1: Link partner, next page available LP_NP_ABLE = 0: Link partner, no next page
2	NP_ABLE	0,RO/P	Local Device Next Page Able NP_ABLE = 1: DM9103, next page available NP_ABLE = 0: DM9103, no next page DM9103 does not support this function, so this bit is always 0
1	PAGE_RX	0, RO	New Page Received A new link code word page received. This bit will be automatically cleared when the register (register 6) is read by management
0	LP_AN_ABLE	0, RO	Link Partner Auto-negotiation Able A “1” in this bit indicates that the link partner supports Auto-negotiation

8.8 DAVICOM Specified Configuration Register (DSCR) – 10H

Bit	Bit Name	Default	Description
15	BP_4B5B	0,RW	Bypass 4B5B Encoding and 5B4B Decoding 1 = 4B5B encoder and 5B4B decoder function bypassed 0 = Normal 4B5B and 5B4B operation
14	BP_SCR	0, RW	Bypass Scrambler/Descrambler Function 1 = Scrambler and descrambler function bypassed 0 = Normal scrambler and descrambler operation
13	BP_ALIGN	0, RW	Bypass Symbol Alignment Function 1 = Receive functions (descrambler, symbol alignment and symbol decoding functions) bypassed. Transmit functions (symbol encoder and scrambler) bypassed 0 = Normal operation
12	BP_ADPOK	0, RW	BYPASS ADPOK Force signal detector (SD) active. This register is for debug only, not release to customer 1=Forced SD is OK, 0=Normal operation
11	Reserved	RW	Reserved Force to 0 in application
10	TX	1, RW	100BASE-TX Mode Control 1 = 100BASE-TX operation 0 = 100BASE-FX operation
9	Reserved	0, RO	Reserved

8	RMII_MODE	0, RW	RMII mode enable
7	F_LINK_100	0, RW	Force Good Link in 100Mbps 0 = Normal 100Mbps operation 1 = Force 100Mbps good link status This bit is useful for diagnostic purposes
6	Reserved	0, RW	Reserved Force to 0 in application.
5	COL_LED	0, RW	COL LED Control (valid in PHY test mode)
4	RPDCTR-EN	1, RW	Reduced Power Down Control Enable This bit is used to enable automatic reduced power down 0 = Disable automatic reduced power down 1 = Enable automatic reduced power down
3	SMRST	0, RW	Reset State Machine When writes 1 to this bit, all state machines of PHY will be reset. This bit is self-clear after reset is completed
2	MFPSC	1, RW	MF Preamble Suppression Control MII frame preamble suppression control bit 1 = MF preamble suppression bit on 0 = MF preamble suppression bit off
1	SLEEP	0, RW	Sleep Mode Writing a 1 to this bit will cause PHY entering the Sleep mode and power down all circuit except oscillator and clock generator circuit. When waking up from Sleep mode (write this bit to 0), the configuration will go back to the state before sleep; but the state machine will be reset
0	RLOUT	0, RW	Remote Loopout Control When this bit is set to 1, the received data will loop out to the transmit channel. This is useful for bit error rate testing

8.9 DAVICOM Specified Configuration and Status Register (DSCSR) – 11H

<table>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Description</th></tr>
<tr><td>15</td><td>100FDX</td><td>1, RO</td><td>100M Full Duplex Operation Mode
After auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 100M full duplex mode. The software can read bit [15:12] to see which mode is selected after auto-negotiation. This bit is invalid when it is not in the auto-negotiation mode</td></tr>
<tr><td>14</td><td>100HDX</td><td>1, RO</td><td>100M Half Duplex Operation Mode
After auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 100M half duplex mode. The software can read bit [15:12] to see which mode is selected after auto-negotiation. This bit is invalid when it is not in the auto-negotiation mode</td></tr>
<tr><td>13</td><td>10FDX</td><td>1, RO</td><td>10M Full Duplex Operation Mode
After auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 10M Full Duplex mode. The software can read bit [15:12] to see which mode is selected after auto-negotiation. This bit is invalid when it is not in the auto-negotiation mode</td></tr>
<tr><td>12</td><td>10HDX</td><td>1, RO</td><td>10M Half Duplex Operation Mode
After auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 10M half duplex mode. The software can read bit [15:12] to see which mode is selected after auto-negotiation. This bit is invalid when it is not in the auto-negotiation mode</td></tr>
<tr><td>11</td><td>Reserved</td><td>0, RO</td><td>Reserved
Read as 0, ignore on write</td></tr>
<tr><td>10</td><td>Reserved</td><td>0,RW</td><td>Reserved</td></tr>
<tr><td>9</td><td>Reserved</td><td>0,RW</td><td>Reserved</td></tr>
<tr><td>8-4</td><td>PHYADR[4:0]</td><td>1, RW</td><td>PHY Address Bit 4:0
The first PHY address bit transmitted or received is the MSB of the address (bit 4). A station management entity connected to multiple PHY entities must know the appropriate address of each PHY</td></tr>
<tr><td>3-0</td><td>ANMB[3:0]</td><td>0, RO</td><td>Auto-negotiation Monitor Bits
These bits are for debug only. The auto-negotiation status will be written to these bits.
<table>
<tr><th>B3</th><th>b2</th><th>b1</th><th>B0</th><th></th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>In IDLE state</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Ability match</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>Acknowledge match</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>Acknowledge match fail</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>Consistency match</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>Consistency match fail</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>Parallel detects signal_link_ready</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Parallel detects signal_link_ready fail</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Auto-negotiation completed successfully</td></tr>
</table></td></tr>
</table>

8.10 10BASE-T Configuration/Status (10BTCSR) – 12H

Bit	Bit Name	Default	Description
15	Reserved	0, RO	Reserved Read as 0, ignore on write
14	LP_EN	1, RW	Link Pulse Enable 1 = Transmission of link pulses enabled 0 = Link pulses disabled, good link condition forced This bit is valid only in 10Mbps operation
13	HBE	1,RW	Heartbeat Enable 1 = Heartbeat function enabled 0 = Heartbeat function disabled When the DM9103 is configured for full duplex operation, this bit will be ignored (the collision/heartbeat function is invalid in full duplex mode)
12	SQUELCH	1, RW	Squelch Enable 1 = Normal squelch 0 = Low squelch
11	JABEN	1, RW	Jabber Enable Enables or disables the Jabber function when the DM9103 is in 10BASE-T full duplex or 10BASE-T transceiver Loopback mode 1 = Jabber function enabled 0 = Jabber function disabled
10	SERIAL	0, RW	10M Serial Mode (valid in PHY test mode) Force to 0, in application.
9-1	Reserved	0, RO	Reserved Read as 0, ignore on write
0	POLR	0, RO	Polarity Reversed When this bit is set to 1, it indicates that the 10Mbps cable polarity is reversed. This bit is automatically set and cleared by 10BASE-T module

8.11 Power Down Control Register (PWDOR) – 13H

Bit	Bit Name	Default	Description
15-9	Reserved	0, RO	Reserved Read as 0, ignore on write
8	PD10DRV	0, RW	Vendor power down control test
7	PD100DL	0, RW	Vendor power down control test
6	PDchip	0, RW	Vendor power down control test
5	PDcrm	0, RW	Vendor power down control test
4	PDaeq	0, RW	Vendor power down control test
3	PDdrv	0, RW	Vendor power down control test
2	PDedi	0, RW	Vendor power down control test
1	PDedo	0, RW	Vendor power down control test
0	PD10	0, RW	Vendor power down control test

***** when selected, the power down value is control by Register 20.0

8.12 (Specified config) Register – 14H

Bit	Bit Name	Default	Description
15	TSTSE1	0,RW	Vendor test select control
14	TSTSE2	0,RW	Vendor test select control
13	FORCE_TXSD	0,RW	Force Signal Detect 1: force SD signal OK in 100M 0: normal SD signal.
12	FORCE_FEF	0,RW	Vendor test select control
11-8	Reserved	0, RO	Reserved Read as 0, ignore on write
7	MDIX_CNTL	MDI/MDIX,RO	The polarity of MDI/MDIX value 1: MDIX mode 0: MDI mode
6	AutoNeg_dpbk	0,RW	Auto-negotiation Loopback 1: test internal digital auto-negotiation Loopback 0: normal.
5	Mdix_fix Value	0, RW	MDIX_CNTL force value: When Mdix_down = 1, MDIX_CNTL value depend on the register value.
4	Mdix_down	0,RW	MDIX Down Manual force MDI/MDIX. 0: Enable HP Auto-MDIX 1: Disable HP Auto-MDIX , MDIX_CNTL value depend on 20.5
3	MonSel1	0,RW	Vendor monitor select
2	MonSel0	0,RW	Vendor monitor select
1	Reserved	0,RW	Reserved Force to 0, in application.
0	PD_value	0,RW	Power down control value Decision the value of each field Register 19. 1: power down 0: normal

8.13 DAVICOM Specified Receive Error Counter Register (RECR) – 16H

Bit	Bit Name	Default	Description
15-0	Rcv_ Err_ Cnt	0, RO	Receive Error Counter Receive error counter that increments upon detection of RXER. Clean by read this register.

8.14 DAVICOM Specified Disconnect Counter Register (DISCR) – 17H

Bit	Bit Name	Default	Description
15-8	Reserved	0, RO	Reserved
7-0	Disconnect Counter	0, RO	Disconnect Counter that increment upon detection of disconnection. Clean by read this register.

9. Functional Description

9.1 PCI Bus Buffer Management

9.1.1. Overview

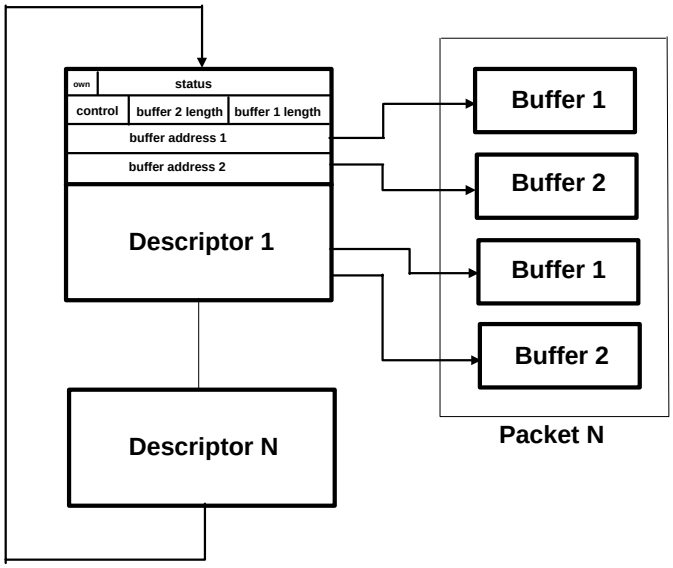
The data buffers for reception and transmission of data reside in the host memory. They are directed by the descriptor lists that are located in another region of the host memory. All actions for the buffer management are operated by the DM9103 in conjunction with the driver. The data structures and processing algorithms are described in the following text.

9.1.2. Data Structure and Descriptor List

There are two types of buffers that reside in the host memory, the transmit buffer and the receive buffer. The buffers are composed of many distributed regions in the host memory. They are linked together and controlled by the descriptor lists that reside in another region of the host memory. The content of each descriptor includes pointer to the buffer, count of the buffer, command and status for the packet to be transmitted or received. Each descriptor list starts from the address setting of CR3 (receive descriptor base address) and CR4 (transmit descriptor base address). The descriptor lists have two types of structure, Ring structure and Chain structure.

9.1.3. Buffer Management : Ring Structure Method

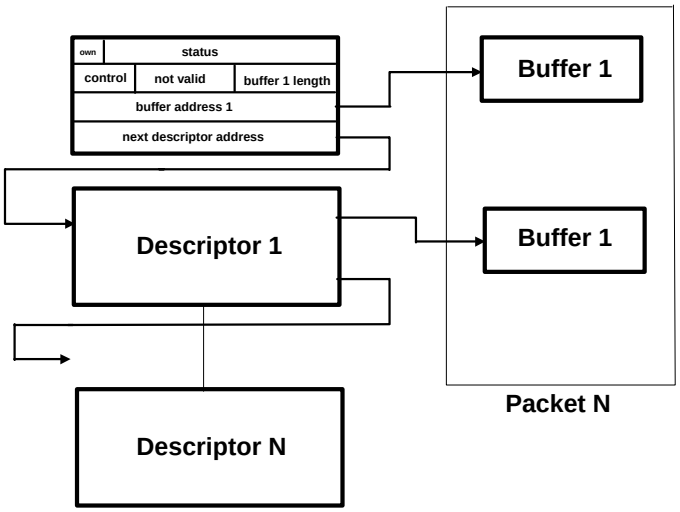
As the Ring structure depicted below, the descriptors are linked directly one after another. The first and last descriptor on the list have the necessary information for the DM9103 to return to the beginning of the list after the bottom descriptor is accessed. Each descriptor points to the two buffer regions and one packet may cross many descriptors boundaries.



9.1.4. Buffer Management : Chain Structure Method

As the Chain structure depicted below, each descriptor contains two pointers, one point to a single buffer and the other to the next descriptor chained. The first descriptor is chained by the last descriptor under host driver's control. With this structure, a descriptor can be allocated anywhere in

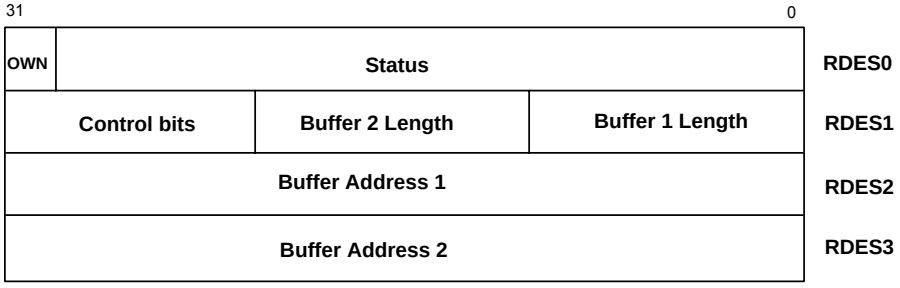
host memory and is chained to the next descriptor. The Chain structure and the Ring structure may combine to make the buffer structure more flexible.



9.1.5. Descriptor List: Buffer Descriptor Format

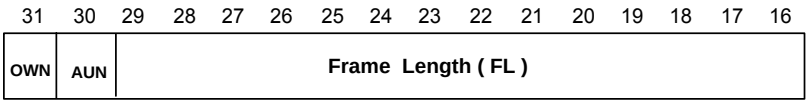
(a). Receive Descriptor Format

Each receive descriptor has four doubleword entries and may be read or written by the host or the DM9103. The descriptor format is shown below with a detailed functional description.



Receive Descriptor Format

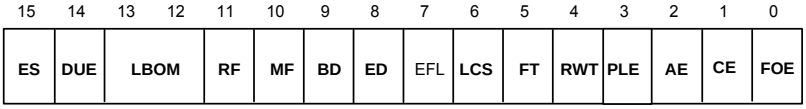
RDES0: Owner bit with receive status



OWN: 1=owned by DM9103, 0=owned by host
This bit should be reset after packet reception is completed. It will be set by the host after received data are removed.

FL: Frame length indicating total byte count of received packet.

AUN: Received address unmatched.



This word-wide content includes status of received frame. They are loaded after the received buffer that belongs to the corresponding descriptor is full. All status bits are valid only when the last descriptor (End Descriptor) bit is set.

Bit 15: ES, Error Summary

It is set for the following error conditions : Descriptor Unavailable Error (DUE =1), Runt Frame (RF=1), Excessive Frame Length (EFL=1), Late Collision Seen (LCS=1), CRC error (CE=1), FIFO Overflow error (FOE=1). Valid only when ED is set.

Bit 14: DUE, Descriptor Unavailable Error
It is set when the frame is truncated due to the buffer
unavailable. It is valid only when ED is set.

Bit 13,12: LBOM, Loopback Operation Mode
These two bits show the received frame is derived from
00 --- normal operation

01 --- internal loopback

10 --- external loopback
11 --- reserved

Bit 11: RF, Runt Frame
It is set to indicate the received frame has the size
smaller than 64 bytes. Valid only when ED is set
and FOE is reset.

Bit 10: MF, Multicast Frame
It is set to indicate the received frame has a
multicast address. Valid only when ED is set.

Bit 9: BD, Begin Descriptor
This bit is set for the descriptor indicating start of a
received frame.

Bit 8: ED, Ending Descriptor
This bit is set for the descriptor indicating end of a
received frame.

Bit 7: EFL, Excessive Frame Length
It is set to indicate the received frame length exceeds
1518 bytes. Valid only when ED is set.

Bit 6: LCS: Late Collision Seen
It is set to indicate a late collision found during the frame reception. Valid only when ED is set.

Bit 5: FT, Frame Type

It is set to indicate the received frame is the Ethernet-type. It is reset to indicate the received frame is the EEE802.3- type. Valid only when ED is set

Bit 4: RWT, Receive Watchdog Time-Out
It is set to indicate the receive Watchdog time-out
during the frame reception. CR5<9> will also be set.
Valid only when ED is set.

Bit 3: PLE, Physical Layer Error

It is set to indicate a physical layer error found during the frame reception.

Bit 2: AE, Alignment Error

It is set to indicate the received frame ends with a non-byte boundary.

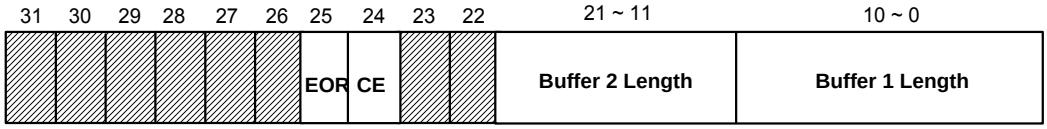
Bit 1: CE, CRC Error

It is set to indicate the received frame ends with a CRC error. Valid only when ED is set.

Bit 0: FOE, FIFO Overflow Error

This bit is valid for Ending Descriptor is set. (ED = 1)
It is set to indicate a FIFO Overflow error happens during the frame reception.

RDES1: Descriptor Status And Buffer Size



Bit 25: EOR, End of Ring

Set to indicate that the descriptor is located on the bottom of the descriptor list.

Bit 24: CE, Chain Enable

Set to indicate that the second address is the chained descriptor instead of the other buffer.
Used as the indication of the Chain structure.

Bit 21-11: Buffer 2 Length

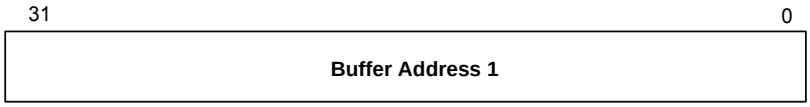
Indicates the size of the second buffer. It has no meaning in chain type descriptor.

Bit 10-0: Buffer 1 Length

Indicates the size of the first buffer in Ring type structure and single buffer in Chain type structure.

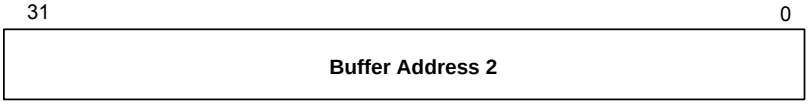
RDES2: Buffer 1 Starting Address

Indicates the physical starting address of buffer 1.



RDES3: Buffer 2 Starting Address

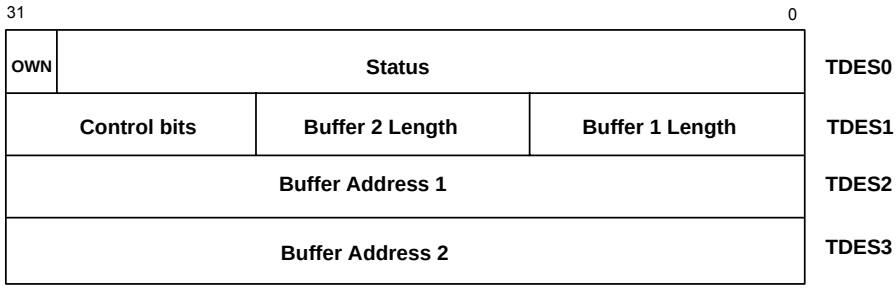
Indicates the physical starting address of buffer 2 under the Ring structure and that of the chained descriptor under the Chain descriptor structure.



(b). Transmit Descriptor Format

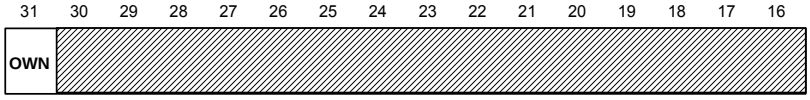
Each transmit descriptor has four doubleword content and may be read or written by the host or

by the DM9103. The descriptor format are shown below with detailed description.

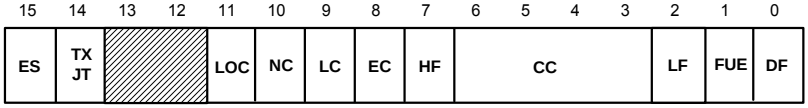


Transmit Descriptor Format

TDES0 : Owner Bit With Transmit Status



Bit 31: OWN,
1=owned by DM9103, 0=owned by host, this bit should be set when the transmitting buffer is filled with data and ready to be transmitted. It will be reset by DM9103 after transmitting the whole data buffer.



This word wide content includes status of transmitted frame. They are loaded after the data buffer that belongs to the corresponding descriptor is transmitted.

Bit 15: ES, Error Summary

It is set for the following error conditions : Transmit Jabber Time-out (TXJT=1), Loss of Carrier (LOC=1), No Carrier (NC=1), Late Collision (LC=1), Excessive Collision (EC=1), FIFO Underrun Error (FUE=1).

Bit 14: TXJT, Transmit Jabber Time Out

It is set to indicate the transmitted frame is truncated due to the transmit jabber time out condition. The transmit jabber time out interrupt
CR5<3> is set.

Bit 11: LOC, Loss Of Carrier

It is set to indicate the loss of carrier during the frame transmission. Not valid in internal loopback mode.

Bit 10: NC, No Carrier

It is set to indicate that no carrier signal from transceiver is found. Not valid in internal loopback mode.

Bit 9: LC, Late Collision

It is set to indicate a collision occurs after the collision window of 64 bytes. Not valid if FUE is set.

Bit 8: EC, Excessive collision

It is set to indicate the transmission is aborted due to 16 excessive collisions.
Bit 7: HF, Heartbeat Fail
It is set to indicate the Heartbeat check failed after complete transmission. Not valid if FUE is set. When TDES0<14> is set, this bit is not valid.

Bits 6-3: CC, Collision Count

These bits shows the number of collision before transmission. Not valid if excessive collision bit is also set.

Bit 2: LF, Link test Fail

It is set to indicate the link test fails before the frame transmission.

Bit 1: FUE, FIFO Underrun Error

It is set to indicate the transmission aborted due to a transmit FIFO underrun condition.

Bit 0: DF, Deferred

It is set to indicate the frame is deferred before ready to transmit.

TDES1 : Transmit buffer control and buffer size

31	30	29	28	27	26	25	24	23	22	21 ~ 11	10 ~ 0
CI	ED	BD	FMB1	SETF	CAD	EOR	CE	PD	FMB0	Buffer 2 Length	Buffer 1 Length

Bit 31: CI, Completion Interrupt

It is set to enable the transmit interrupt after the present frame has been transmitted. It is valid only when TDES1<30> is set or when it is a setup frame.

Bit 30: ED, Ending Descriptor

It is set to indicate the pointed buffer contains the last segment of a frame.

Bit 29: BD, Begin Descriptor

It is set to indicate the pointed buffer contains the first segment of a frame.

Bit 28: FMB1, Filtering Mode Bit 1

This bit is used with FMB0 to indicate the filtering type when the present frame is a setup frame.

Bit 27: SETF, Setup Frame

It is set to indicate the current frame is a setup frame.

Bit 26: CAD, CRC Append Disable

It is set to disable the CRC appending at the end of the transmitted frame. Valid only when TDES1<29> is set.

Bit 25: EOR, End of Ring Descriptor

It is set to indicate the descriptor is located on the bottom of the descriptor list.

Bit 24: CE, Chain Enable

This bit is set to indicate the second address (TDES3) is the chained descriptor instead of the other buffer. It is used as the indication of the Chain structure. When reset, it indicates the Ring structure.

Bit 23: PD, Padding Disable

This bit is set to disable the padding field for a packet shorter than 64 bytes.

Bit 22: FMB0, Filtering Mode Bit 0

This bit is used with FMB1 to indicate the filtering type when the present frame is a setup frame.

FMB1	FMB0	Filtering Type
0	0	Perfect Filtering
0	1	Hash Filtering
1	0	Inverse Filtering
1	1	Hash-Only Filtering

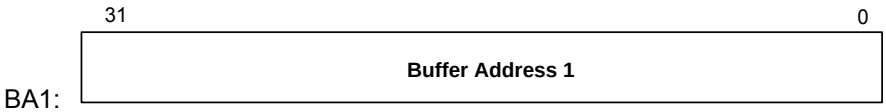
Bits 21-11: Buffer 2 length

Indicates the size of second buffer. It has no meaning with chain structure descriptor type.

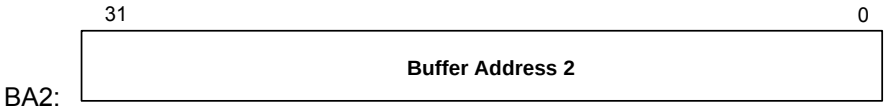
Bit 10-0: Buffer 1 length

Indicates the size of the first buffer in Ring type structure and single buffer in Chain type structure.

TDES2 : Buffer 1 Starting Address indicates the physical starting address of buffer 1.



TDES3 : Buffer 2 Starting Address indicates the physical starting address of buffer 2 under the Ring structure.



Initialization Procedure

After hardware or software reset, the transmit and receive processes are placed in the STOP state. The DM9103 can accept the host commands to start operation. The general procedure for initialization is described below:

(1) Read/write suitable values for the PCI configuration registers.
(2) Write CR3 and CR4 to provide the starting address of each descriptor list.
(3) Write CR0 to set global host bus operation parameters.
(4) Write CR7 to mask unnecessary interrupt causes.
(5) Write CR6 to set global parameters and start both the receive and transmit processes. The receive and transmit processes will enter the running state and attempt to acquire descriptors from the respective descriptor lists.
(6) Wait for any interrupt.

Data Buffer Processing Algorithm

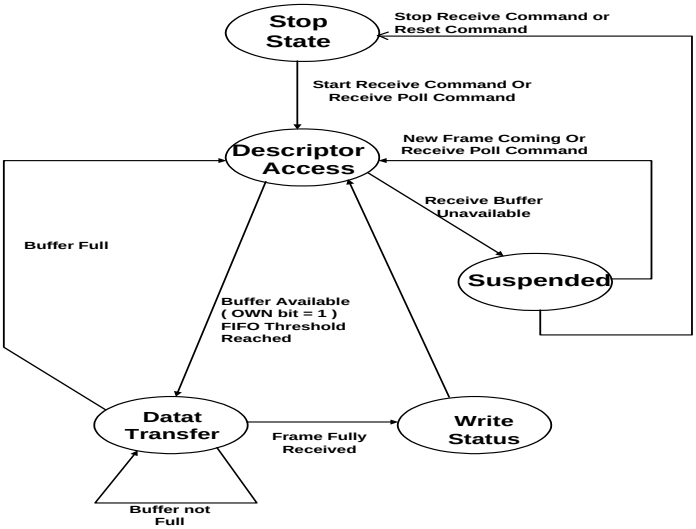
The data buffer processing algorithm is based on the cooperation of the host and the DM9103. The host sets CR3 (receive descriptor base address) and CR4 (transmit descriptor base address) for the descriptor list initialization. The DM9103 will start the data buffer transfer after the descriptor polling and get the ownership. For detailed processing procedure, please see below.

1. Receive Data Buffer Processing

The DM9103 always attempts to acquire an extra descriptor in anticipation of the incoming frames. Any incoming frame size covers a few buffer regions and descriptors. The following conditions satisfy the descriptor acquisition attempt :

- When start/stop receive sets immediately after being placed in the running state.
- When the DM9103 begins writing frame data to a data buffer pointed to by the current descriptor and the buffer ends before the frame ends.
- When the DM9103 completes the reception of a frame and the current receive descriptor is closed.
- When the receive process is suspended due to no free buffer for the DM9103 and a new frame is received.
- When the receive poll demand is issued.

After acquiring the free descriptor, the DM9103 processes the incoming frame and places it in the acquired descriptor's data buffer. When the whole received frame data has been transferred, the DM9103 will write the status information to the last descriptor. The same process will repeat until it encounters a descriptor flagged as being owned by the host. If this occurs, the receive process enters the suspended state and waits the host to service.

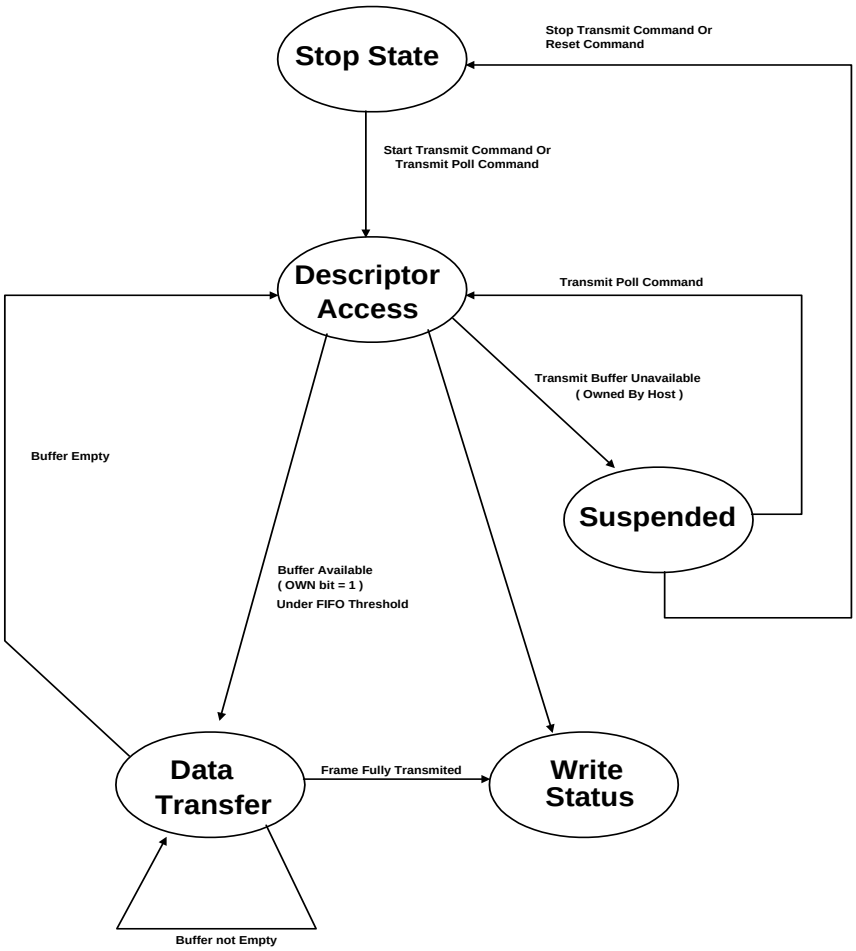


Receive Buffer Management State Transition

9.1.2. Transmit Data Buffer Processing

When start/stop transmit command is set and the DM9103 is in running state, the transmit process polls the transmit descriptor list for frames requiring transmission. When it completes a frame transmission, the status related to the transmitted frame will be written into the transmit descriptor. If the DM9103 detects a descriptor flagged as owned by the host and no transmit buffers are available, the transmit process will be suspended. While in the running state, the transmit process can simultaneously acquire two frames. As the transmit process completes copying the first frame, it immediately polls the transmit descriptor list for the second frame. If the second frame is valid, the transmit process copies the frame before writing the status information of the first frame.

Both conditions below will make transmit process be suspended : (i) The DM9103 detects a descriptor owned by the host. (ii) A frame transmission is aborted when a locally induced error is detected. Under either condition, the host driver has to service the condition before the DM9103 can resume.



Transmit Buffer Management State Transition

9.2 Switch function:

9.2.1 Address Learning

The DM9103 has a self-learning mechanism for learning the MAC addresses of incoming packets in real time. DM9103 stores MAC addresses, port number and time stamp information in the Hash-based Address Table. It can learn up to 1K unicast address entry.

The switch engine updates address table with new entry if incoming packet's Source Address (SA) does not exist and incoming packet is valid (non-error and legal length).

Besides, DM9103 has an option to disable address learning for individual port. This feature can be set by bit 24 of register CR19

9.2.2 Address Aging

The time stamp information of address table is used in the aging process. The switch engine updates time stamp whenever the corresponding SA receives. The switch engine would delete the entry if its time stamp is not updated for a period of time.

The period can be programmed or disabled through bit 0 & 1 of register CR16.

9.2.3 Packet Forwarding

The DM9103 forwards the incoming packet according to following decision:

(1). If DA is Multicast/Broadcast, the packet is forwarded to all ports, except to the port on which the packet was received.

(2). Switch engine would look up address table based on DA when incoming packets is UNICAST. If the DA was not found in address table, the packet is treated as a multicast packet and forward to other ports. If the DA was found and its destination port number is different to source port number, the packet is forward to destination port.

(3). Switch engine also look up VLAN, Port Monitor setting and other forwarding constraints for the forwarding decision, more detail will discuss in later sections.

The DM9103 will filter incoming packets under following conditions:

(1). Error packets, including CRC errors, alignment errors, illegal size errors.

(2). PAUSE packets.

(3). If incoming packet is UNICAST and its destination port number is equal to source port number.

9.2.4 Inter-Packet Gap (IPG)

IPG is the idle time between any two valid packets at the same port. The typical number is 96 bits time. In other word, the value is 9.6u sec for 10Mbps and 960n sec for 100Mbps.

9.2.5 Back-off Algorithm

The DM9103 implements the binary exponential back-off algorithm in half-duplex mode compliant to IEEE standard 802.3.

9.2.6 Late Collision

Late Collision is a type of collision. If a collision error occurs after the first 512 bit times of data are transmitted, the packet is dropped.

9.2.7 Half Duplex Flow Control

The DM9103 supports IEEE standard 802.3x flow control frames on both transmit and receive sides.

On the receive side, The DM9103 will defer transmitting next normal frames, if it receives a pause frame from link partner.

On the transmit side, The DM9103 issues pause frame with maximum pause time when internal resources such as received buffers, transmit queue and transmit descriptor ring are unavailable. Once resources are available, The DM9103 sends out a pause frame with zero pause time allows traffic to resume immediately.

9.2.8 Full Duplex Flow Control

The DM9103 supports half-duplex backpressure. The inducement is the same as full duplex mode. When flow control is required, the DM9103 sends jam pattern, thus forcing a collision.

The flow control ability can be set in bit 4 of register CR18.

9.2.9 Partition Mode

The DM9103 provides a partition mode for each port, see bit 6 of register CR18. The port enters

partition mode when more than 64 consecutive collisions are occurred. In partition mode the port continuous to transmit but it will not receive. The port returned to normal operation mode when a good packet is seen on the wire. The detail description of partition mode represent following:

(1). Entering Partition State

A port will enter the Partition State when either of the following conditions occurs:

- The port detects a collision on every one of 64 consecutive re-transmit attempts to the same packet.
- The port detects a single collision which occurs for more than 512 bit times.
- Transmit defer timer time out, which indicates the transmitting packet is deferred to long.

(2). While in Partition state:

The port will continue to transmit its pending packet, regardless of the collision detection, and will not allow the usual Back-off Algorithm. Additional packets pending for transmission will be transmitted, while ignoring the internal collision indication. This frees up the port's transmit buffers which would otherwise be filled up at the expense of other ports buffers. The assumption is that the partition is signifying a system failure situation (bad connection/cable/station), thus dropping packets is a small price to pay vs. the cost of halting the switch due to a buffer full condition.

(3). Exiting from Partition State

The Port exits from Partition State, following the end of a successful packet transmission. A successful packet transmission is defined as no collisions were detected on the first 512 bits of the transmission.

9.2.10 Broadcast Storm Filtering

The DM9103 has an option to limit the traffic of broadcast or multicast packets, to protect the switch from lower bandwidth availability.

There are two type of broadcast storm control, one is throttling broadcast packet only, the other includes multicast. This feature can be set through bit 0 of register CR18.

The broadcast storm threshold can be programmed by EEPROM or bit 23~20 of CR18, the default setting is no broadcast storm protecting.

9.2.11 Bandwidth Control

The DM9103 supports two type of bandwidth control for each port. One is the ingress and egress bandwidth rate can be control separately, the other is combined together, this function can be set through bit 3 of register CR18. The bandwidth control is disabled by default.

For separated bandwidth control mode, the threshold rate is defined in bit 15~8 of register CR18. For combined mode, it is defined in bit 19~16 of register CR18.

The behavior of bandwidth control as below:

(1).For the ingress control, if flow control function is enabled, Pause or Jam packet will be transmitted. The ingress packets will be dropped if flow control is disabled.

(2).For the egress control, the egress port will not transmit any packets. On the other hand, the ingress bandwidth of source port will be throttled that prevent packets from forwarding.

(3).In combined mode, if the sum of ingress and egress bandwidth over threshold, the bandwidth will be throttled.

9.2.12 Port Monitoring Support

The DM9103 supports "Port Monitoring" function on per port base, detail as below:

(1). Sniffer Port and Monitor Port

There is only one port can be selected as "sniffer port" by bit 4~3 of register CR16, multiple ports can be set as "receive monitor port" or "transmit monitor port" in per-port bit 29 and 30 of register CR19 respectively.

(2).Receive monitor

All packets received on the "receive monitor port" are send a copy to "sniffer port". For example, port 0 is set as "receive monitor port" and port 3 is selected as "sniffer port". If a packet is received form port 0 and predestined to port 1 after forwarding decision, the DM9103 will forward it to port 1 and port 3 in the end.

(3).Transmit monitor

All packets transmitted on the "transmit monitor port" are send a copy to "sniffer port". For example, port 1 is set as "transmit monitor port" and port 3 is selected as "sniffer port". If a packet is received from port 0 and predestined to port 1 after forwarding decision, the DM9103 will forward it to port 1 and port 3 in the end.

(4).Exception

The DM9103 has an optional setting that broadcast/multicast packets are not monitored (see bit 28 of register CR19). It's useful to avoid unnecessary bandwidth.

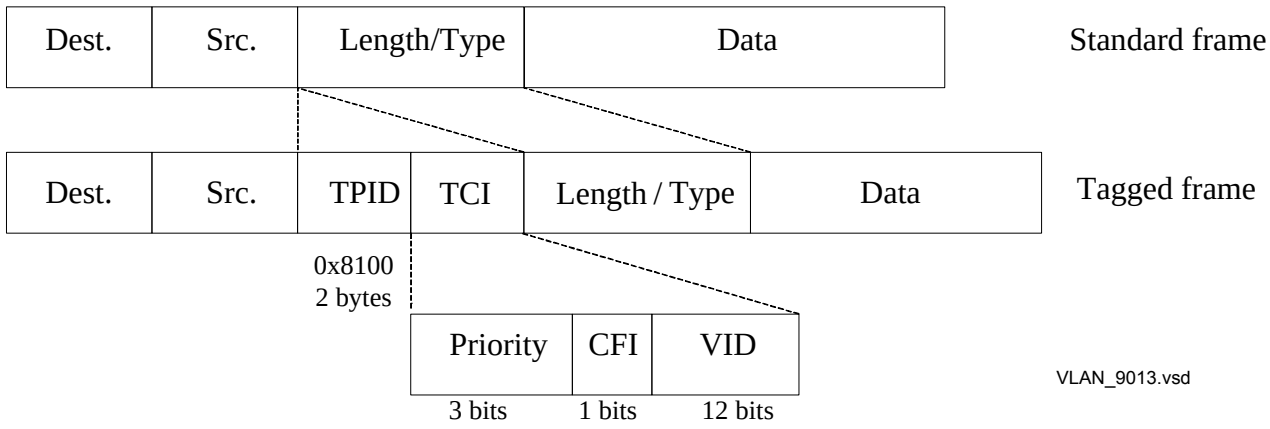
9.2.13 VLAN Support

9.2.13.1 Port-Based VLAN

The DM9103 supports port-based VLAN as default, up to 16 groups. Each port has a default VID called PVID (Port VID, see bit 11~0 of register CR20). The DM9103 used LSB 4-bytes of PVID as index and mapped to register CR24~27, to define the VLAN groups.

9.2.13.2 802.1Q-Based VLAN

Regarding IEEE 802.1Q standard, Tag-based VLAN uses an extra tag to identify the VLAN membership of a frame across VLAN-aware switch/router. A tagged frame is four bytes longer than an untagged frame and contains two bytes of TPID (Tag Protocol Identifier) and two bytes of TCI (Tag Control Information).



The DM9103 also supports 16 802.1Q-based VLAN groups, as specified in bit 8 of register CR16. It's obvious that the tagged packets can be assigned to several different VLANs which are determined according to the VID inside the VLAN Tag. Therefore, the operation is similar to port-based VLAN. The DM9103 used LSB 4-bytes VID of received packet with VLAN tag and VLAN Group Mapping Register (CR24~CR27) to configure the VLAN partition. If the destination port of received packet is not same VLAN group with received port, it will be discarded.

9.2.13.3 Tag/Untag

User can define each port as Tag port or Un-tag port by bit 31 of register CR18 in 802.1Q-based VLAN mode. The operation of Tag and Un-tag can explain as below conditions:

(1). Receive untagged packet and forward to Un-tag port.

Received packet will forward to destination port without modification.

(2). Receive tagged packet and forward to Un-tag port.

The DM9103 will remove the tag from the packet and recalculate CRC before sending it out.

(3). Receive untagged packet and forward to Tag port.

The DM9103 will insert the PVID tag when an untagged packet enters the port, and recalculate CRC before delivering it.

(4). Receive tagged packet and forward to Tag port.

Received packet will forward to destination port without modification.

9.2.14 Priority Support

The DM9103 supports Quality of Service (QoS) mechanism for multimedia communication such as VoIP and video conferencing.

The DM9103 provides three priority classifications: Port-based, 802.1p-based and DiffServ-based priority. See next section for more detail. The DM9103 offers four level queues for transmit on per-port based.

The DM9103 provides two packet scheduling algorithms: Weighted Fair Queuing and Strict Priority Queuing. Weighted Fair Queuing (WFQ) based on their priority and queue weight. Queues with larger weights get more service than smaller. This mechanism can get highly efficient bandwidth and smooth the traffic. Strict Priority Queuing (SPQ) based on priority only. The Packet on the highest priority queue is transmitted first. The next highest-priority queue is work until last queue empties, and so on. This feature can be set in bit 29 of register CR18.

9.2.14.1 Port-Based Priority

Port based priority is the simplest scheme and as default. Each port has a 2-bit priority value as index for splitting ingress packets to the corresponding transmit queue. This value can be set in bit 24 and 25 of register CR18.

9.2.14.2 802.1p-Based Priority

802.1p priority can be disabled by bit 26 of register CR18, it is enabled by default.

The DM9103 extracts 3-bit priority field from received packet with 802.1p VLAN tag, and maps this field against VLAN Priority Map Register CR23 to determine which transmit queue is designated. The VLAN Priority Map is programmable.

9.2.14.3 DiffServ-Based Priority

DiffServ based priority uses the most significant 6-bit of the ToS field in standard IPv4 header, and maps this field against ToS Priority Map Registers (C0h~CFh) to determine which transmit queue is designated. The ToS Priority Map is programmable too. In addition, User can only refer to most significant 3-bit of the ToS field optionally, see bit 15 of register CR16.

9.3 MII Interface

9.3.1 MII data interface

The DM9103 port 2 provides a Media Independent Interface (MII) as defined in the IEEE 802.3u standard (Clause 22).

The MII consists of a nibble wide receive data bus, a nibble wide transmit data bus, and control signals to facilitate data transfers between the DM9103 port 2 and external device (a PHY or a MAC in reverse MII).

- TXD2 (transmit data) is a nibble (4 bits) of data that are driven by the DM9103 synchronously with respect to TXC2. For each TXC2 period, which TXE2 is asserted, TXD2 (3:0) are accepted for transmission by the external device.
- TXC2 (transmit clock) from the external device is a continuous clock that provides the timing reference for the transfer of the TXE2, TXD2. The DM9103 can drive 25MHz clock if it is configured to reversed MII mode.
- TXE2 (transmit enable) from the DM9103 port 2 MAC indicates that nibbles are being presented on the MII for transmission to the external device.

- RXD2 (receive data) is a nibble (4 bits) of data that are sampled by the DM9103 port 2 MAC synchronously with respect to RXC2. For each RXC2 period which RXDV2 is asserted, RXD2 (3:0) are transferred from the external device to the DM9103 port 2 MAC reconciliation sublayer.
- RXC2 (receive clock) from external device to the DM9103 port 2 MAC reconciliation sublayer is a continuous clock that provides the timing reference for the transfer of the RXDV2, RXD2, and RXER2 signals.
- RXDV2 (receive data valid) input from the external device to indicates that the external device is presenting recovered and decoded nibbles to the DM9103 port 2 MAC reconciliation sublayer. To interpret a receive frame correctly by the reconciliation sublayer, RXDV2 must encompass the frame, starting no later than the Start-of-Frame delimiter and excluding any End-Stream delimiter.
- RXER2 (receive error) input from the external device is synchronously with respect to RXC2. RXER2 will be asserted for 1 or more clock periods to indicate to the reconciliation sublayer that an error was detected somewhere in the frame being transmitted from the external device to the DM9103 port 2 MAC.
- CRS2 (carrier sense) is asserted by the external device when either the transmit or receive medium is non-idle, and de-asserted by the external device when the transmit and receive medium are idle. The CRS2 can also in output mode when the DM9103 port 2 is configured to reversed MII mode.
- COL2 (collision detection) is asserted by the external device, when both the transmit and receive medium is non-idle, and de-asserted by the external device when the either transmit or receive medium are idle. The COL2 can also in output mode when the DM9103 port 2 is configured to reversed MII mode.

9.3.2 MII Serial Management

The MII serial management interface consists of a data interface, basic register set in DM9103 port 0 and 1, and a serial management interface to the register set. Through this interface it is possible to control and configure multiple PHY devices, include internal two ports, get status and error information, and determine the type and capabilities of the attached PHY device(s). The DM9103 default is polling 3 ports basic registers 0,1,4, and 5 to get the link, duplex, and speed status automatically. Alternatively, the DM9103 can be programmed to read or write any registers of 3 ports by section 6.8~11 CSR B,C,D,and E.

The DM9103 management functions correspond to MII specification for IEEE 802.3u-1995 (Clause 22) for registers 0 through 6 with vendor-specific registers 16,17, 18, 21, 22, 23 and 24~27.

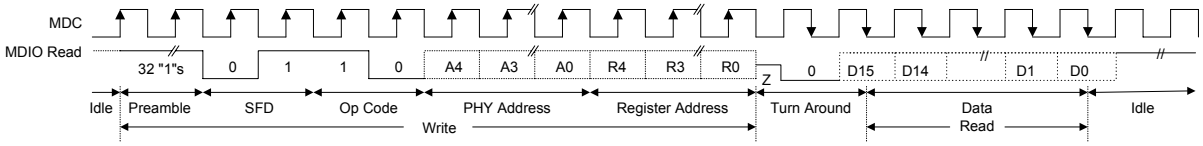
In read/write operation, the management data frame is 64-bits long and starts with 32 contiguous logic one bits (preamble) synchronization clock cycles on MDC. The Start of Frame Delimiter (SFD) is indicated by a <01> pattern followed by the operation code (OP):<10> indicates Read operation and <01> indicates Write operation. For read operation, a 2-bit turnaround (TA) filing between Register Address field and Data field is provided for MDIO to avoid contention. Following the turnaround time, 16-bit data is read from or written onto management registers.

9.3.3 Serial Management Interface

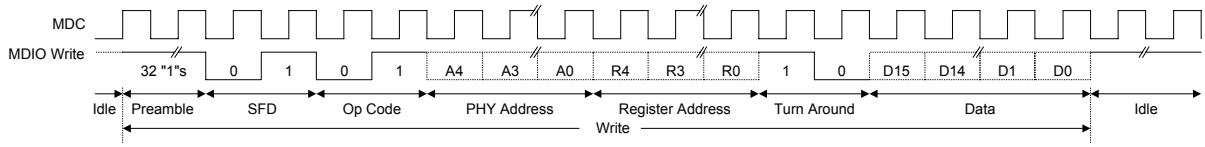
The serial control interface uses a simple two-wired serial interface to obtain and control the status of the physical layer through the MII interface. The serial control interface consists of MDC (Management Data Clock), and MDI/O (Management Data Input/Output) signals.

The MDIO pin is bi-directional and may be shared by up to 32 devices.

9.3.4 Management Interface - Read Frame Structure



9.3.5 Management Interface - Write Frame Structure



9.4 Internal PHY functions

9.4.1 100Base-TX Operation

The transmitter section contains the following functional blocks:

- 4B5B Encoder
- Scrambler
- Parallel to Serial Converter
- NRZ to NRZI Converter
- NRZI to MLT-3
- MLT-3 Driver

9.4.1.1 4B5B Encoder

The 4B5B encoder converts 4-bit (4B) nibble data generated by the MAC Reconciliation Layer into a 5-bit (5B) code group for transmission, see reference Table 1. This conversion is required for control and packet data to be combined in code groups. The 4B5B encoder substitutes the first 8 bits of the MAC preamble with a J/K code-group pair (11000 10001) upon transmit. The 4B5B encoder continues to replace subsequent 4B preamble and data nibbles with corresponding 5B code-groups. At the end of the transmit packet, upon the deassertion of the Transmit Enable signal from the MAC Reconciliation layer, the 4B5B encoder injects the T/R code-group pair (01101 00111) indicating the end of frame. After the T/R code-group pair, the 4B5B encoder continuously injects IDLEs into the transmit data stream until Transmit Enable is asserted and the next transmit packet is detected.

9.4.1.2 Scrambler

The scrambler is required to control the radiated emissions (EMI) by spreading the transmit energy across the frequency spectrum at the media connector and on the twisted pair cable in 100Base-TX operation.

By scrambling the data, the total energy presented to the cable is randomly distributed over a wide frequency range. Without the scrambler, energy levels on the cable could peak beyond FCC limitations at frequencies related to the repeated 5B sequences, like the continuous transmission of IDLE symbols. The scrambler output is combined with the NRZ 5B data from the code-group encoder via an XOR logic function. The result is a scrambled data stream with sufficient randomization to decrease radiated emissions at critical frequencies.

9.4.1.3 Parallel to Serial Converter

The Parallel to Serial Converter receives parallel 5B scrambled data from the scrambler, and serializes it (converts it from a parallel to a serial data stream). The serialized data stream is then presented to the NRZ to NRZI encoder block

9.4.1.4 NRZ to NRZI Encoder

After the transmit data stream has been scrambled and serialized, the data must be NRZI encoded for compatibility with the TP-PMD standard, for 100Base -TX transmission over Category-5 unshielded twisted pair cable.

9.4.1.5 MLT-3 Converter

The MLT-3 conversion is accomplished by converting the data stream output, from the NRZI encoder into two binary data streams, with alternately phased logic one event.

9.4.1.6 MLT-3 Driver

The two binary data streams created at the MLT-3 converter are fed to the twisted pair output driver, which converts these streams to current sources and alternately drives either side of the transmit transformer's primary winding, resulting in a minimal current MLT-3 signal.

9.4.1.7 4B5B Code Group

Symbol	Meaning	4B code 3210	5B Code 43210
0	Data 0	0000	11110
1	Data 1	0001	01001
2	Data 2	0010	10100
3	Data 3	0011	10101
4	Data 4	0100	01010
5	Data 5	0101	01011
6	Data 6	0110	01110
7	Data 7	0111	01111
8	Data 8	1000	10010
9	Data 9	1001	10011
A	Data A	1010	10110
B	Data B	1011	10111
C	Data C	1100	11010
D	Data D	1101	11011
E	Data E	1110	11100
F	Data F	1111	11101
I	Idle	undefined	11111
J	SFD (1)	0101	11000
K	SFD (2)	0101	10001
T	ESD (1)	undefined	01101
R	ESD (2)	undefined	00111
H	Error	undefined	00100
V	Invalid	undefined	00000
V	Invalid	undefined	00001
V	Invalid	undefined	00010
V	Invalid	undefined	00011
V	Invalid	undefined	00101
V	Invalid	undefined	00110
V	Invalid	undefined	01000
V	Invalid	undefined	01100
V	Invalid	undefined	10000
V	Invalid	undefined	11001

Table 1

9.4.2 100Base-TX Receiver

The 100Base-TX receiver contains several function blocks that convert the scrambled 125Mb/s serial data to synchronous 4-bit nibble data.
The receive section contains the following functional blocks:

- Signal Detect
- Digital Adaptive Equalization
- MLT-3 to Binary Decoder
- Clock Recovery Module
- NRZI to NRZ Decoder
- Serial to Parallel
- Descrambler
- Code Group Alignment
- 4B5B Decoder

9.4.2.1 Signal Detect

The signal detect function meets the specifications mandated by the ANSI XT12 TP-PMD 100Base-TX standards for both voltage thresholds and timing parameters.

9.4.2.2 Adaptive Equalization

When transmitting data over copper twisted pair cable at high speed, attenuation based on frequency becomes a concern. In high speed twisted pair signaling, the frequency content of the transmitted signal can vary greatly during normal operation based on the randomness of the scrambled data stream. This variation in signal attenuation, caused by frequency variations, must be compensated for to ensure the integrity of the received data. In order to ensure quality transmission when employing MLT-3 encoding, the compensation must be able to adapt to various cable lengths and cable types depending on the installed environment. The selection of long cable lengths for a given implementation requires significant compensation, which will be over-killed in a situation that includes shorter, less attenuating cable lengths. Conversely, the selection of short or intermediate cable lengths requiring less compensation will cause serious under-compensation for longer length cables. Therefore, the compensation or equalization must be adaptive to ensure proper conditioning of the received signal independent of the cable length.

9.4.2.3 MLT-3 to NRZI Decoder

The DM9103 decodes the MLT-3 information from the Digital Adaptive Equalizer into NRZI data.

9.4.2.4 Clock Recovery Module

The Clock Recovery Module accepts NRZI data from the MLT-3 to NRZI decoder. The Clock Recovery Module locks onto the data stream and extracts the 125Mhz reference clock. The extracted and synchronized clock and data are presented to the NRZI to NRZ decoder.

9.4.2.5 NRZI to NRZ

The transmit data stream is required to be NRZI encoded for compatibility with the TP-PMD standard for 100Base-TX transmission over Category-5 unshielded twisted pair cable. This conversion process must be reversed on the receive end. The NRZI to NRZ decoder, receives the NRZI data stream from the Clock Recovery Module and converts it to a NRZ data stream to be presented to the Serial to Parallel conversion block.

9.4.2.6 Serial to Parallel

The Serial to Parallel Converter receives a serial data stream from the NRZI to NRZ converter. It converts the data stream to parallel data to be presented to the descrambler.

9.4.2.7 Descrambler

Because of the scrambling process requires to control the radiated emissions of transmit data streams, the receiver must descramble the receive data streams. The descrambler receives scrambled parallel data streams from the Serial to Parallel converter, and it descrambles the data streams, and presents the data streams to the Code Group alignment block.

9.4.2.8 Code Group Alignment

The Code Group Alignment block receives un-aligned 5B data from the descrambler and converts it into 5B code group data. Code Group Alignment occurs after the J/K is detected, and subsequent data is aligned on a fixed boundary.

9.4.2.9 4B5B Decoder

The 4B5B Decoder functions as a look-up table that translates incoming 5B code groups into 4B (Nibble) data. When receiving a frame, the first 2 5-bit code groups receive the start-of-frame delimiter (J/K symbols). The J/K symbol pair is stripped and two nibbles of preamble pattern are substituted. The last two code groups are the end-of-frame delimiter (T/R Symbols).

The T/R symbol pair is also stripped from the nibble, presented to the Reconciliation layer.

9.4.3 10Base-T Operation

The 10Base-T transceiver is IEEE 802.3u compliant. When the DM9103 is operating in 10Base-T mode, the coding scheme is Manchester. Data processed for transmit is presented in nibble format, converted to a serial bit stream, then the Manchester encoded. When receiving, the bit stream, encoded by the Manchester, is decoded and converted into nibble format.

9.4.4 Collision Detection

For half-duplex operation, a collision is detected when the transmit and receive channels are active simultaneously. Collision detection is disabled in full duplex operation.

9.4.5 Carrier Sense

Carrier Sense (CRS) is asserted in half-duplex operation during transmission or reception of data. During full-duplex mode, CRS is asserted only during receive operations.

9.4.6 Auto-Negotiation

The objective of Auto-negotiation is to provide a means to exchange information between linked devices and to automatically configure both devices to take maximum advantage of their abilities. It is important to note that Auto-negotiation does not test the characteristics of the linked segment. The Auto-Negotiation function provides a means for a device to advertise supported modes of operation to a remote link partner, acknowledge the receipt and understanding of common modes of operation, and to reject un-shared modes of operation. This allows devices on both ends of a segment to establish a link at the best common mode of operation. If more than one common mode exists between the two devices, a mechanism is provided to allow the devices to resolve to a single mode of operation using a predetermined priority resolution function.

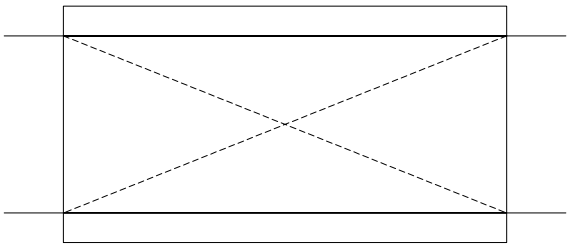
Auto-negotiation also provides a parallel detection function for devices that do not support the Auto-negotiation feature. During Parallel detection there is no exchange of information of configuration. Instead, the receive signal is examined. If it is discovered that the signal matches a technology, which the receiving device supports, a connection will be automatically established using that technology. This allows devices not to support Auto-negotiation but support a common mode of operation to establish a link.

9.5 Auto MDIX HP Auto-MDIX Functional Description

The DM9103 supports the automatic detect cable connection type, MDI/MDIX (straight through/cross over). A manual configuration by register bit for MDI or MDIX is still accepted.

When set to automatic, the polarity of MDI/MDIX controlled timing is generated by a 16-bits LFSR. The switching cycle time is located from 200ms to 420ms. The polarity control is always switch until detect received signal. After selected MDI or MDIX,
This feature is able to detect the required cable connection type.(straight through or crossed over) and make correction automatically

RX + /- from DM9103 RX+/- to RJ45



TX + /- from DM9103 TX+/- to RJ45

* MDI : _____

* MDIX : - - - - - - - - -

10. DC and AC Electrical Characteristics

10.1 Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit	Conditions
VCC3	3.3V Supply Voltage	-0.3	3.6	V	
VCCI	1.8V core power supply	-0.3	1.95	V	
AVDD3	Analog power supply 3.3V	-0.3	3.6	V	
AVDDI	Analog power supply 1.8V	-0.3	1.95	V	
V_{IN}	DC Input Voltage (VIN)	-0.5	5.5	V	
T_{STG}	Storage Temperature range	-65	+150	°C	
T_C	Case Temperature	-	+85	°C	as T_A=70°C
T_A	Ambient Temperature	0	+70	°C	
L_T	Lead Temperature (TL,soldering,10 sec.).	-	+260	°C	Lead-free Device

10.2 Operating Conditions

Symbol	Parameter	Min.	Max.	Unit	Conditions
VCC3	3.3V Supply Voltage	3.135	3.465	V	
VCCI	1.8V core power supply	1.71	1.89	V	
AVDD3	Analog power supply 3.3V	3.135	3.465	V	
AVDDI	Analog power supply 1.8V	1.71	1.89	V	
P_D (Power Dissipation)	100BASE-TX	-	300	mA	3.3V
	10BASE-T TX (100% utilization)	-	400	mA	3.3V
	Auto-negotiation	-	430	mA	3.3V
	Power Down Mode	-	40	mA	3.3V

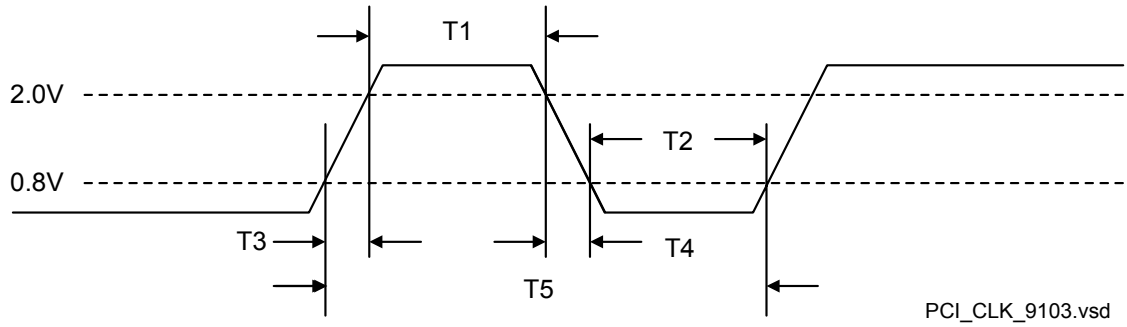
10.3 DC Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Inputs						
VIL	Input Low Voltage	-	-	0.8	V	Vcond1
VIH	Input High Voltage	2.0	-	-	V	Vcond1
IIL	Input Low Leakage Current	-1	-	-	uA	VIN = 0.0V, Vcond1
IIH	Input High Leakage Current	-	-	1	uA	VIN = 3.3V, Vcond1
Outputs						
VOL	Output Low Voltage	-	-	0.4	V	IOL = 4mA
VOH	Output High Voltage	2.4	-	-	V	IOH = -4mA
Receiver						
VICM	RX+/RX- Common Mode Input Voltage	-	1.8	-	V	100 Ω Termination Across
Transmitter						
VTD100	100TX+/- Differential Output Voltage	1.9	2.0	2.1	V	Peak to Peak
VTD10	10TX+/- Differential Output Voltage	4.4	5	5.6	V	Peak to Peak
ITD100	100TX+/- Differential Output Current	|19|	|20|	|21|	mA	Absolute Value
ITD10	10TX+/- Differential Output Current	|44|	|50|	|56|	mA	Absolute Value

Note: Vcond1 = VCC3 = 3.3V, VCCI = 1.8V, AVDD3 = 3.3V, AVDDI = 1.8V.

10.3 AC characteristics

10.3.1 PCI Clock Specifications Timing

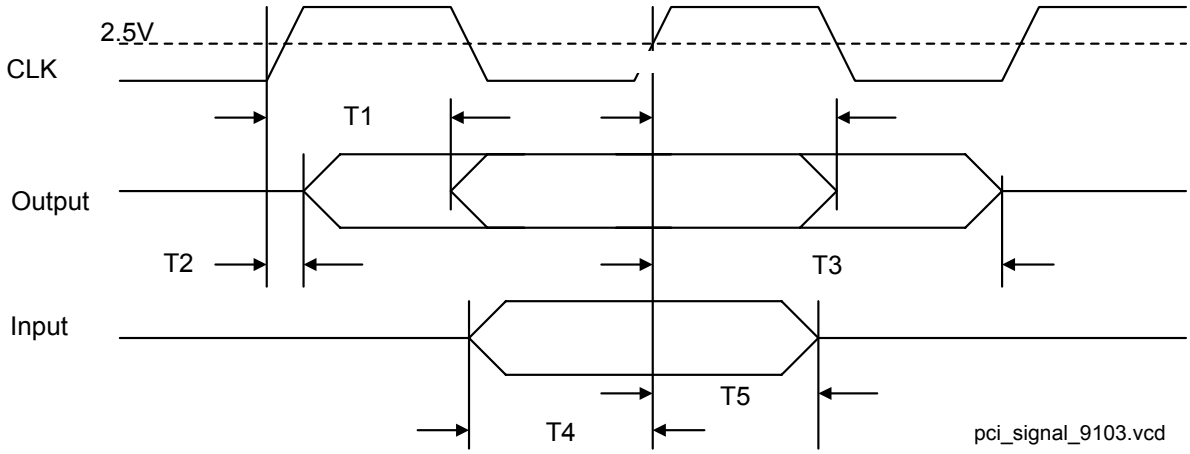


Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
T1	PCI_CLK High Time	12	-	-	ns	-
T2	PCI_CLK Low Time	12	-	-	ns	-
T3	PCI_CLK Rising Time	-	-	4	ns	-
T4	PCI_CLK Falling Time	-	-	4	ns	-
T5	Cycle Time	25	30	-	ns	-

10.3.2 Power On Reset Timing

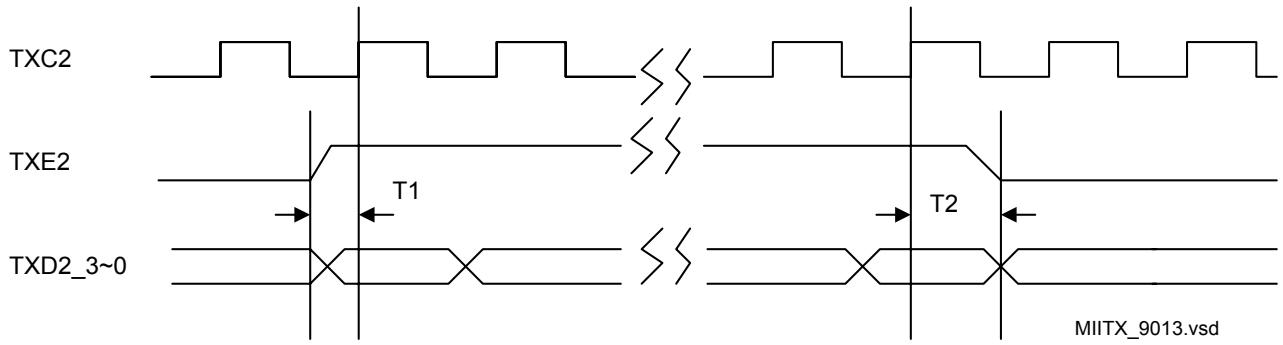
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
T1	PWRST# Low Period	1	-	-	ms	-
T2	Strap pin hold time with PWRST#	40	-	-	ns	-

10.3.3 Other PCI Signals Timing Diagram



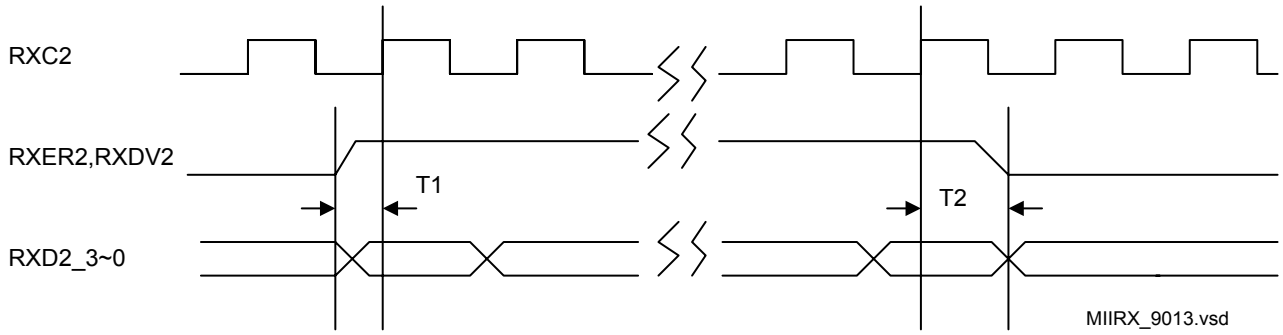
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
T1	Clk-To-Signal Valid Delay	2	-	13	ns	Cload = 50 pF
T2	Float-To-Active Delay From Clk	2	-	-	ns	-
T3	Active-To-Float Delay From Clk	-	-	28	ns	-
T4	Input Signal Valid Setup Time Before Clk	7	-	-	ns	-
T5	Input Signal Hold Time From Clk	0	-	-	ns	-

10.3.4 Port 2 MII Interface Transmit Timing



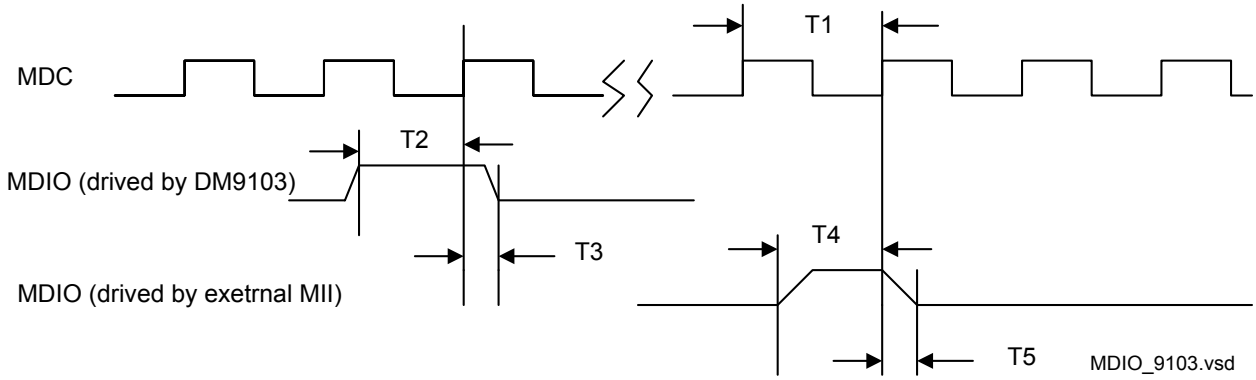
Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	TXE2,TXD2_3~0 Setup Time		32		ns
T2	TXE2,TXD2_3~0 Hold Time		8		ns

10.3.5 Port 2 MII Interface Receive Timing



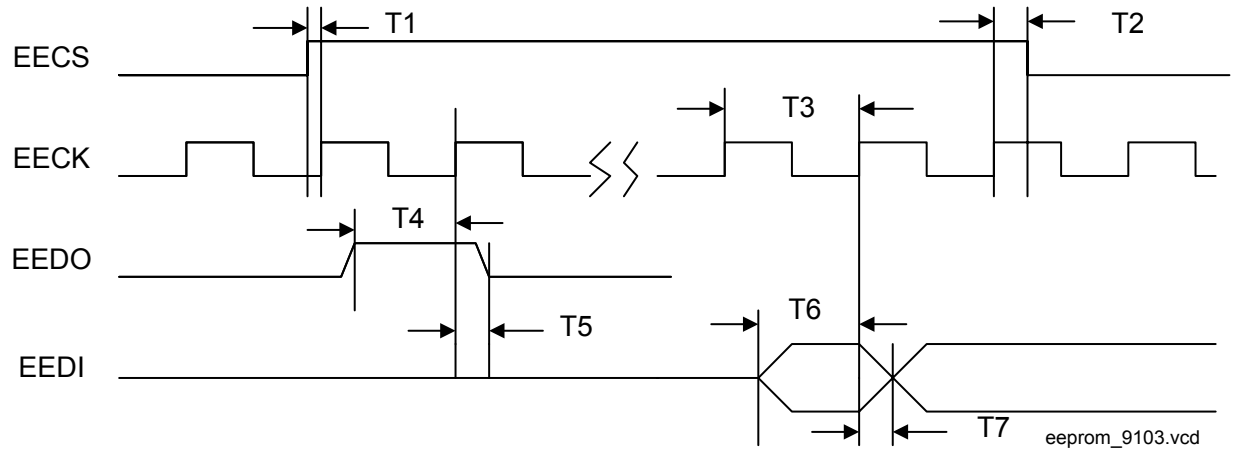
Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	RXER2, RXDV2,RXD2_3~0 Setup Time	5			ns
T2	RXER2, RXDV2,RXD2_3~0 Hold Time	5			ns

10.3.6 MII Management Interface Timing



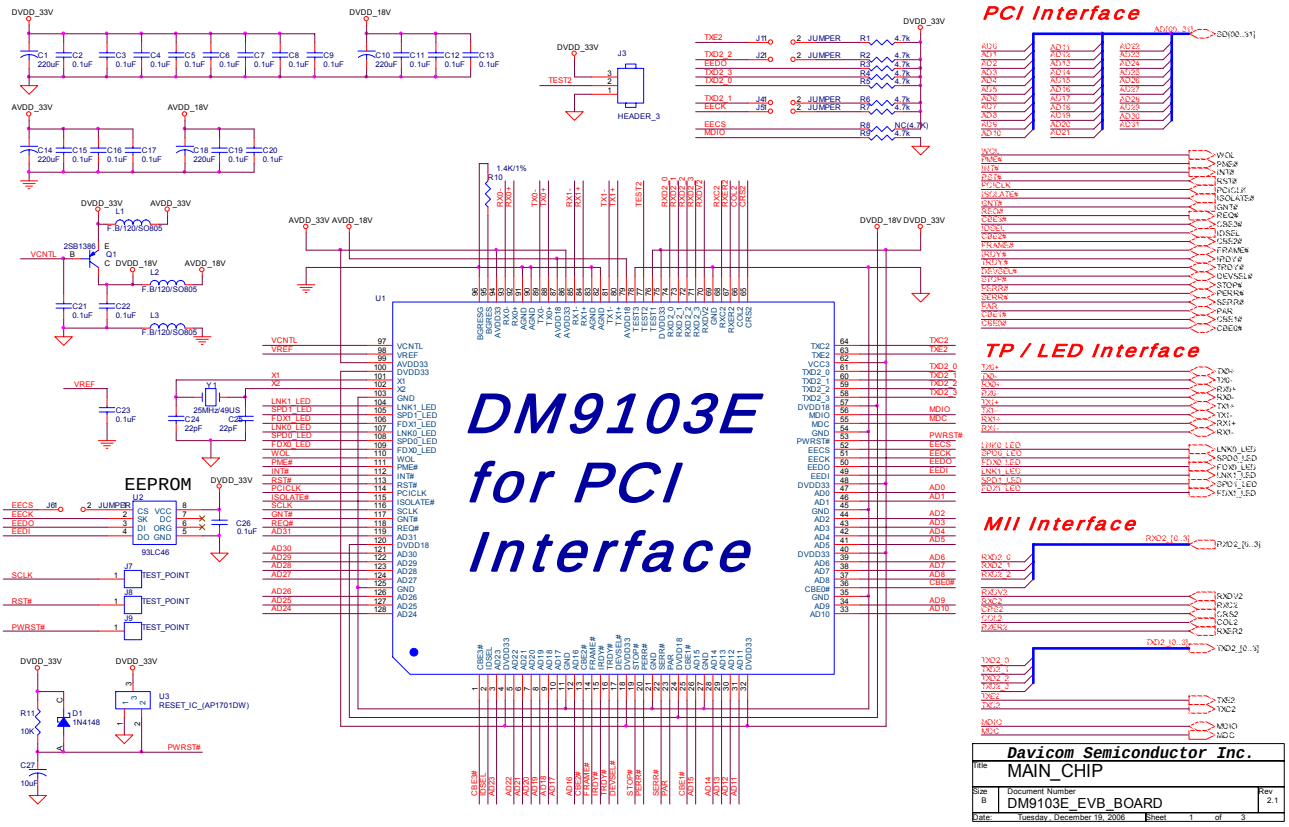
Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	MDC Frequency		0.52		MHz
T2	MDIO by DM9103 Setup Time		955		ns
T3	MDIO by DM9103 Hold Time		960		ns
T4	MDIO by External MII Setup Time	40			ns
T5	MDIO by External MII Hold Time	40			ns

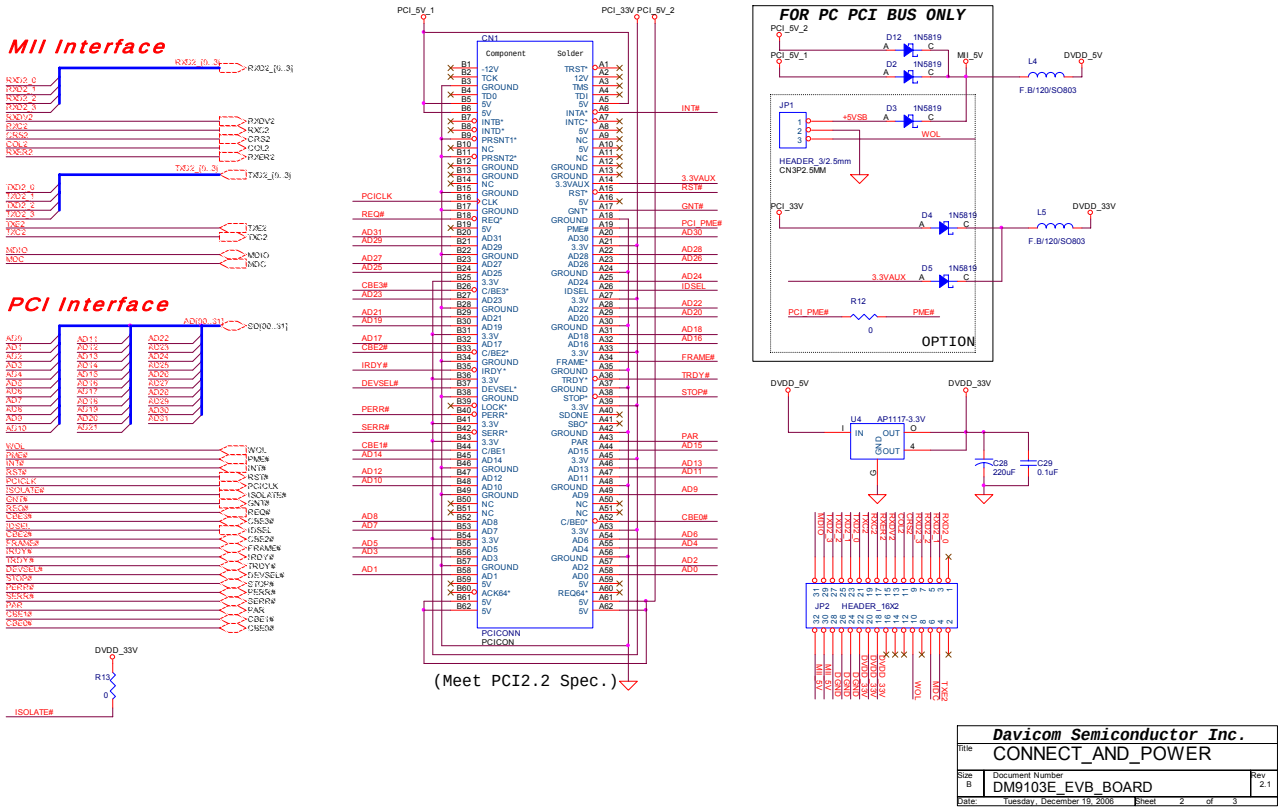
10.3.7 EEPROM timing

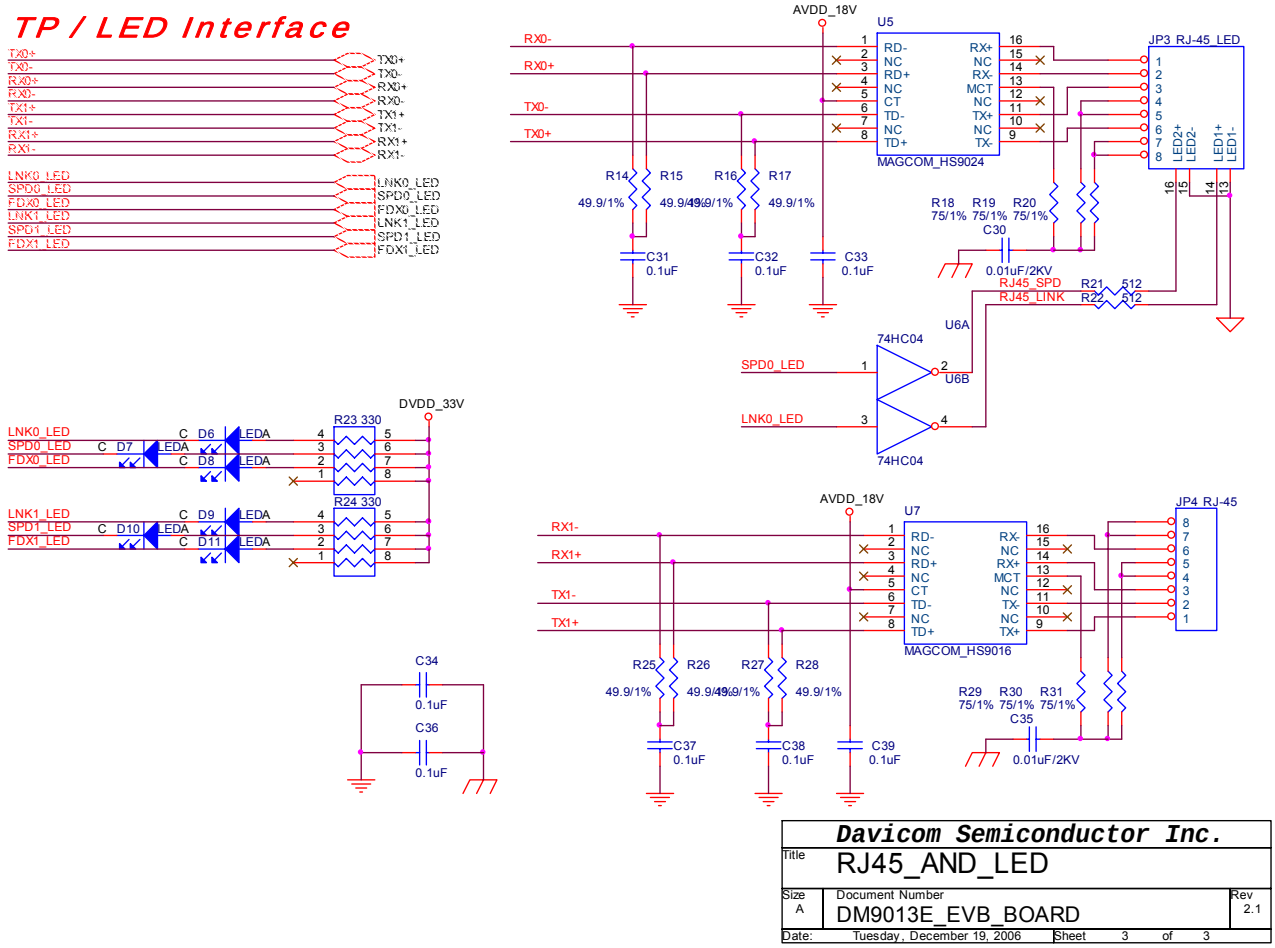


Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	EECS Setup Time		480		ns
T2	EECS Hold Time		2080		ns
T3	EECK Frequency		0.38		MHz
T4	EEDO Setup Time		460		
T5	EEDO Hold Time		2100		ns
T6	EEDI Setup Time	8			ns
T7	EEDI Hold Time	8			ns

11. Application circuit



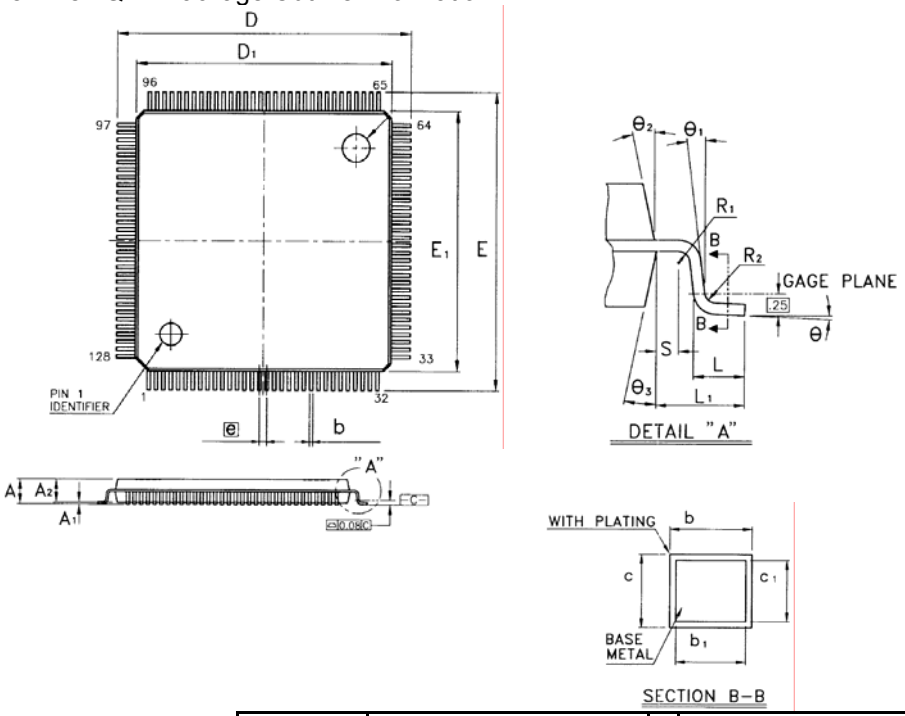

MII Interface
PCI Interface
PCI_5V_1
PCI_33V
PCI_5V_2
CN1
Component
Solder
PCICONN
PCICON
(Meet PCI2.2 Spec.)
FOR PC PCI BUS ONLY
PCI_5V_2
PCI_5V_1
MII_5V
DVDD_5V
F.B/120/SO803
JP1
+5VSB
WOL
HEADER_3/2.5mm
CN3P2.5MM
PCI_33V
DVDD_33V
3.3VAUX
PCI_PME#
PME#
R12
OPTION
DVDD_5V
DVDD_33V
U4
AP1117-3.3V
C28
220uF
C29
0.1uF
JP2
HEADER_16X2
DVDD_33V
R13
ISOLATE#
Davicom Semiconductor Inc.
CONNECT_AND_POWER
DM9103E_EVB_BOARD
Tuesday, December 19, 2006



Davicom Semiconductor Inc.		
Title: RJ45_AND_LED		
Size: A	Document Number: DM9013E_EVB_BOARD	Rev: 2.1
Date: Tuesday, December 19, 2006	Sheet 3 of 3	

12. Package Information

128 Pins LQFP Package Outline Information:



Symbol	Dimension in mm				Dimension in inch		
	Min	Nom	Max		Min	Nom	Max
A	-	-	1.60		-	-	0.063
A_1	0.05	-	-		0.002	-	-
A_2	1.35	1.40	1.45		0.053	0.055	0.057
b	0.13	0.18	0.23		0.005	0.007	0.009
b_1	0.13	0.16	0.19		0.005	0.006	0.007
c	0.09	-	0.20		0.004	-	0.008
c_1	0.09	-	0.16		0.004	-	0.006
D	15.85	16.00	16.15		0.624	0.630	0.636
D_1	13.90	14.00	14.10		0.547	0.551	0.555
E	15.85	16.00	16.15		0.624	0.630	0.636
E_1	13.90	14.00	14.10		0.547	0.551	0.555
e	0.40 BSC				0.016 BSC		
L	0.45	0.60	0.75		0.018	0.024	0.030
L_1	1.00 REF				0.039 REF		
R_1	0.08	-	-		0.003	-	-
R_2	0.08	-	0.20		0.003	-	0.008
S	0.20	-	-		0.008	-	-
θ	0°	3.5°	7°		0°	3.5°	7°
θ_1	0°	-	-		0°	-	-
θ_2	12° TYP				12° TYP		
θ_3	12° TYP				12° TYP		

1. Dimension D_1 and E_1 do not include resin fin.
2. All dimensions are base on metric system.
3. General appearance spec should base on its final visual inspection spec.

13. Ordering Information

Part Number	Pin Count	Package
DM9103EP	128	LQFP (Pb-free)

Disclaimer

The information appearing in this publication is believed to be accurate. Integrated circuits sold by DAVICOM Semiconductor are covered by the warranty and patent indemnification provisions stipulated in the terms of sale only. DAVICOM makes no warranty, express, statutory, implied or by description regarding the information in this publication or regarding the information in this publication or regarding the freedom of the described chip(s) from patent infringement. FURTHER, DAVICOM MAKES NO WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PURPOSE. DAVICOM reserves the right to halt production or alter the specifications and prices at any time without notice. Accordingly, the reader is cautioned to verify that the data sheets and other information in this publication are current before placing orders. Products described herein are intended for use in normal commercial applications. Applications involving unusual environmental or reliability requirements, e.g. military equipment or medical life support equipment, are specifically not recommended without additional processing by DAVICOM for such applications. Please note that application circuits illustrated in this document are for reference purposes only.

DAVICOM's terms and conditions printed on the order acknowledgment govern all sales by DAVICOM. DAVICOM will not be bound by any terms inconsistent with these unless DAVICOM agrees otherwise in writing. Acceptance of the buyer's orders shall be based on these terms.

Company Overview

DAVICOM Semiconductor Inc. develops and manufactures integrated circuits for integration into data communication products. Our mission is to design and produce IC products that are the industry's best value for Data, Audio, Video, and Internet/Intranet applications. To achieve this goal, we have built an organization that is able to develop chipsets in response to the evolving technology requirements of our customers while still delivering products that meet their cost requirements.

Products

We offer only products that satisfy high performance requirements and which are compatible with major hardware and software standards. Our currently available and soon to be released products are based on our proprietary designs and deliver high quality, high performance chipsets that comply with modem communication standards and Ethernet networking standards.

Contact Windows

For additional information about DAVICOM products, contact the Sales department at:

Headquarters

Hsin-chu Office:
No.6 Li-Hsin Rd. VI,
Science-based Park,
Hsin-chu City, Taiwan, R.O.C.
TEL: + 886-3-5798797
FAX: + 886-3-5646929
MAIL: sales@davicom.com.tw
HTTP: http://www.davicom.com.tw

WARNING

Conditions beyond those listed for the absolute maximum may destroy or damage the products. In addition, conditions for sustained periods at near the limits of the operating ranges will stress and may temporarily (and permanently) affect and damage structure, performance and/or function.