

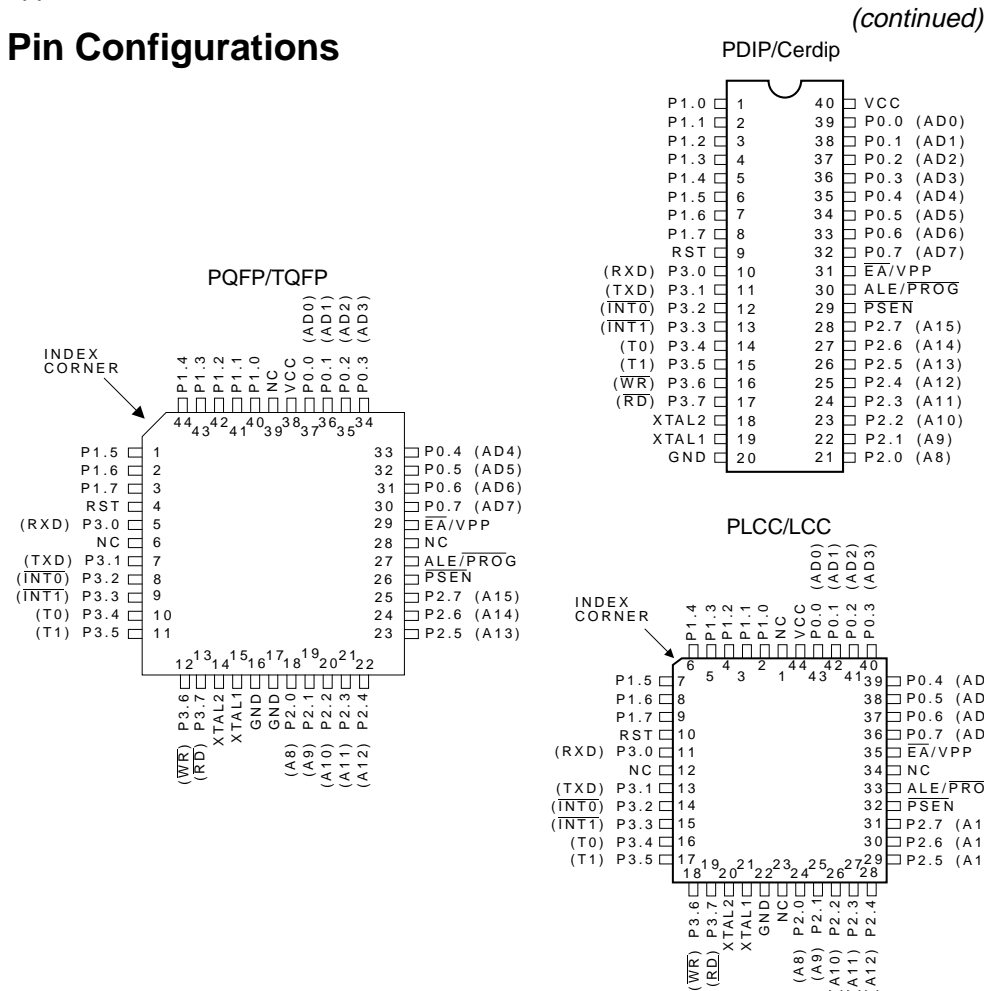
Features

- Compatible with MCS-51™ Products
- 4 Kbytes of In-System Reprogrammable Flash Memory
Endurance: 1,000 Write/Erase Cycles
- Fully Static Operation: 0 Hz to 24 MHz
- Three-Level Program Memory Lock
- 128 x 8-Bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-Bit Timer/Counters
- Six Interrupt Sources
- Programmable Serial Channel
- Low Power Idle and Power Down Modes

Description

The AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4 Kbytes of Flash Programmable and Erasable Read Only Memory (PEROM). The device is manufactured using Atmel's high density nonvolatile memory technology and is compatible with the industry standard MCS-51™ instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications.

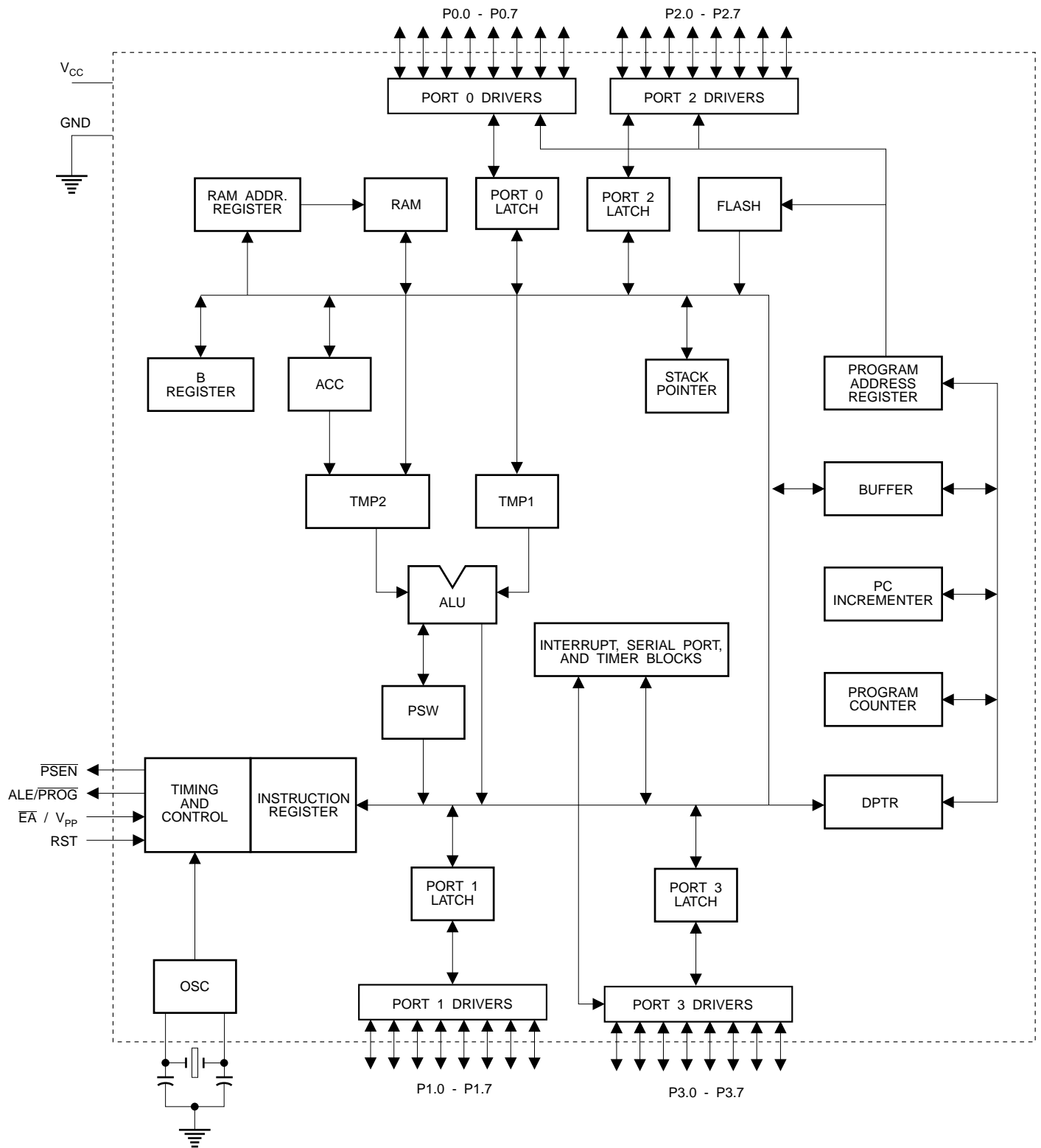
Pin Configurations



8-Bit Microcontroller with 4 Kbytes Flash

AT89C51

Block Diagram



Description (Continued)

The AT89C51 provides the following standard features: 4 Kbytes of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit timer/counters, a five vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator and clock circuitry. In addition, the AT89C51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power Down Mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset.

Pin Description

V_{CC}

Supply voltage.

GND

Ground.

Port 0

Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 may also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode P0 has internal pullups.

Port 0 also receives the code bytes during Flash programming, and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1

Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 1 also receives the low-order address bytes during Flash programming and program verification.

Port 2

Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX

@ DPTR). In this application it uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification. Port 3

Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89C51 as listed below:

| Port Pin | Alternate Functions |
|----------|--|
| P3.0 | RXD (serial input port) |
| P3.1 | TXD (serial output port) |
| P3.2 | $\overline{\text{INT0}}$ (external interrupt 0) |
| P3.3 | $\overline{\text{INT1}}$ (external interrupt 1) |
| P3.4 | T0 (timer 0 external input) |
| P3.5 | T1 (timer 1 external input) |
| P3.6 | $\overline{\text{WR}}$ (external data memory write strobe) |
| P3.7 | $\overline{\text{RD}}$ (external data memory read strobe) |

Port 3 also receives some control signals for Flash programming and programming verification.

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/ $\overline{\text{PROG}}$

Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{\text{PROG}}$) during Flash programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

PSEN

Program Store Enable is the read strobe to external program memory.

(continued)

Pin Description (Continued)

When the AT89C51 is executing code from external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory.

$\overline{\text{EA}}/V_{PP}$

External Access Enable. $\overline{\text{EA}}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, EA will be internally latched on reset.

$\overline{\text{EA}}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming, for parts that require 12-volt V_{PP} .

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier.

Oscillator Characteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

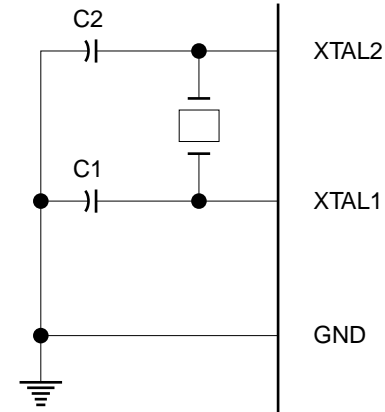
Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this

mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

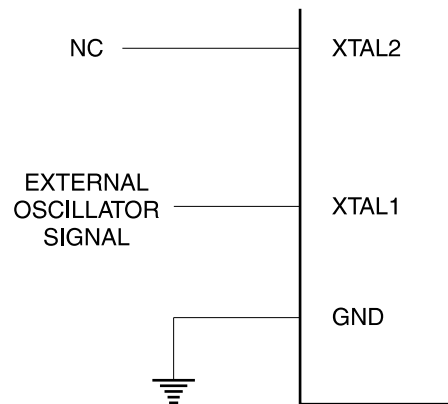
It should be noted that when idle is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hard-

Figure 1. Oscillator Connections



Notes: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 2. External Clock Drive Configuration



Status of External Pins During Idle and Power Down

| Mode | Program Memory | ALE | $\overline{\text{PSEN}}$ | PORT0 | PORT1 | PORT2 | PORT3 |
|------------|----------------|-----|--------------------------|-------|-------|---------|-------|
| Idle | Internal | 1 | 1 | Data | Data | Data | Data |
| Idle | External | 1 | 1 | Float | Data | Address | Data |
| Power Down | Internal | 0 | 0 | Data | Data | Data | Data |
| Power Down | External | 0 | 0 | Float | Data | Data | Data |

ware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

Power Down Mode

In the power down mode the oscillator is stopped, and the instruction that invokes power down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power down mode is terminated. The only exit from power down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before Vcc

is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Program Memory Lock Bits

On the chip are three lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below:

When lock bit 1 is programmed, the logic level at the \overline{EA} pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of \overline{EA} be in agreement with the current logic level at that pin in order for the device to function properly.

Lock Bit Protection Modes

| Program Lock Bits | | | | |
|-------------------|-----|-----|-----|--|
| | LB1 | LB2 | LB3 | Protection Type |
| 1 | U | U | U | No program lock features. |
| 2 | P | U | U | MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, \overline{EA} is sampled and latched on reset, and further programming of the Flash is disabled. |
| 3 | P | P | U | Same as mode 2, also verify is disabled. |
| 4 | P | P | P | Same as mode 3, also external execution is disabled. |

Programming the Flash

The AT89C51 is normally shipped with the on-chip Flash memory array in the erased state (that is, contents = FFH) and ready to be programmed. The programming interface accepts either a high-voltage (12-volt) or a low-voltage (Vcc) program enable signal. The low voltage programming mode provides a convenient way to program the AT89C51 inside the user's system, while the high-voltage programming mode is compatible with conventional third party Flash or EPROM programmers.

The AT89C51 is shipped with either the high-voltage or low-voltage programming mode enabled. The respective top-side marking and device signature codes are listed in the following table.

| | VPP = 12 V | VPP = 5 V |
|---------------|--|--|
| Top-Side Mark | AT89C51 xxxx yyww | AT89C51 xxxx-5 yyww |
| Signature | (030H)=1EH (031H)=51H (032H)=FFH | (030H)=1EH (031H)=51H (032H)=05H |

The AT89C51 code memory array is programmed byte-by-byte in either programming mode. *To program any non-blank byte in the on-chip Flash Memory, the entire memory must be erased using the Chip Erase Mode.*

Programming Algorithm: Before programming the AT89C51, the address, data and control signals should be set up according to the Flash programming mode table and Figures 3 and 4. To program the AT89C51, take the following steps.

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise \overline{EA}/V_{PP} to 12 V for the high-voltage programming mode.
5. Pulse $\overline{ALE}/\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 1.5 ms. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

Data Polling: The AT89C51 features \overline{Data} Polling to indicate the end of a write cycle. During a write cycle, an at-

Programming the Flash (Continued)

tempted read of the last byte written will result in the complement of the written datum on PO.7. Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. Data Polling may begin any time after a write cycle has been initiated.

Ready/Busy: The progress of byte programming can also be monitored by the RDY/BSY output signal. P3.4 is pulled low after ALE goes high during programming to indicate BUSY. P3.4 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

Chip Erase: The entire Flash array is erased electrically by using the proper combination of control signals and by holding ALE/PROG low for 10 ms. The code array is written with all "1"s. The chip erase operation must be executed before the code memory can be re-programmed.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H,

031H, and 032H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(030H) = 1EH indicates manufactured by Atmel

(031H) = 51H indicates 89C51

(032H) = FFH indicates 12 V programming





(032H) = 05H indicates 5 V programming

Programming Interface

Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Flash Programming Modes

| Mode | RST | $\overline{\text{PSEN}}$ | ALE/ PROG | EA/ V _{PP} | P2.6 | P2.7 | P3.6 | P3.7 | | | | | | | | |
|---------------------|---------|--------------------------|---|------------------------|------|------|------|------|---------|---|--|-------|---|---|---|---|
| Write Code Data | H | L |  | H/12V ⁽¹⁾ | L | H | H | H | | | | | | | | |
| Read Code Data | H | L | H | H | L | L | H | H | | | | | | | | |
| Write Lock | Bit - 1 | L |  | H/12V | H | H | H | H | | | | | | | | |
| | | | | | | | | | Bit - 2 | L |  ⁽²⁾ | H/12V | H | H | L | L |
| | | | | | | | | | | | | | | | | |
| Chip Erase | H | L |  | H/12V | H | L | L | L | | | | | | | | |
| Read Signature Byte | H | L | H | H | L | L | L | L | | | | | | | | |

Notes: 1. The signature byte at location 032H designates whether V_{PP} = 12 V or V_{PP} = 5 V should be used to enable programming.

2. Chip Erase requires a 10 ms $\overline{\text{PROG}}$ pulse.

Figure 3. Programming the Flash

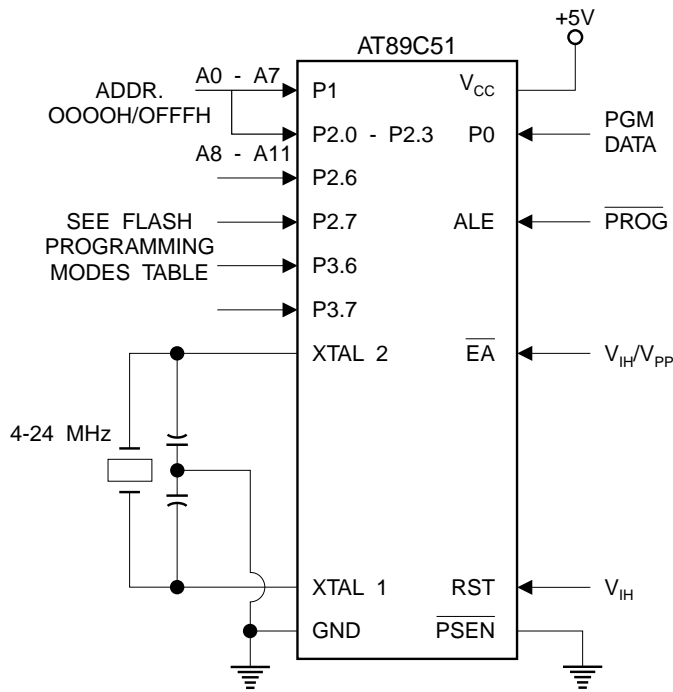
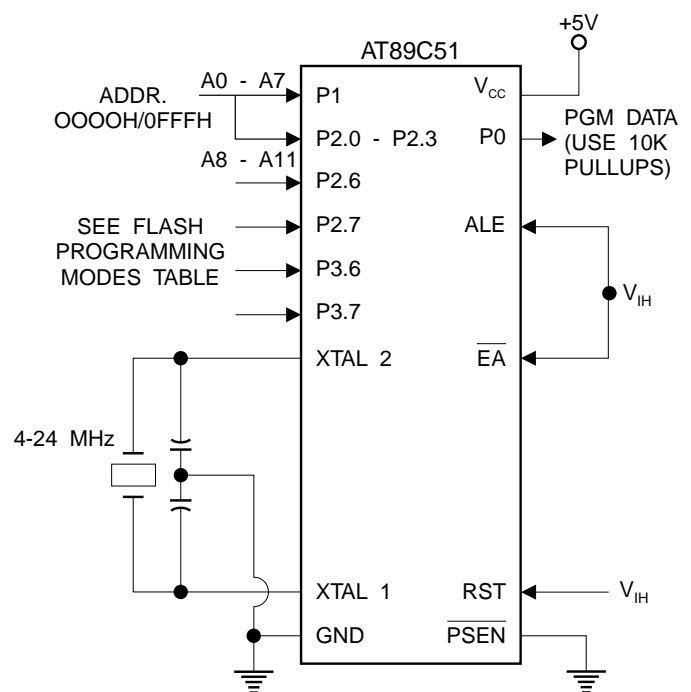


Figure 4. Verifying the Flash



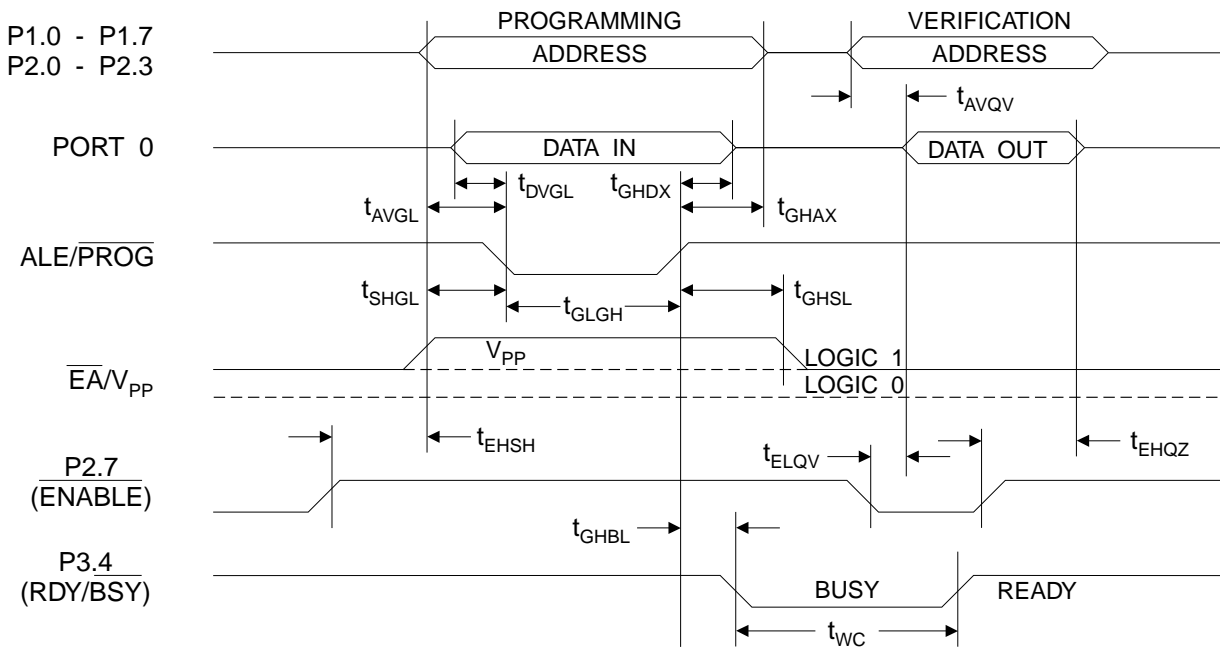
Flash Programming and Verification Characteristics

$T_A = 21^\circ\text{C}$ to 27°C , $V_{CC} = 5.0 \pm 10\%$

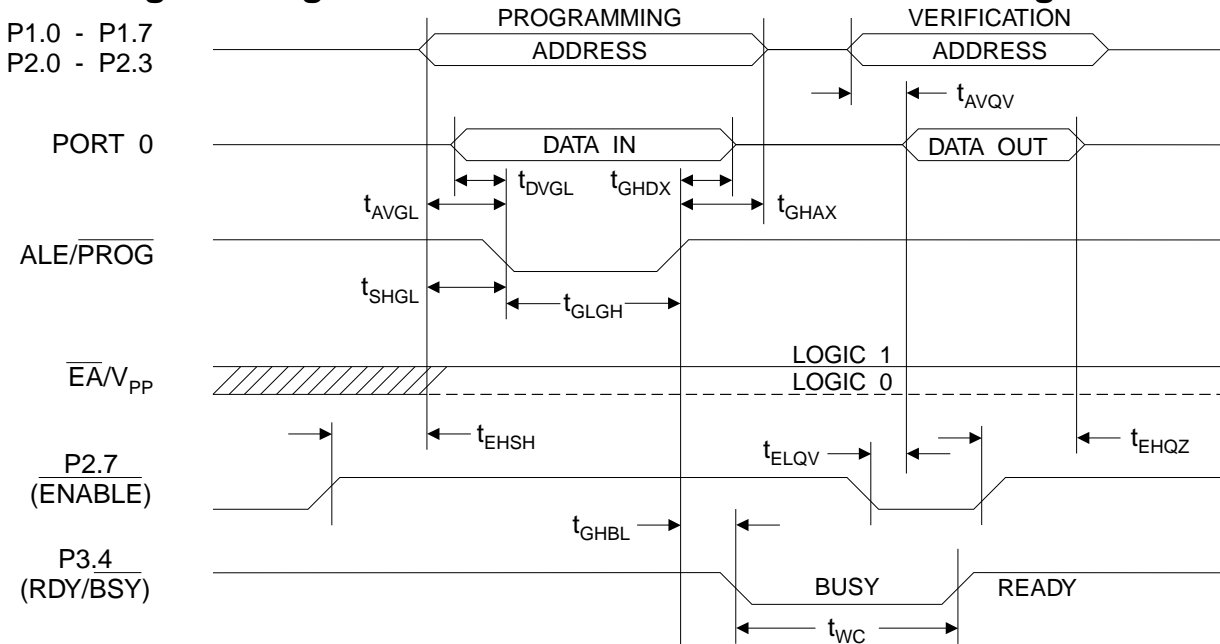
| Symbol | Parameter | Min | Max | Units |
|------------------|---|--------------|--------------|---------------|
| $V_{PP}^{(1)}$ | Programming Enable Voltage | 11.5 | 12.5 | V |
| $I_{PP}^{(1)}$ | Programming Enable Current | | 1.0 | mA |
| $1/t_{CLCL}$ | Oscillator Frequency | 4 | 24 | MHz |
| t_{AVGL} | Address Setup to $\overline{\text{PROG}}$ Low | $48t_{CLCL}$ | | |
| t_{GHAX} | Address Hold After $\overline{\text{PROG}}$ | $48t_{CLCL}$ | | |
| t_{DVGL} | Data Setup to $\overline{\text{PROG}}$ Low | $48t_{CLCL}$ | | |
| t_{GHDX} | Data Hold After $\overline{\text{PROG}}$ | $48t_{CLCL}$ | | |
| t_{ESHSH} | P2.7 ($\overline{\text{ENABLE}}$) High to V_{PP} | $48t_{CLCL}$ | | |
| t_{SHGL} | V_{PP} Setup to $\overline{\text{PROG}}$ Low | 10 | | μs |
| $t_{GHSL}^{(1)}$ | V_{PP} Hold After $\overline{\text{PROG}}$ | 10 | | μs |
| t_{GLGH} | $\overline{\text{PROG}}$ Width | 1 | 110 | μs |
| t_{AVQV} | Address to Data Valid | | $48t_{CLCL}$ | |
| t_{ELQV} | $\overline{\text{ENABLE}}$ Low to Data Valid | | $48t_{CLCL}$ | |
| t_{EHQV} | Data Float After $\overline{\text{ENABLE}}$ | 0 | $48t_{CLCL}$ | |
| t_{GHBL} | $\overline{\text{PROG}}$ High to $\overline{\text{BUSY}}$ Low | | 1.0 | μs |
| t_{WC} | Byte Write Cycle Time | | 2.0 | ms |

Note: 1. Only used in 12-volt programming mode.

Flash Programming and Verification Waveforms - High Voltage Mode



Flash Programming and Verification Waveforms - Low Voltage Mode



Absolute Maximum Ratings*

| | |
|--|------------------|
| Operating Temperature..... | -55°C to +125°C |
| Storage Temperature..... | -65°C to +150°C |
| Voltage on Any Pin with Respect to Ground | -1.0 V to +7.0 V |
| Maximum Operating Voltage | 6.6 V |
| DC Output Current..... | 15.0 mA |

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

T_A = -40°C to 85°C, V_{CC} = 5.0 V ± 20% (unless otherwise noted)

| Symbol | Parameter | Condition | Min | Max | Units |
|------------------|--|--|--------------------------|--------------------------|-------|
| V _{IL} | Input Low Voltage | (Except \overline{EA}) | -0.5 | 0.2 V _{CC} -0.1 | V |
| V _{IL1} | Input Low Voltage (\overline{EA}) | | -0.5 | 0.2 V _{CC} -0.3 | V |
| V _{IH} | Input High Voltage | (Except XTAL1, RST) | 0.2 V _{CC} +0.9 | V _{CC} +0.5 | V |
| V _{IH1} | Input High Voltage | (XTAL1, RST) | 0.7 V _{CC} | V _{CC} +0.5 | V |
| V _{OL} | Output Low Voltage ⁽¹⁾ (Ports 1,2,3) | I _{OL} = 1.6 mA | | 0.45 | V |
| V _{OL1} | Output Low Voltage ⁽¹⁾ (Port 0, ALE, PSEN) | I _{OL} = 3.2 mA | | 0.45 | V |
| V _{OH} | Output High Voltage (Ports 1,2,3, ALE, PSEN) | I _{OH} = -60 μA, V _{CC} = 5 V ± 10% | 2.4 | | V |
| | | I _{OH} = -25 μA | 0.75 V _{CC} | | V |
| | | I _{OH} = -10 μA | 0.9 V _{CC} | | V |
| V _{OH1} | Output High Voltage (Port 0 in External Bus Mode) | I _{OH} = -800 μA, V _{CC} = 5 V ± 10% | 2.4 | | V |
| | | I _{OH} = -300 μA | 0.75 V _{CC} | | V |
| | | I _{OH} = -80 μA | 0.9 V _{CC} | | V |
| I _{IL} | Logical 0 Input Current (Ports 1,2,3) | V _{IN} = 0.45 V | | -50 | μA |
| I _{TL} | Logical 1 to 0 Transition Current (Ports 1,2,3) | V _{IN} = 2 V | | -650 | μA |
| I _{LI} | Input Leakage Current (Port 0, \overline{EA}) | 0.45 < V _{IN} < V _{CC} | | ±10 | μA |
| RRST | Reset Pulldown Resistor | | 50 | 300 | KΩ |
| C _{IO} | Pin Capacitance | Test Freq. = 1 MHz, T _A = 25°C | | 10 | pF |
| I _{CC} | Power Supply Current | Active Mode, 12 MHz | | 20 | mA |
| | | Idle Mode, 12 MHz | | 5 | mA |
| | Power Down Mode ⁽²⁾ | V _{CC} = 6 V | | 100 | μA |
| | | V _{CC} = 3 V | | 40 | μA |

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
 Maximum I_{OL} per port pin: 10 mA
 Maximum I_{OL} per 8-bit port:
 Port 0: 26 mA
 Ports 1, 2, 3: 15 mA

Maximum total I_{OL} for all output pins: 71 mA
 If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
 2. Minimum V_{CC} for Power Down is 2 V.

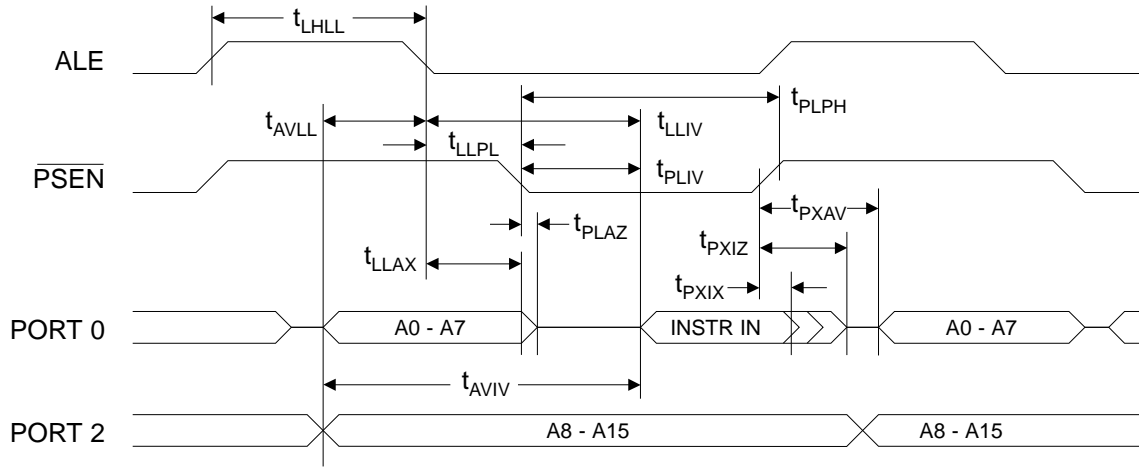
A.C. Characteristics

(Under Operating Conditions; Load Capacitance for Port 0, ALE/PROG, and PSEN = 100 pF; Load Capacitance for all other outputs = 80 pF)

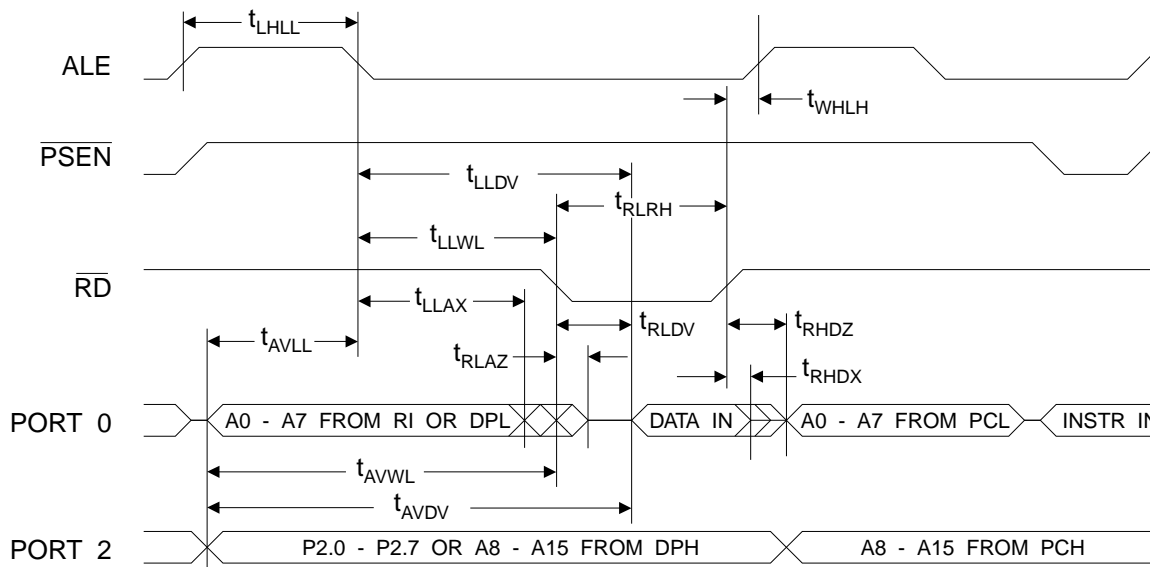
External Program and Data Memory Characteristics

| Symbol | Parameter | 12 MHz Oscillator | | 16 to 24 MHz Oscillator | | Units |
|---------------------|------------------------------------|-------------------|-----|-------------------------|-------------------------|-------|
| | | Min | Max | Min | Max | |
| 1/t _{CLCL} | Oscillator Frequency | | | 0 | 24 | MHz |
| t _{LHLL} | ALE Pulse Width | 127 | | 2t _{CLCL} -40 | | ns |
| t _{AVLL} | Address Valid to ALE Low | 28 | | t _{CLCL} -13 | | ns |
| t _{LLAX} | Address Hold After ALE Low | 48 | | t _{CLCL} -20 | | ns |
| t _{LLIV} | ALE Low to Valid Instruction In | | 233 | | 4t _{CLCL} -65 | ns |
| t _{LLPL} | ALE Low to PSEN Low | 43 | | t _{CLCL} -13 | | ns |
| t _{PLPH} | PSEN Pulse Width | 205 | | 3t _{CLCL} -20 | | ns |
| t _{PLIV} | PSEN Low to Valid Instruction In | | 145 | | 3t _{CLCL} -45 | ns |
| t _{PXIX} | Input Instruction Hold After PSEN | 0 | | 0 | | ns |
| t _{PXIZ} | Input Instruction Float After PSEN | | 59 | | t _{CLCL} -10 | ns |
| t _{PXAV} | PSEN to Address Valid | 75 | | t _{CLCL} -8 | | ns |
| t _{AVIV} | Address to Valid Instruction In | | 312 | | 5t _{CLCL} -55 | ns |
| t _{PLAZ} | PSEN Low to Address Float | | 10 | | 10 | ns |
| t _{RLRH} | RD Pulse Width | 400 | | 6t _{CLCL} -100 | | ns |
| t _{WLWH} | WR Pulse Width | 400 | | 6t _{CLCL} -100 | | ns |
| t _{RLDV} | RD Low to Valid Data In | | 252 | | 5t _{CLCL} -90 | ns |
| t _{RHDX} | Data Hold After RD | 0 | | 0 | | ns |
| t _{RHDZ} | Data Float After RD | | 97 | | 2t _{CLCL} -28 | ns |
| t _{LLDV} | ALE Low to Valid Data In | | 517 | | 8t _{CLCL} -150 | ns |
| t _{AVDV} | Address to Valid Data In | | 585 | | 9t _{CLCL} -165 | ns |
| t _{LLWL} | ALE Low to RD or WR Low | 200 | 300 | 3t _{CLCL} -50 | 3t _{CLCL} +50 | ns |
| t _{AVWL} | Address to RD or WR Low | 203 | | 4t _{CLCL} -75 | | ns |
| t _{QVWX} | Data Valid to WR Transition | 23 | | t _{CLCL} -20 | | ns |
| t _{QVWH} | Data Valid to WR High | 433 | | 7t _{CLCL} -120 | | ns |
| t _{WHQX} | Data Hold After WR | 33 | | t _{CLCL} -20 | | ns |
| t _{RLAZ} | RD Low to Address Float | | 0 | | 0 | ns |
| t _{WHLH} | RD or WR High to ALE High | 43 | 123 | t _{CLCL} -20 | t _{CLCL} +25 | ns |

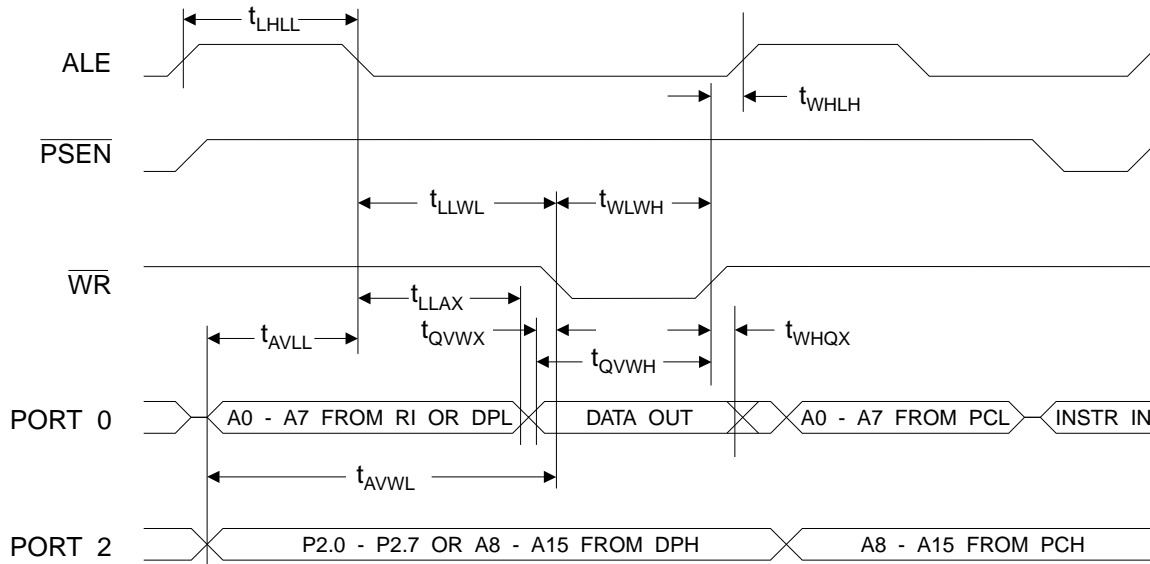
External Program Memory Read Cycle



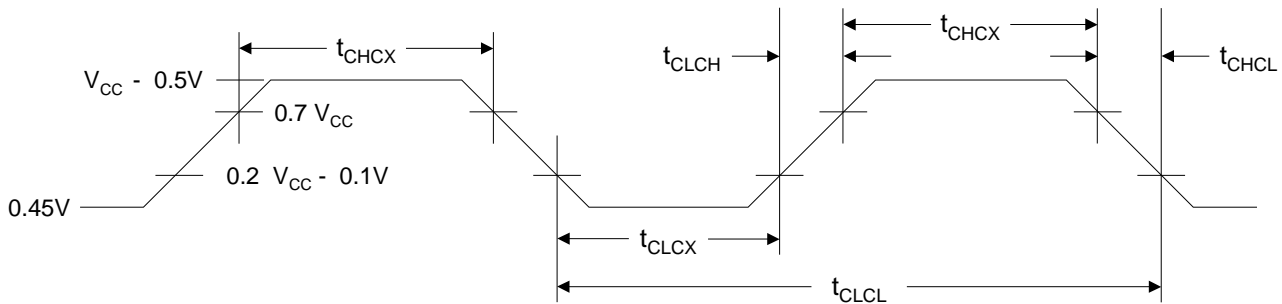
External Data Memory Read Cycle



External Data Memory Cycle



External Clock Drive Waveforms



External Clock Drive

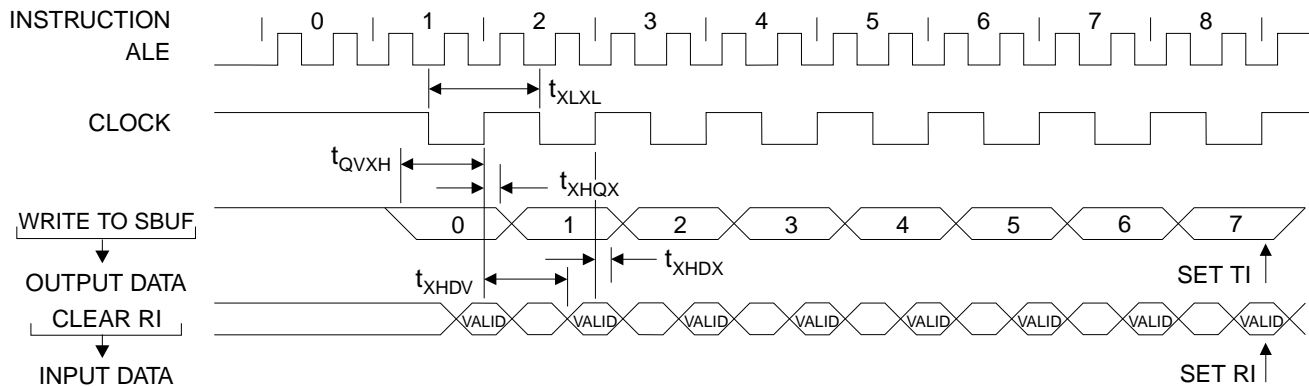
| Symbol | Parameter | Min | Max | Units |
|--------------|----------------------|------|-----|-------|
| $1/t_{CLCL}$ | Oscillator Frequency | 0 | 24 | MHz |
| t_{CLCL} | Clock Period | 41.6 | | ns |
| t_{CHCX} | High Time | 15 | | ns |
| t_{CLCX} | Low Time | 15 | | ns |
| t_{CLCH} | Rise Time | | 20 | ns |
| t_{CHCL} | Fall Time | | 20 | ns |

Serial Port Timing: Shift Register Mode Test Conditions

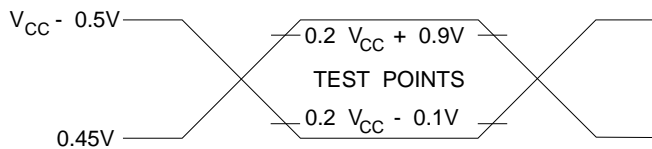
(V_{CC} = 5.0 V ± 20%; Load Capacitance = 80 pF)

| Symbol | Parameter | 12 MHz Osc | | Variable Oscillator | | Units |
|-------------------|--|------------|-----|--------------------------|--------------------------|-------|
| | | Min | Max | Min | Max | |
| t _{XLXL} | Serial Port Clock Cycle Time | 1.0 | | 12t _{CLCL} | | μs |
| t _{QVXH} | Output Data Setup to Clock Rising Edge | 700 | | 10t _{CLCL} -133 | | ns |
| t _{XHQX} | Output Data Hold After Clock Rising Edge | 50 | | 2t _{CLCL} -33 | | ns |
| t _{XHDX} | Input Data Hold After Clock Rising Edge | 0 | | 0 | | ns |
| t _{XHDV} | Clock Rising Edge to Input Data Valid | | 700 | | 10t _{CLCL} -133 | ns |

Shift Register Mode Timing Waveforms

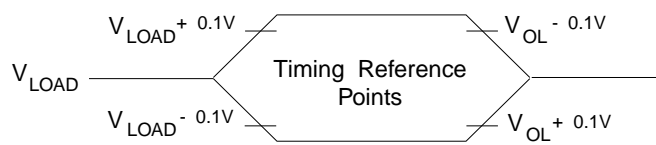


AC Testing Input/Output Waveforms ⁽¹⁾



Note: 1. AC Inputs during testing are driven at $V_{CC} - 0.5 V$ for a logic 1 and $0.45 V$ for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms ⁽¹⁾



Note: 1. For timing purposes, a port pin is no longer floating when a $100 mV$ change from load voltage occurs. A port pin begins to float when a $100 mV$ change from the loaded V_{OH}/V_{OL} level occurs.

Ordering Information

| Speed (MHz) | Power Supply | Ordering Code | Package | Operation Range |
|------------------|---------------|---------------|---|-------------------------------|
| 12 | 5 V \pm 20% | AT89C51-12AC | 44A | Commercial (0°C to 70°C) |
| | | AT89C51-12JC | 44J | |
| | | AT89C51-12PC | 40P6 | |
| | | AT89C51-12QC | 44Q | Industrial (-40°C to 85°C) |
| | | AT89C51-12AI | 44A | |
| | | AT89C51-12JI | 44J | |
| | AT89C51-12PI | 40P6 | | |
| | AT89C51-12QI | 44Q | Automotive (-40°C to 125°C) | |
| | AT89C51-12AA | 44A | | |
| | AT89C51-12JA | 44J | | |
| AT89C51-12PA | 40P6 | | | |
| 5 V \pm 10% | AT89C51-12QA | 44Q | Military (-55°C to 125°C) | |
| | AT89C51-12DM | 40D6 | | |
| | AT89C51-12LM | 44L | Military/883C Class B, Fully Compliant (-55°C to 125°C) | |
| AT89C51-12DM/883 | 40D6 | | | |
| AT89C51-12LM/883 | 44L | | | |
| 16 | 5 V \pm 20% | AT89C51-16AC | 44A | Commercial (0°C to 70°C) |
| | | AT89C51-16JC | 44J | |
| | | AT89C51-16PC | 40P6 | |
| | | AT89C51-16QC | 44Q | Industrial (-40°C to 85°C) |
| | | AT89C51-16AI | 44A | |
| | | AT89C51-16JI | 44J | |
| | AT89C51-16PI | 40P6 | | |
| | AT89C51-16QI | 44Q | Automotive (-40°C to 125°C) | |
| | AT89C51-16AA | 44A | | |
| | AT89C51-16JA | 44J | | |
| AT89C51-16PA | 40P6 | | | |
| AT89C51-16QA | 44Q | | | |
| 20 | 5 V \pm 20% | AT89C51-20AC | 44A | Commercial (0°C to 70°C) |
| | | AT89C51-20JC | 44J | |
| | | AT89C51-20PC | 40P6 | |
| | | AT89C51-20QC | 44Q | Industrial (-40°C to 85°C) |
| | | AT89C51-20AI | 44A | |
| | | AT89C51-20JI | 44J | |
| | AT89C51-20PI | 40P6 | | |
| | AT89C51-20QI | 44Q | | |

Ordering Information

| Speed (MHz) | Power Supply | Ordering Code | Package | Operation Range |
|-------------|--------------|---------------|---------|-------------------------------|
| 24 | 5 V ± 20% | AT89C51-24AC | 44A | Commercial (0°C to 70°C) |
| | | AT89C51-24JC | 44J | |
| | | AT89C51-24PC | 44P6 | |
| | | AT89C51-24QC | 44Q | |
| | | AT89C51-24AI | 44A | Industrial (-40°C to 85°C) |
| | | AT89C51-24JI | 44J | |
| | | AT89C51-24PI | 44P6 | |
| | | AT89C51-24QI | 44Q | |

| Package Type | |
|--------------|--|
| 44A | 44 Lead, Thin Plastic Gull Wing Quad Flatpack (TQFP) |
| 40D6 | 40 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip) |
| 44J | 44 Lead, Plastic J-Leaded Chip Carrier (PLCC) |
| 44L | 44 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC) |
| 40P6 | 40 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP) |
| 44Q | 44 Lead, Plastic Gull Wing Quad Flatpack (PQFP) |