

STQ2NF06L

N-CHANNEL 60V - 0.1 Ω - 2A TO-92 STripFET™ II POWER MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STQ2NF06L	60 V	<0.12 Ω	2 A

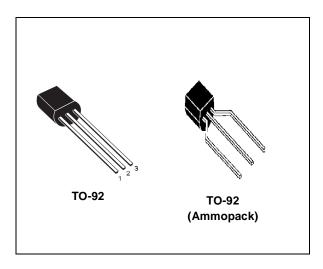
- TYPICAL R_{DS}(on) = 0.1Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- AVALANCHE RUGGED TECHNOLOGY
- LOW THRESHOLD DRIVE

DESCRIPTION

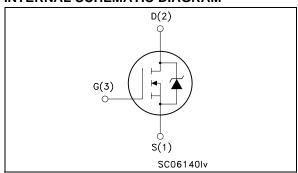
This Power MOSFET is the latest development of STMicroelectronis unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low onresistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

- DC MOTOR CONTROL (DISK DRIVES, etc.)
- DC-DC & DC-AC CONVERTERS
- SYNCHRONOUS RECTIFICATION



INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
VDS	Drain-source Voltage (VGS = 0)	60	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	60	V
VGS	Gate- source Voltage	± 16	V
ΙD	Drain Current (continuous) at T _C = 25°C	2	A
ΙD	Drain Current (continuous) at T _C = 100°C	1.2	A
I _{DM} (•)	Drain Current (pulsed)	8	A
P _{tot} (1)	Total Dissipation at T _C = 25°C	3	W
	Derating Factor	8	W/°C
dv/dt (2)	Peak Diode Recovery voltage slope	6	V/ns
EAS (3)	Single Pulse Avalanche Energy	200	mJ
T _{stg}	Storage Temperature	-55 to 150	°C
Tj	Max. Operating Junction Temperature	55 10 150	°C

^(•) Pulse width limited by safe operating area.
(1) Related to Rthj -I

(2) IsD \leq 2A, di/dt \leq 100A/ μ s, VDD \leq V(BR)DSS, T $_j \leq$ TJMAX (3) Starting T $_j =$ 25 °C, ID = 2A, VDD = 30V

October 2003 1/9

THERMAL DATA

	Rthj- _{lead} Rthj-amb T _l	Thermal Resistance Junction-Lead Thermal Resistance Junction-ambient Maximum Lead Temperature For Soldering Purpose	Max Max Typ	40 125 260	°C/W °C/W °C	
--	---	---	-------------------	------------------	--------------------	--

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V(BR)DSS	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	60			V
IDSS	Zero Gate Voltage Drain Current (V _{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating T_{C} = 125°C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 16 V			±100	nA

ON (*)

Symbol	Parameter	Test Conditions		Min.	Тур.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}$	I _D = 250 μA	1			V
R _{DS(on)}	Static Drain-source On Resistance	V _G S = 10 V V _G S = 5 V	I _D = 1 A I _D = 1 A		0.1 0.12	0.12 0.14	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
9fs (*)	Forward Transconductance	V _{DS} = 15 V I _D = 1 A		3		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 25V f = 1 MHz V _{GS} = 0		360 55 25		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t _{d(on)} t _r	Turn-on Time Rise Time	$\begin{array}{cccc} V_{DD} = 30 \text{ V} & I_D = 1 \text{ A} \\ R_G = 4.7 \ \Omega & V_{GS} = 4.5 \text{ V} \\ \text{(Resistive Load, Figure 3)} \end{array}$		10 20		ns ns
Q _g Q _{gs} Q _{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V _{DD} = 48 V I _D = 2 A V _{GS} = 5 V		5.6 1.2 2.6	7.6	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t _{d(off)} t _f	Turn-off Delay Time Fall Time	$\begin{array}{ccc} V_{DD} = 30 \text{ V} & I_D = 1 \text{ A} \\ R_G = 4.7\Omega, & V_{GS} = 4.5 \text{ V} \\ \text{(Resistive Load, Figure 3)} \end{array}$		17 6		ns ns

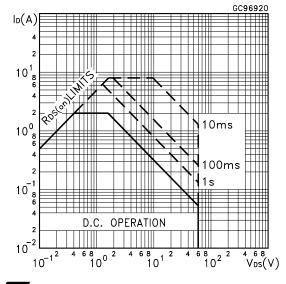
SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
I _{SDM} (•)	Source-drain Current Source-drain Current (pulsed)				2 8	A A
V _{SD} (*)	Forward On Voltage	I _{SD} = 2 A V _{GS} = 0			1.3	V
t _{rr} Q _{rr} I _{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 2 \text{ A}$ $di/dt = 100 \text{A}/\mu \text{s}$ $V_{DD} = 20 \text{ V}$ $T_j = 150 ^{\circ}\text{C}$ (see test circuit, Figure 5)		28 31 2.2		ns nC A

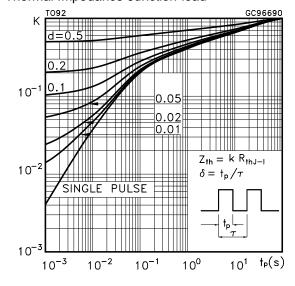
^(*)Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.

(•)Pulse width limited by safe operating area.

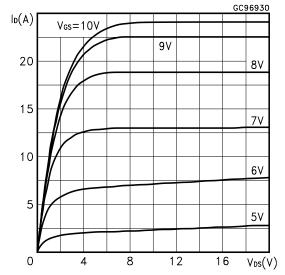
Safe Operating Area



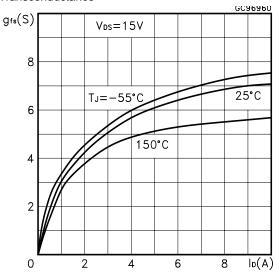
Thermal Impedance Junction-lead



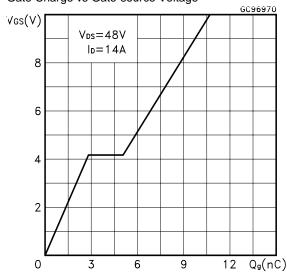
Output Characteristics



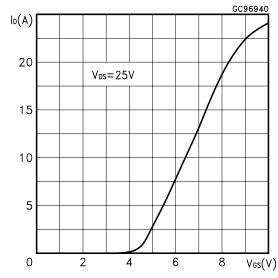
Transconductance



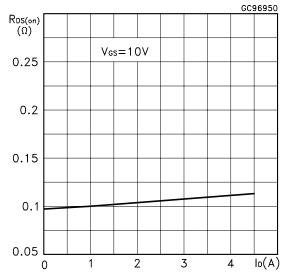
Gate Charge vs Gate-source Voltage



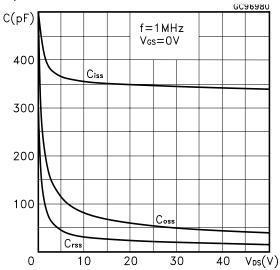
Transfer Characteristics



Static Drain-source On Resistance

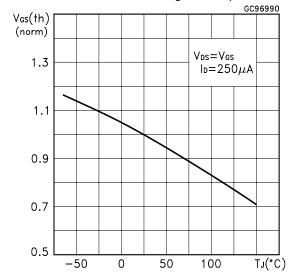


Capacitance Variations

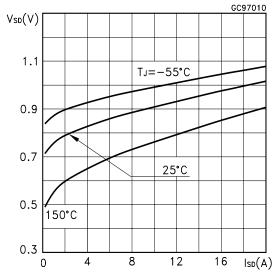


477

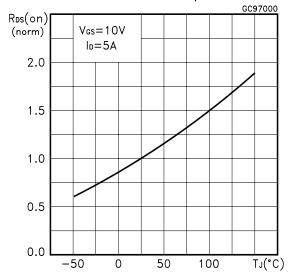
Normalized Gate Threshold Voltage vs Temperature



Source-drain Diode Forward Characteristics



Normalized on Resistance vs Temperature



Normalized Breakdown Voltage vs Temperature.

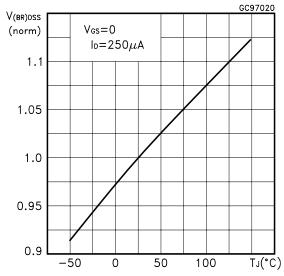


Fig. 1: Unclamped Inductive Load Test Circuit

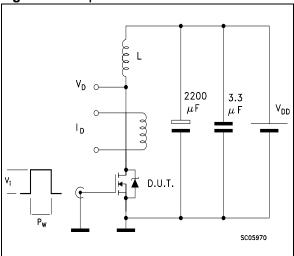


Fig. 3: Switching Times Test Circuits For Resistive Load

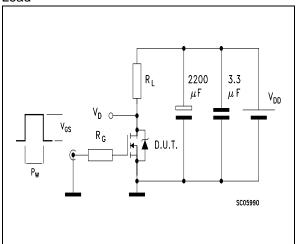


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times

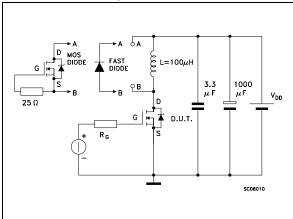


Fig. 2: Unclamped Inductive Waveform

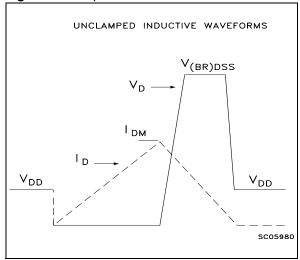
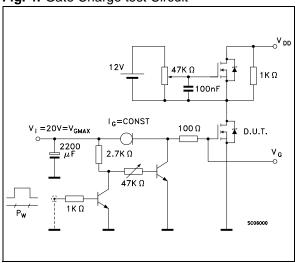
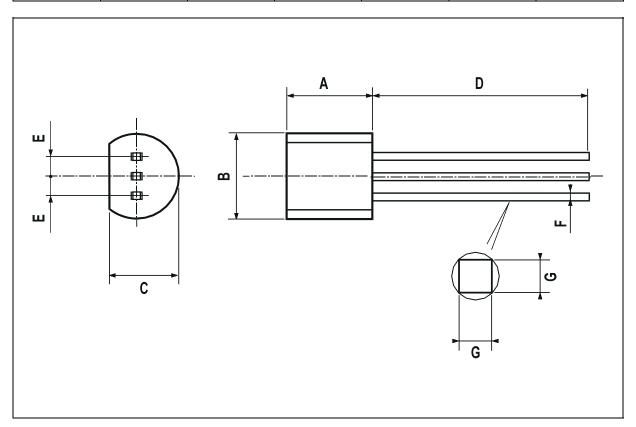


Fig. 4: Gate Charge test Circuit



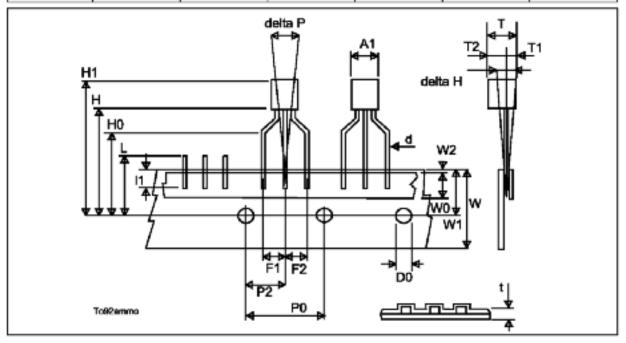
TO-92 MECHANICAL DATA

DIM.	mm				inch	
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
А	4.58		5.33	0.180		0.210
В	4.45		5.2	0.175		0.204
С	3.2		4.2	0.126		0.165
D	12.7			0.500		
E		1.27			0.050	
F	0.4		0.51	0.016		0.020
G	0.35			0.14		



TO-92 AMMOPACK

DIM.		mm.			inch	
DIM.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A1			4.8			0.19
Т			3.8			0.15
T1			1,6			0.06
T2			2.3			0.09
d			0.48			0.02
P0	12.5	12.7	12.9	0.49	0.5	0.51
P2	5.65	6.35	7.05	0.22	0.25	0.27
F1, F2	2.44	2.54	2.94	0.09	0.1	0.11
delta H	-2		2	-0.08		0.08
w	17.5	18	19	0.69	0.71	0.74
W0	5.7	6	6.3	0.22	0.23	0.24
W1	8.5	9	9.25	0.33	0.35	0.36
W2			0.5			0.02
Н	18.5		20.5	0.72		0.80
H0	15.5	16	16.5	0.61	0.63	0.65
H1			25			0.98
D0	3.8	4	4.2	0.15	0.157	0.16
t			0.9			0.035
L			11			0.43
l1	3			0.11		
delta P	-1		1	-0.04		0.04



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is registered trademark of STMicroelectronics All other names are the property of their respective owners.

® 2003 STMicroelectronics - All Rights Reserved

STMicroelectronics GROUP OF COMPANIES

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

www.st.com

