

8-bit Proprietary Microcontrollers

CMOS

F²MC-8FX MB95110A Series

MB95116A/F118AS/F118AW/FV100A-101

■ DESCRIPTION

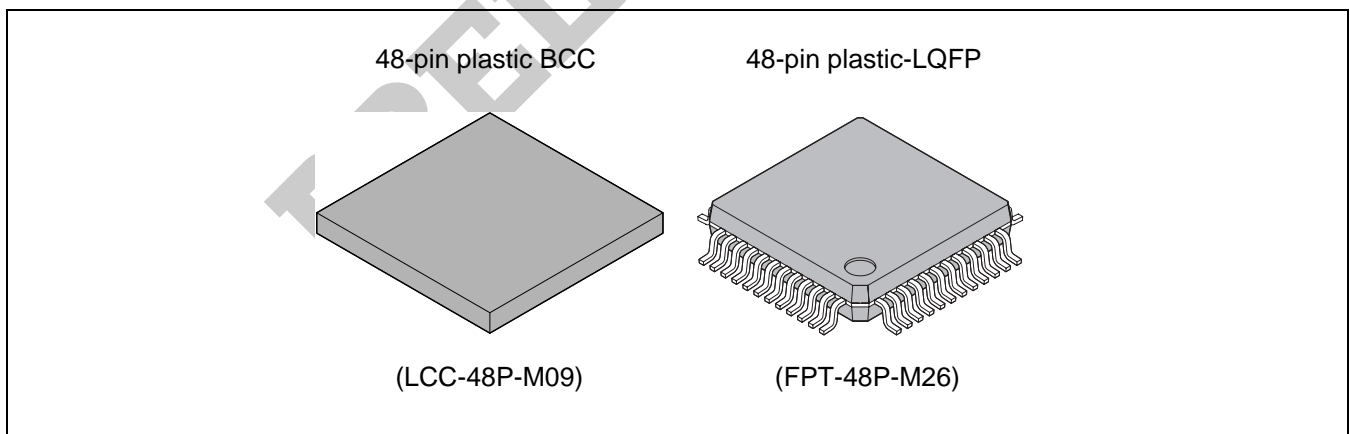
The MB95110A series is general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers contain a variety of peripheral functions.

■ FEATURES

- F²MC-8FX CPU core
Instruction set that is optimum to the controllers
 - Multiplication and division instructions
 - 16-bit arithmetic operation
 - Bit test branch instruction
 - Bit manipulation instructions etc.
- Clock
 - Main clock
 - Main PLL clock
 - Subclock (for dual clock product)
 - Sub PLL clock (for dual clock product)

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■ PACKAGES



MB95110A Series

(Continued)

- Timer
 - 8/16-bit compound timer × 2 channels
 - 8/16-bit PPG × 2 channels
 - 16-bit PPG
 - Timebase timer
 - Watch prescaler (for dual clock product)
- LIN-UART
 - Full duplex double buffer
 - Clock asynchronous or synchronous serial transfer capable
- UART/SIO
 - Clock asynchronous or synchronous serial transfer capable
- I²C*
 - Built-in wake-up function
- External interrupt
 - Interrupt by edge detection (rising, falling, or both edges can be selected)
 - Can be used to recover from low-power consumption modes.
- 10-bit A/D converter
 - 10-bit resolution
- Low-power consumption (standby mode)
 - Stop mode
 - Sleep mode
 - Watch mode (for dual clock product)
 - Timebase timer mode
- I/O port: Max 40
 - General-purpose I/O ports (Nch open drain) : 2 ports
 - General-purpose I/O ports (CMOS) : 38 ports

* : Purchase of Fujitsu I²C components conveys a license under the Philips I²C Patent Rights to use, these components in an I²C system provided that the system conforms to the I²C Standard Specification as defined by Philips.

MB95110A Series

■ PRODUCT LINEUP

| Part number | | MB95116A | MB95F118AS | MB95F118AW | MB95FV100A-101 |
|----------------------|--------------------------------------|--|---------------|-------------|----------------------------------|
| Parameter | | | | | |
| Type | | MASK product | FLASH product | | EVA product |
| ROM capacity | | 32 Kbytes | 60 Kbytes | | |
| RAM capacity | | 1 Kbytes | 2 Kbytes | | 3.75 Kbytes |
| Reset output | | No | | | |
| Option | | Selectable single/dual -system*2 | Single-system | Dual-system | Selectable single/dual -system*1 |
| CPU functions | | Number of basic instructions : 136 Instruction bit length : 8 bits Instruction length : 1 to 3 bytes Data bit length : 1, 8, and 16 bits Minimum instruction execution time : 0.1 μ s (at internal 10 MHz) Interrupt processing time : 0.9 μ s (at internal 10 MHz) | | | |
| Peripheral functions | Ports (Max 40 ports) | General-purpose I/O port (Nch open drain) : 2 ports General-purpose I/O port (CMOS) : 38 ports | | | |
| | Timebase timer | Interrupt cycle : 0.5 ms, 2.05 ms, 8.2 ms, 32.8 ms (at main oscillation clock 4 MHz) | | | |
| | Watchdog timer | Reset generated cycle At main oscillation clock 10 MHz : Minimum 105 ms At sub oscillation clock 32.768 kHz (for dual clock product) : Minimum 250 ms | | | |
| | Wild register | Capable of replacing 3 bytes of data | | | |
| | I ² C bus | Master/slave sending and receiving Bus error function and arbitration function Detecting transmitting direction function Start condition repeated generation and detection functions Built-in wake-up function | | | |
| | UART/SIO | Data transfer capable in UART/SIO Full duplex double buffer, variable data length (5/6/7/8-bit), built-in baud rate generator Transfer rate : 2400 bps to 125000 bps (at machine clock 10 MHz) NRZ type transfer format, error detected function LSB-first or MSB-first can be selected. Clock synchronous (SIO) or clock asynchronous (UART) data transfer capable | | | |
| | LIN-UART | Dedicated reload timer allowing a wide range of communication speeds to be set. Capable of data transfer synchronous or asynchronous to clock signal. LIN functions available as the LIN master or LIN slave. | | | |
| | A/D converter (8 channels) | 8-bit or 10-bit resolution can be selected. | | | |
| | 8/16-bit compound timer (2 channels) | Each channel of the timer can be used as "8-bit timer \times 2 channels" or "16-bit timer \times 1 channel". Built-in timer function, PWC function, PWM function, capture function and square waveform output Count clock : 7 internal clocks and external clock can be selected. | | | |

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MB95110A Series

(Continued)

| Part number | | MB95116A | MB95F118AS | MB95F118AW | MB95FV100A-101 |
|----------------------|---|--|------------|------------|----------------|
| Parameter | | | | | |
| Peripheral functions | 16-bit PPG | PWM mode or one-shot mode can be selected. Counter operating clock : Eight selectable clock sources Support for external trigger start | | | |
| | 8/16-bit PPG (2 channels) | Each channel of the PPG can be used as "8-bit PPG × 2 channels" or "16-bit PPG × 1 channel". Counter operating clock : Eight selectable clock sources | | | |
| | Watch counter (for dual clock product) | Count clock : Four selectable clock sources (125ms, 250ms, 500ms, or 1s) Counter value can be set from 0 to 63. (Capable of counting for 1 minute) | | | |
| | Watch prescaler (for dual clock product) | Four selectable interval times (125 ms, 250 ms, 500 ms, or 1 s) | | | |
| | External interrupt (8 channels) | Interrupt by edge detection (rising, falling, or both edges can be selected) Can be used to recover from standby modes. | | | |
| Standby mode | | Sleep, stop, watch, and timebase timer | | | |

*1 : Change by the switch on MCU board.

*2 : Specify clock mode when ordering MASK ROM.

■ SELECT OF OSCILLATION STABILIZATION WAIT TIME (MASK PRODUCT ONLY)

For the MASK product, you can set the mask option when ordering MASK ROM to select the initial value of main clock oscillation stabilization wait time from among the following four values.

Note that the EVA and FLASH products are fixed their initial value of main clock oscillation stabilization wait time at the maximum value.

| Selection of oscillation stabilization wait time | Remarks |
|--|---|
| $(2^2 - 2) / F_{CH}$ | 0.5 μ s (at main oscillation clock 4 MHz) |
| $(2^{12} - 2) / F_{CH}$ | Approx. 1.02 ms (at main oscillation clock 4 MHz) |
| $(2^{13} - 2) / F_{CH}$ | Approx. 2.05 ms (at main oscillation clock 4 MHz) |
| $(2^{14} - 2) / F_{CH}$ | Approx. 4.10 ms (at main oscillation clock 4 MHz) |

■ PACKAGES AND CORRESPONDING PRODUCTS

| Part number Package | MB95116A | MB95F118AS | MB95F118AW | MB95FV100A-101 |
|------------------------|----------|------------|------------|----------------|
| LCC-48P-M09 | ○ | ○ | ○ | × |
| FPT-48P-M26 | ○ | ○ | ○ | × |
| BGA-224P-M08 | × | × | × | ○ |

- : Available
- × : Unavailable

MB95110A Series

■ DIFFERENCES AMONG PRODUCTS AND NOTES ON SELECTING PRODUCTS

• Notes on Using EVA Products

The EVA product has not only the functions of the MB95110A series but also those of other products to support software development for multiple series and products of F²MC-8FX family. The I/O addresses for peripheral resources not used by the MB95110A series are therefore access-barred. Read/write access to these access-barred addresses may cause peripheral resources supposed to be unused to operate, resulting in unexpected malfunctions of hardware or software.

Take particular care not to use word, long word, or similar access to read or write odd numbered bytes in the prohibited areas.

Note that the values read from barred addresses are different between the EVA product and the FLASH or MASK product. Therefore, the data must not be used for software processing.

The EVA product does not support the functions of some bits in single-byte registers. Read/write access to these bits does not cause hardware malfunctions. Since the EVA, FLASH, and MASK products are designed to behave completely the same way in terms of hardware and software, you do not have to pay special attention to specific products.

• Difference of Memory Spaces

If the amount of memory on the EVA product is different from that of the FLASH or MASK product, carefully check the difference in the amount of memory from the product to be actually used when developing software.

• Current Consumption

- The current consumption of FLASH product is typically greater than for MASK product.
- For details of current consumption, refer to “■ ELECTRICAL CHARACTERISTICS”.

• Package

For details of information on each package, see “■ PACKAGE DIMENSIONS”.

• Operating voltage

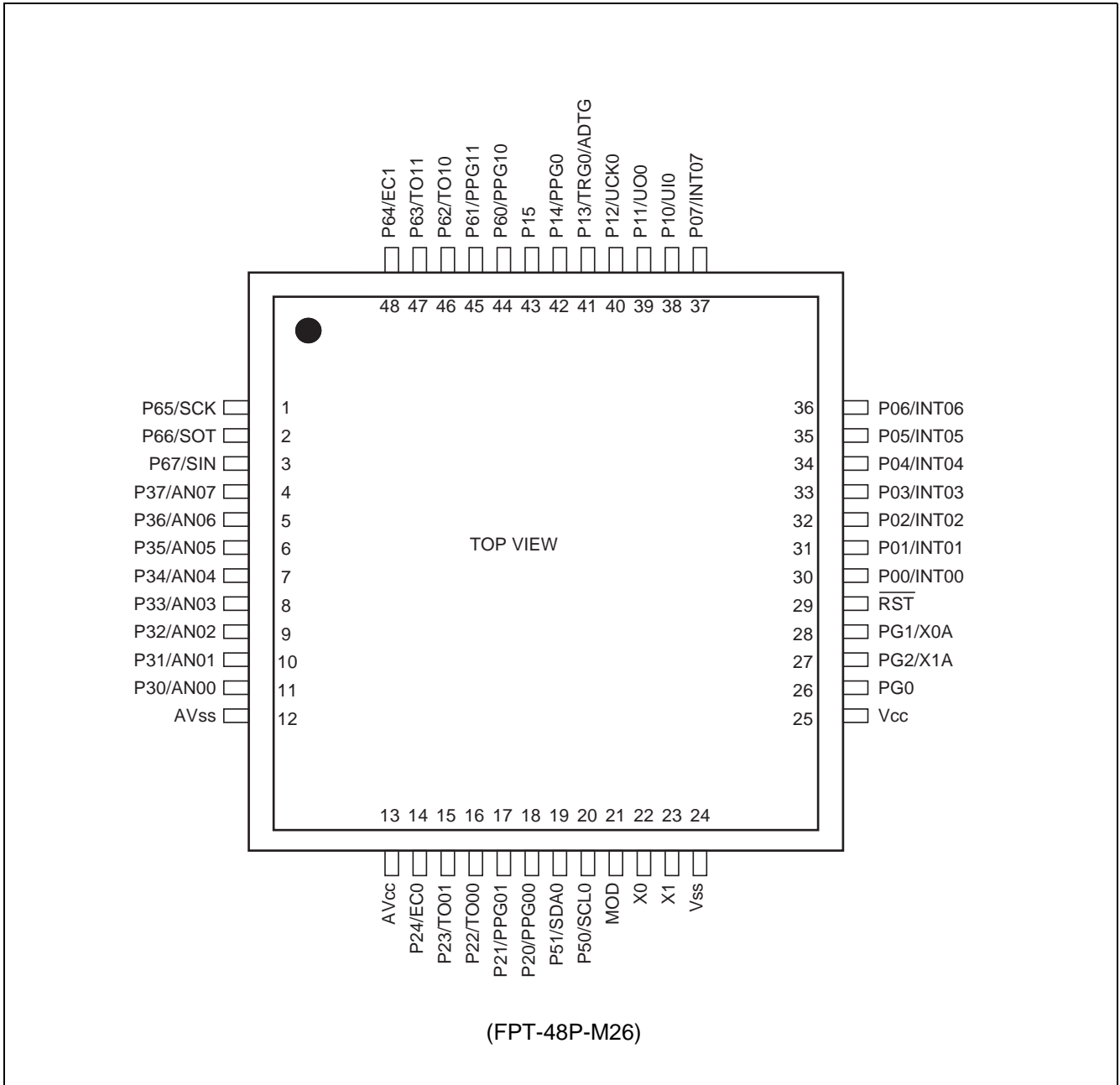
The operating voltage are different among the EVA, FLASH and MASK products.

For details of operating voltage, refer to “■ ELECTRICAL CHARACTERISTICS”

• Difference between $\overline{\text{RST}}$ and MOD pins

The $\overline{\text{RST}}$ and MOD pins are hysteresis inputs on the MASK product. A pull-down resistor is provided for the MOD pin of the MASK product.

MB95110A Series



■ PIN DESCRIPTION

| Pin no. | Pin name | Circuit type | Description |
|---------|-------------------------|--------------|--|
| 1 | P65/SCK | K | General-purpose I/O port. The pin is shared with LIN-UART clock I/O. |
| 2 | P66/SOT | | General-purpose I/O port. The pin is shared with LIN-UART data output. |
| 3 | P67/SIN | L | General-purpose I/O port. The pin is shared with LIN-UART data input. |
| 4 | P37/AN07 | J | General-purpose I/O port. The pins are shared with A/D analog input. |
| 5 | P36/AN06 | | |
| 6 | P35/AN05 | | |
| 7 | P34/AN04 | | |
| 8 | P33/AN03 | | |
| 9 | P32/AN02 | | |
| 10 | P31/AN01 | | |
| 11 | P30/AN00 | | |
| 12 | AVss | — | A/D power supply pin (GND) |
| 13 | AVcc | — | A/D power supply pin |
| 14 | P24/EC0 | H | General-purpose I/O port. The pin is shared with 8/16-bit compound timer ch0 clock input. |
| 15 | P23/TO01 | | General-purpose I/O port. The pins are shared with 8/16-bit compound timer ch0 output. |
| 16 | P22/TO00 | | |
| 17 | P21/PPG01 | | |
| 18 | P20/PPG00 | | |
| 19 | P51/SDA0 | I | General-purpose I/O port. The pin is shared with I ² C ch0 data I/O. |
| 20 | P50/SCL0 | | General-purpose I/O port. The pin is shared with I ² C ch0 clock I/O. |
| 21 | MOD | B | Operating mode designation pin |
| 22 | X0 | A | Crystal oscillation pin |
| 23 | X1 | | |
| 24 | Vss | — | Power supply pin (GND) |
| 25 | Vcc | — | Power supply pin |
| 26 | PG0 | H | General-purpose I/O port. |
| 27 | PG2/X1A | H/A | Single-system product is general-purpose port. Dual-system product is Crystal oscillation pin (32 kHz). |
| 28 | PG1/X0A | | |
| 29 | $\overline{\text{RST}}$ | B' | Reset pin |

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MB95110A Series

(Continued)

| Pin no. | Pin name | Circuit type | Description | |
|---------|-------------------|--------------|---|---|
| 30 | P00/INT00 | C | General-purpose I/O port. The pins are shared with external interrupt input. Large current port. | |
| 31 | P01/INT01 | | | |
| 32 | P02/INT02 | | | |
| 33 | P03/INT03 | | | |
| 34 | P04/INT04 | | | |
| 35 | P05/INT05 | | | |
| 36 | P06/INT06 | | | |
| 37 | P07/INT07 | | | |
| 38 | P10/UI0 | G | General-purpose I/O port. The pin is shared with UART/SIO ch0 data input. | |
| 39 | P11/UO0 | H | General-purpose I/O port. The pin is shared with UART/SIO ch0 data output. | |
| 40 | P12/UCK0 | | General-purpose I/O port. The pin is shared with UART/SIO ch0 clock I/O. | |
| 41 | P13/TRG0/ ADTG | | General-purpose I/O port. The pin is shared with 16-bit PPG ch0 trigger input (TRG0) and A/D trigger input (ADTG). | |
| 42 | P14/PPG0 | | General-purpose I/O port. The pin is shared with 16-bit PPG ch0 output. | |
| 43 | P15 | | General-purpose I/O port. | |
| 44 | P60/PPG10 | | K | General-purpose I/O port. The pins are shared with 8/16-bit PPG ch1 output. |
| 45 | P61/PPG11 | K | | |
| 46 | P62/TO10 | | | General-purpose I/O port. The pins are shared with 8/16-bit compound timer ch1 output. |
| 47 | P63/TO11 | | | K |
| 48 | P64/EC1 | | | |

■ I/O CIRCUIT TYPE

| Type | Circuit | Remarks |
|------|---------|---|
| A | | <ul style="list-style-type: none"> • Oscillation circuit • High-speed side Feedback resistance value : approx. 1 MΩ • Low-speed side Feedback resistance : approx. 24 MΩ (EVA product : approx. 10 MΩ) • Dumping resistance : approx. 144 kΩ (EVA product : without dumping resistance) |
| B | | <ul style="list-style-type: none"> • Only for input • Hysteresis input only for MASK product • With pull-down resistor only for MASK product |
| B' | | <ul style="list-style-type: none"> • Hysteresis input only for MASK product |
| C | | <ul style="list-style-type: none"> • CMOS output • Hysteresis input |
| G | | <ul style="list-style-type: none"> • CMOS output • CMOS input • Hysteresis input • With pull-up control |

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MB95110A Series

(Continued)

| Type | Circuit | Remarks |
|------|---------|---|
| H | | <ul style="list-style-type: none"> • CMOS output • Hysteresis input • With pull-up control |
| I | | <ul style="list-style-type: none"> • Nch open drain output • CMOS input • Hysteresis input |
| J | | <ul style="list-style-type: none"> • CMOS output • Hysteresis input • Analog input • With pull-up control |
| K | | <ul style="list-style-type: none"> • CMOS output • Hysteresis input |
| L | | <ul style="list-style-type: none"> • CMOS output • CMOS input • Hysteresis input |

■ HANDLING DEVICES

• Preventing Latchup

Care must be taken to ensure that maximum voltage ratings are not exceeded when it is used.

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- and high-withstand voltage pins or if higher than the rating voltage is applied between V_{CC} and V_{SS} .

When latchup occurs, power supply current increases rapidly and might thermally damage elements.

Also, take care to prevent the analog power supply voltage (AV_{CC}) and analog input voltage from exceeding the digital power supply voltage (V_{CC}) when the analog system power supply is turned on or off.

• Stable Supply Voltage

Supply voltage should be stabilized.

A sudden change in power-supply voltage may cause a malfunction even within the guaranteed operating range of the V_{CC} power-supply voltage.

For stabilization, in principle, keep the variation in V_{CC} ripple (p-p value) in a commercial frequency range (50 Hz to 60 Hz) not to exceed 10% of the V_{CC} value and suppress the voltage variation so that the transient variation rate does not exceed 0.1 V/ms during a momentary change such as when the power supply is switched.

• Treatment of Unused Input Pin

An unused input pin may cause a malfunction if it is left open. It should be connected to a pull-up or pull-down resistor.

• Treatment of Power Supply Pins on A/D Converter

Connect to be $AV_{CC} = V_{CC}$ and $AV_{SS} = V_{SS}$ even if the A/D converter is not in use.

• Precautions for Use of External Clock

Even when an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from subclock mode or stop mode.

• Precaution against Noise to the External Reset Pin (\overline{RST})

An input of a reset pulse below the specified level to the external reset pin (\overline{RST}) may cause malfunctions. Be sure not to allow an input of a reset pulse below the specified level to the external reset pin (\overline{RST}).

MB95110A Series

■ PROGRAMMING FLASH MICROCONTROLLERS USING PARALLEL PROGRAMMER

• Supported Parallel Programmers and Adapters

The following table lists supported parallel programmers and adapters.

| Package | Applicable adapter model | Parallel programmers |
|-------------|--------------------------|--|
| FPT-48P-M26 | TEF110-108F37AP | AF9708 (Ver 02.35G or more) AF9709/B (Ver 02.35G or more) |
| LCC-48P-M09 | TEF100-108F41AP | AF9723+AF9834 (Ver 02.08E or more) |

Notes: • Set all of the J1 to J3 switches on the adapter to "95F108".

- For information on applicable adapter models and parallel programmers, contact the following:
Flash Support Group, Inc. TEL: 053-428-8380

• Sector Configuration

The individual sectors of flash memory correspond to addresses used for CPU access and programming by the parallel programmer as follows:

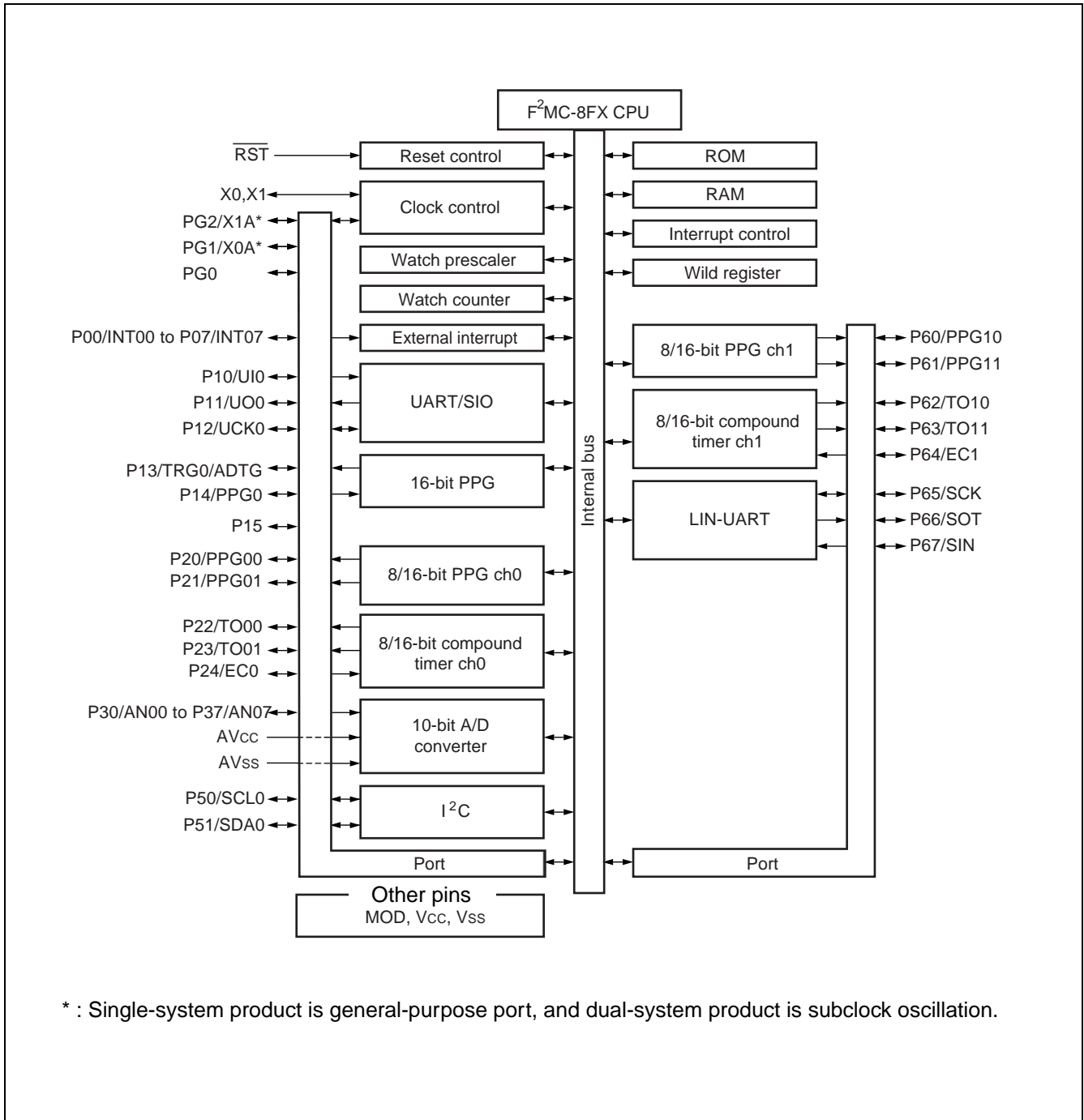
| Flash memory | CPU address | Writer address* |
|-----------------|-------------------|--------------------|
| SA1 (4 Kbytes) | 1000 _H | 71000 _H |
| SA2 (4 Kbytes) | 1FFF _H | 71FFF _H |
| | 2000 _H | 72000 _H |
| SA3 (4 Kbytes) | 2FFF _H | 72FFF _H |
| | 3000 _H | 73000 _H |
| SA4 (16 Kbytes) | 3FFF _H | 73FFF _H |
| | 4000 _H | 74000 _H |
| SA5 (16 Kbytes) | 7FFF _H | 77FFF _H |
| | 8000 _H | 78000 _H |
| SA6 (4 Kbytes) | BFFF _H | 7BFFF _H |
| | C000 _H | 7C000 _H |
| SA7 (4 Kbytes) | CFFF _H | 7CFFF _H |
| | D000 _H | 7D000 _H |
| SA8 (4 Kbytes) | DFFF _H | 7DFFF _H |
| | E000 _H | 7E000 _H |
| SA9 (4 Kbytes) | EFFF _H | 7EFFF _H |
| | F000 _H | 7F000 _H |
| | FFF _H | 7FFF _H |

*: Programmer addresses are equivalent to CPU addresses, used when the parallel programmer programs data into flash memory.
These programmer addresses are used for the parallel programmer to program or erase data in flash memory.

• Programming Method

- 1) Set the type code of the parallel programmer to 17226.
- 2) Load program data to programmer addresses 71000_H to 7FFFF_H.
- 3) Programmed by parallel programmer

■ BLOCK DIAGRAM



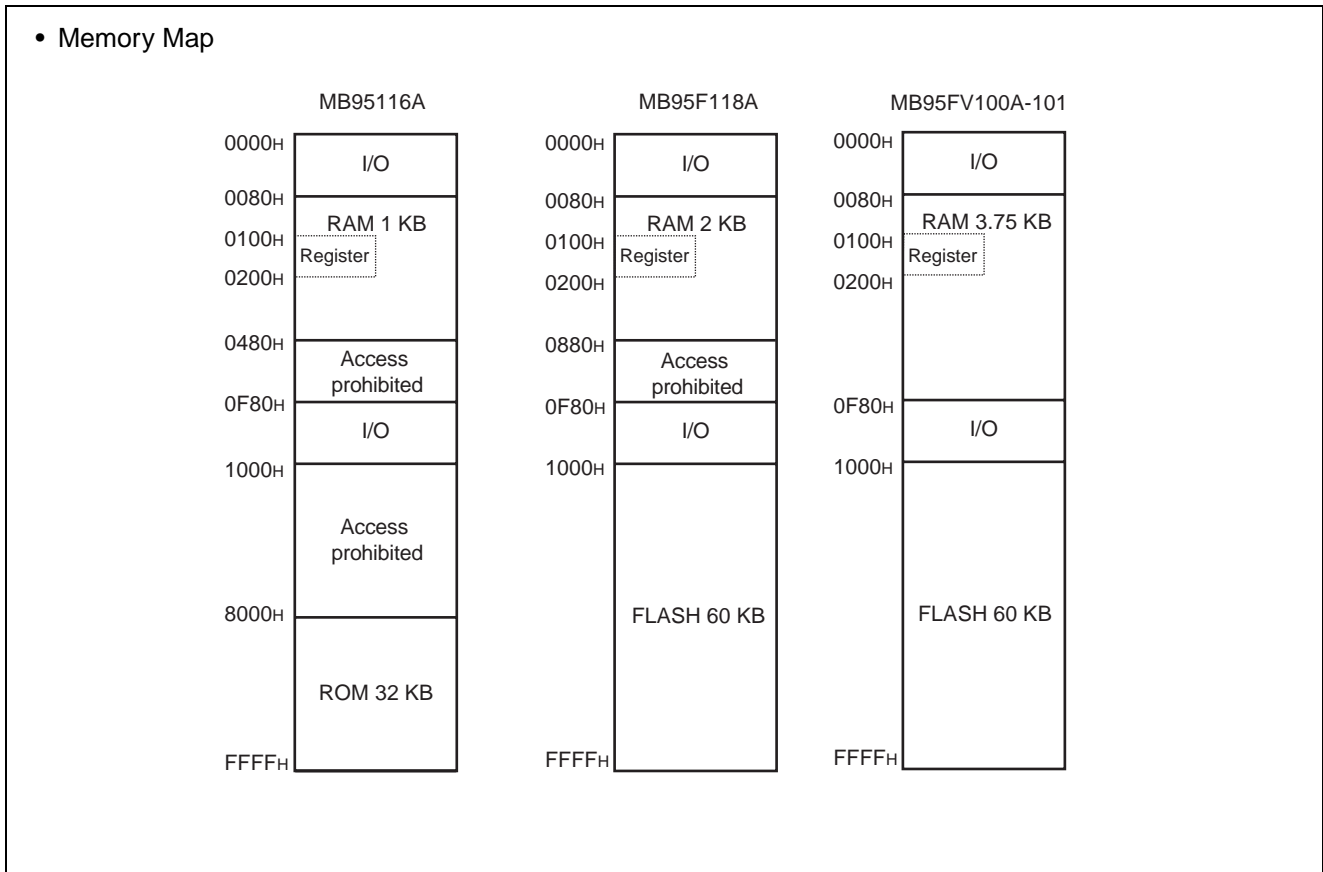
* : Single-system product is general-purpose port, and dual-system product is subclock oscillation.

MB95110A Series

■ CPU CORE

1. Memory space

Memory space of the MB95110A series is 64 Kbytes and consists of I/O area, data area, and program area. The memory space includes special-purpose areas such as the general-purpose registers and vector table. Memory map of the MB95110A series shown in below.



2. Register

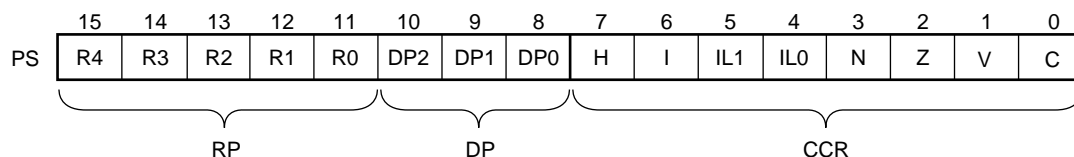
The MB95110A series has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The dedicated registers are as follows:

- Program counter (PC) : A 16-bit register to indicate locations where instructions are stored.
- Accumulator (A) : A 16-bit register for temporary storage of arithmetic operations. In the case of an 8-bit data processing instruction, the lower one byte is used.
- Temporary accumulator (T) : A 16-bit register which performs arithmetic operations with the accumulator. In the case of an 8-bit data processing instruction, the lower one byte is used.
- Index register (IX) : A 16-bit register for index modification
- Extra pointer (EP) : A 16-bit pointer to point to a memory address.
- Stack pointer (SP) : A 16-bit register to indicate a stack area.
- Program status (PS) : A 16-bit register for storing a register bank pointer, a direct bank pointer, and a condition code register

| 16-bit | | Initial Value |
|--------|-------------------------|-------------------|
| PC | : Program counter | FFFD _H |
| A | : Accumulator | 0000 _H |
| T | : Temporary accumulator | 0000 _H |
| IX | : Index register | 0000 _H |
| EP | : Extra pointer | 0000 _H |
| SP | : Stack pointer | 0000 _H |
| PS | : Program status | 0030 _H |

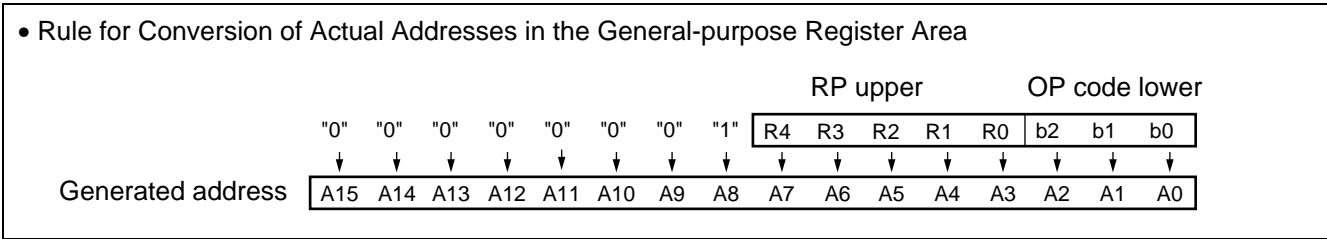
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and a direct bank pointer (DP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

- Structure of the program status



MB95110A Series

The RP indicates the address of the register bank currently being used. The relationship between the content of RP and the real address conforms to the conversion rule illustrated below:



The DP specifies the area for mapping instructions (16 different instructions such as MOV A, dir) using direct addresses to 0080H to 00FFH.

| Direct bank pointer (DP2 to DP0) | Specified address area | Mapping area |
|----------------------------------|------------------------|----------------------------------|
| Don't care | 0000H to 007FH | 0000H to 007FH (without mapping) |
| 000B (initial value) | 0080H to 00FFH | 0080H to 00FFH (without mapping) |
| 001B | | 0100H to 017FH |
| 010B | | 0180H to 01FFH |
| 011B | | 0200H to 027FH |
| 100B | | 0280H to 02FFH |
| 101B | | 0300H to 037FH |
| 110B | | 0380H to 03FFH |
| 111B | | 0400H to 047FH |

The CCR consists of the bits indicating arithmetic operation results or transfer data contents and the bits that control CPU operations at interrupt.

- H flag : Set to "1" when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared to "0" otherwise. This flag is for decimal adjustment instructions.
- I flag : Interrupt is enabled when this flag is set to "1". Interrupt is disabled when this flag is set to "0". The flag is set to "0" when reset.
- IL1, IL0 : Indicates the level of the interrupt currently enabled. Processes an interrupt only if its request level is higher than the value indicated by this bit.

| IL1 | IL0 | Interrupt level | Priority |
|-----|-----|-----------------|---|
| 0 | 0 | 0 | High ↑ ↓ Low = no interruption |
| 0 | 1 | 1 | |
| 1 | 0 | 2 | |
| 1 | 1 | 3 | |

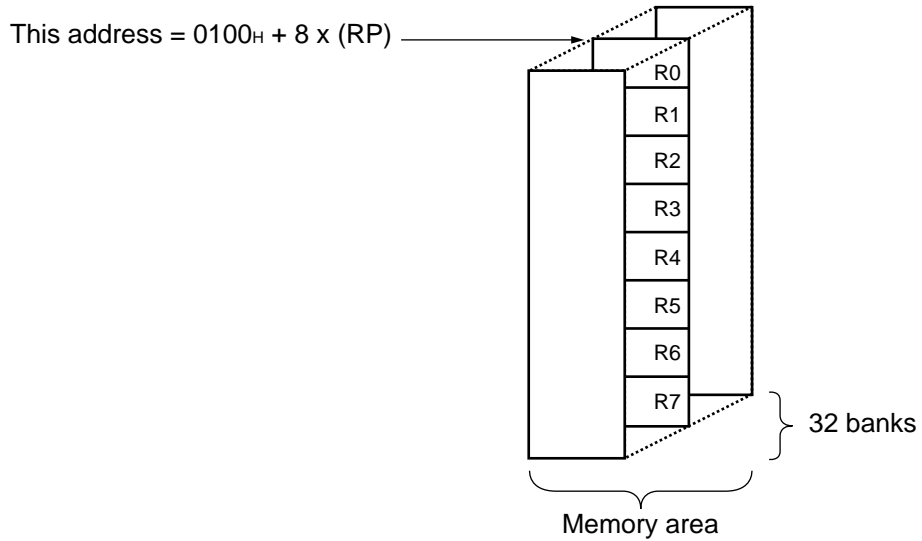
- N flag : Set to "1" if the MSB is set to "1" as the result of an arithmetic operation. Cleared to "0" when the bit is set to "0".
- Z flag : Set to "1" when an arithmetic operation results in 0. Cleared to "0" otherwise.
- V flag : Set to "1" if the complement on 2 overflows as a result of an arithmetic operation. Cleared to "0" otherwise.
- C flag : Set to "1" when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to "0" otherwise. Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided:

General-purpose registers: 8-bit data storage registers

The general-purpose registers are 8 bits and located in the register banks on the memory. One bank contains eight registers. Up to a total of 32 banks can be used on the MB95110A series. The bank currently in use is indicated by the register bank pointer (RP).

- Register Bank Configuration



MB95110A Series

■ I/O MAP

| Address | Register abbreviation | Register name | R/W | Initial value |
|--|-----------------------|--|-----|-----------------------|
| 0000 _H | PDR0 | Port 0 data register | R/W | 00000000 _B |
| 0001 _H | DDR0 | Port 0 direction register | R/W | 00000000 _B |
| 0002 _H | PDR1 | Port 1 data register | R/W | 00000000 _B |
| 0003 _H | DDR1 | Port 1 direction register | R/W | 00000000 _B |
| 0004 _H | — | (Vacancy) | — | — |
| 0005 _H | WATR | Oscillation stabilization wait time setting register | R/W | 11111111 _B |
| 0006 _H | PLL0 | PLL control register | R/W | 00000000 _B |
| 0007 _H | SYCC | System clock control register | R/W | 1010X011 _B |
| 0008 _H | STBC | Standby control register | R/W | 00000000 _B |
| 0009 _H | RSRR | Reset source register | R | XXXXXXXX _B |
| 000A _H | TBTC | Timebase timer control register | R/W | 00000000 _B |
| 000B _H | WPCR | Watch prescaler control register | R/W | 00000000 _B |
| 000C _H | WDTC | Watchdog timer control register | R/W | 00000000 _B |
| 000D _H | — | (Vacancy) | — | — |
| 000E _H | PDR2 | Port 2 data register | R/W | 00000000 _B |
| 000F _H | DDR2 | Port 2 direction register | R/W | 00000000 _B |
| 0010 _H | PDR3 | Port 3 data register | R/W | 00000000 _B |
| 0011 _H | DDR3 | Port 3 direction register | R/W | 00000000 _B |
| 0012 _H | — | (Vacancy) | — | — |
| 0013 _H | | | | |
| 0014 _H | PDR5 | Port 5 data register | R/W | 00000000 _B |
| 0015 _H | DDR5 | Port 5 direction register | R/W | 00000000 _B |
| 0016 _H | PDR6 | Port 6 data register | R/W | 00000000 _B |
| 0017 _H | DDR6 | Port 6 direction register | R/W | 00000000 _B |
| 0018 _H to 0029 _H | — | (Vacancy) | — | — |
| 002A _H | PDRG | Port G data register | R/W | 00000000 _B |
| 002B _H | DDRG | Port G direction register | R/W | 00000000 _B |
| 002C _H | — | (Vacancy) | — | — |
| 002D _H | PUL1 | Port 1 pull-up register | R/W | 00000000 _B |
| 002E _H | PUL2 | Port 2 pull-up register | R/W | 00000000 _B |
| 002F _H | PUL3 | Port 3 pull-up register | R/W | 00000000 _B |
| 0030 _H to 0034 _H | — | (Vacancy) | — | — |

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MB95110A Series

| Address | Register abbreviation | Register name | R/W | Initial value |
|--|-----------------------|--|-----|-----------------------|
| 0035 _H | PULG | Port G pull-up register | R/W | 00000000 _B |
| 0036 _H | T01CR1 | 8/16-bit compound timer 01 control status register 1 ch0 | R/W | 00000000 _B |
| 0037 _H | T00CR1 | 8/16-bit compound timer 00 control status register 1 ch0 | R/W | 00000000 _B |
| 0038 _H | T11CR1 | 8/16-bit compound timer 11 control status register 1 ch1 | R/W | 00000000 _B |
| 0039 _H | T10CR1 | 8/16-bit compound timer 10 control status register 1 ch1 | R/W | 00000000 _B |
| 003A _H | PC01 | 8/16-bit PPG1 control register ch0 | R/W | 00000000 _B |
| 003B _H | PC00 | 8/16-bit PPG0 control register ch0 | R/W | 00000000 _B |
| 003C _H | PC11 | 8/16-bit PPG1 control register ch1 | R/W | 00000000 _B |
| 003D _H | PC10 | 8/16-bit PPG0 control register ch1 | R/W | 00000000 _B |
| 003E _H to 0041 _H | — | (Vacancy) | — | — |
| 0042 _H | PCNTH0 | 16-bit PPG status control register (Upper byte) ch0 | R/W | 00000000 _B |
| 0043 _H | PCNTL0 | 16-bit PPG status control register (Lower byte) ch0 | R/W | 00000000 _B |
| 0044 _H to 0047 _H | — | (Vacancy) | — | — |
| 0048 _H | EIC00 | External interrupt circuit control register ch0/1 | R/W | 00000000 _B |
| 0049 _H | EIC10 | External interrupt circuit control register ch2/3 | R/W | 00000000 _B |
| 004A _H | EIC20 | External interrupt circuit control register ch4/5 | R/W | 00000000 _B |
| 004B _H | EIC30 | External interrupt circuit control register ch6/7 | R/W | 00000000 _B |
| 004C _H to 004F _H | — | (Vacancy) | — | — |
| 0050 _H | SCR | LIN-UART serial control register | R/W | 00000000 _B |
| 0051 _H | SMR | LIN-UART serial mode register | R/W | 00000000 _B |
| 0052 _H | SSR | LIN-UART serial status register | R/W | 00001000 _B |
| 0053 _H | RDR/TDR | LIN-UART reception/transmission data register | R/W | 00000000 _B |
| 0054 _H | ESCR | LIN-UART extended status control register | R/W | 00000100 _B |
| 0055 _H | ECCR | LIN-UART extended communication control register | R/W | 000000XX _B |
| 0056 _H | SMC10 | UART/SIO serial mode control register 1 ch0 | R/W | 00000000 _B |
| 0057 _H | SMC20 | UART/SIO serial mode control register 2 ch0 | R/W | 00100000 _B |
| 0058 _H | SSR0 | UART/SIO serial status register ch0 | R/W | 00000001 _B |
| 0059 _H | TDR0 | UART/SIO serial output data register ch0 | R/W | 00000000 _B |
| 005A _H | RDR0 | UART/SIO serial input data register ch0 | R | 00000000 _B |
| 005B _H to 005F _H | — | (Vacancy) | — | — |

(Continued)

MB95110A Series

| Address | Register abbreviation | Register name | R/W | Initial value |
|--|-----------------------|--|-----|-----------------------|
| 0060 _H | IBCR00 | I ² C bus control register 0 ch0 | R/W | 00000000 _B |
| 0061 _H | IBCR10 | I ² C bus control register 1 ch0 | R/W | 00000000 _B |
| 0062 _H | IBSR0 | I ² C bus status register ch0 | R | 00000000 _B |
| 0063 _H | IDDR0 | I ² C data register ch0 | R/W | 00000000 _B |
| 0064 _H | IAAR0 | I ² C address register ch0 | R/W | 00000000 _B |
| 0065 _H | ICCR0 | I ² C clock control register ch0 | R/W | 00000000 _B |
| 0066 _H to 006B _H | — | (Vacancy) | — | — |
| 006C _H | ADC1 | A/D control register 1 | R/W | 00000000 _B |
| 006D _H | ADC2 | A/D control register 2 | R/W | 00000000 _B |
| 006E _H | ADDH | A/D data register (Upper byte) | R/W | 00000000 _B |
| 006F _H | ADDL | A/D data register (Lower byte) | R/W | 00000000 _B |
| 0070 _H | WCSR | Watch counter status register | R/W | 00000000 _B |
| 0071 _H | — | (Vacancy) | — | — |
| 0072 _H | FSR | Flash memory status register | R/W | 000X0000 _B |
| 0073 _H | SWRE0 | Flash memory sector writing control register 0 | R/W | 00000000 _B |
| 0074 _H | SWRE1 | Flash memory sector writing control register 1 | R/W | 00000000 _B |
| 0075 _H | — | (Vacancy) | — | — |
| 0076 _H | WREN | Wild register address compare enable register | R/W | 00000000 _B |
| 0077 _H | WROR | Wild register data test setting register | R/W | 00000000 _B |
| 0078 _H | — | (Mirror of register bank pointer (RP) and direct bank pointer (DP)) | — | — |
| 0079 _H | ILR0 | Interrupt level setting register 0 | R/W | 11111111 _B |
| 007A _H | ILR1 | Interrupt level setting register 1 | R/W | 11111111 _B |
| 007B _H | ILR2 | Interrupt level setting register 2 | R/W | 11111111 _B |
| 007C _H | ILR3 | Interrupt level setting register 3 | R/W | 11111111 _B |
| 007D _H | ILR4 | Interrupt level setting register 4 | R/W | 11111111 _B |
| 007E _H | ILR5 | Interrupt level setting register 5 | R/W | 11111111 _B |
| 007F _H | — | (Vacancy) | — | — |
| 0F80 _H | WRARH0 | Wild register address setting register (Upper byte) ch0 | R/W | 00000000 _B |
| 0F81 _H | WRARL0 | Wild register address setting register (Lower byte) ch0 | R/W | 00000000 _B |
| 0F82 _H | WRDR0 | Wild register data setting register ch0 | R/W | 00000000 _B |
| 0F83 _H | WRARH1 | Wild register address setting register (Upper byte) ch1 | R/W | 00000000 _B |
| 0F84 _H | WRARL1 | Wild register address setting register (Lower byte) ch1 | R/W | 00000000 _B |
| 0F85 _H | WRDR1 | Wild register data setting register ch1 | R/W | 00000000 _B |

(Continued)

MB95110A Series

| Address | Register abbreviation | Register name | R/W | Initial value |
|--|-----------------------|---|-----|-----------------------|
| 0F86 _H | WRARH2 | Wild register address setting register (Upper byte) ch2 | R/W | 00000000 _B |
| 0F87 _H | WRARL2 | Wild register address setting register (Lower byte) ch2 | R/W | 00000000 _B |
| 0F88 _H | WRDR2 | Wild register data setting register ch2 | R/W | 00000000 _B |
| 0F89 _H to 0F91 _H | — | (Vacancy) | — | — |
| 0F92 _H | T01CR0 | 8/16-bit compound timer 01 control status register 0 ch0 | R/W | 00000000 _B |
| 0F93 _H | T00CR0 | 8/16-bit compound timer 00 control status register 0 ch0 | R/W | 00000000 _B |
| 0F94 _H | T01DR | 8/16-bit compound timer 01 data register ch0 | R/W | 00000000 _B |
| 0F95 _H | T00DR | 8/16-bit compound timer 00 data register ch0 | R/W | 00000000 _B |
| 0F96 _H | TMCR0 | 8/16-bit compound timer 00/01 timer mode control register ch0 | R/W | 00000000 _B |
| 0F97 _H | T11CR0 | 8/16-bit compound timer 11 control status register 0 ch1 | R/W | 00000000 _B |
| 0F98 _H | T10CR0 | 8/16-bit compound timer 10 control status register 0 ch1 | R/W | 00000000 _B |
| 0F99 _H | T11DR | 8/16-bit compound timer 11 data register ch1 | R/W | 00000000 _B |
| 0F9A _H | T10DR | 8/16-bit compound timer 10 data register ch1 | R/W | 00000000 _B |
| 0F9B _H | TMCR1 | 8/16-bit compound timer 10/11 timer mode control register ch1 | R/W | 00000000 _B |
| 0F9C _H | PPS01 | 8/16-bit PPG1 cycle setting buffer register ch0 | R/W | 11111111 _B |
| 0F9D _H | PPS00 | 8/16-bit PPG0 cycle setting buffer register ch0 | R/W | 11111111 _B |
| 0F9E _H | PDS01 | 8/16-bit PPG1 duty setting buffer register ch0 | R/W | 11111111 _B |
| 0F9F _H | PDS00 | 8/16-bit PPG0 duty setting buffer register ch0 | R/W | 11111111 _B |
| 0FA0 _H | PPS11 | 8/16-bit PPG1 cycle setting buffer register ch1 | R/W | 11111111 _B |
| 0FA1 _H | PPS10 | 8/16-bit PPG0 cycle setting buffer register ch1 | R/W | 11111111 _B |
| 0FA2 _H | PDS11 | 8/16-bit PPG1 duty setting buffer register ch1 | R/W | 11111111 _B |
| 0FA3 _H | PDS10 | 8/16-bit PPG0 duty setting buffer register ch1 | R/W | 11111111 _B |
| 0FA4 _H | PPGS | 8/16-bit PPG starting register | R/W | 00000000 _B |
| 0FA5 _H | REVC | 8/16-bit PPG output inversion register | R/W | 00000000 _B |
| 0FA6 _H to 0FA9 _H | — | (Vacancy) | — | — |
| 0FAA _H | PDCRH0 | 16-bit PPG down counter register (Upper byte) ch0 | R | 00000000 _B |
| 0FAB _H | PDCRL0 | 16-bit PPG down counter register (Lower byte) ch0 | R | 00000000 _B |
| 0FAC _H | PCSRH0 | 16-bit PPG cycle setting buffer register (Upper byte) ch0 | R/W | 11111111 _B |
| 0FAD _H | PCSRL0 | 16-bit PPG cycle setting buffer register (Lower byte) ch0 | R/W | 11111111 _B |
| 0FAE _H | PDUTH0 | 16-bit PPG duty setting buffer register (Upper byte) ch0 | R/W | 11111111 _B |
| 0FAF _H | PDUTL0 | 16-bit PPG duty setting buffer register (Lower byte) ch0 | R/W | 11111111 _B |

(Continued)

MB95110A Series

(Continued)

| Address | Register abbreviation | Register name | R/W | Initial value |
|--|-----------------------|---|-----|-----------------------|
| 0FB0 _H to 0FBB _H | — | (Vacancy) | — | — |
| 0FBC _H | BGR1 | LIN-UART baud rate generator register 1 | R/W | 00000000 _B |
| 0FBD _H | BGR0 | LIN-UART baud rate generator register 0 | R/W | 00000000 _B |
| 0FBE _H | PSSR0 | UART/SIO prescaler selection register ch0 | R/W | 00000000 _B |
| 0FBF _H | BRSR0 | UART/SIO baud rate setting register ch0 | R/W | 00000000 _B |
| 0FC0 _H to 0FC2 _H | — | (Vacancy) | — | — |
| 0FC3 _H | AIDRL | A/D input disable register (Lower byte) | R/W | 00000000 _B |
| 0FC4 _H to 0FE2 _H | — | (Vacancy) | — | — |
| 0FE3 _H | WCDR | Watch counter data register | R/W | 00111111 _B |
| 0FE4 _H to 0FED _H | — | (Vacancy) | — | — |
| 0FEE _H | ILSR | Input level select register | R/W | 00000000 _B |
| 0FEF _H | WICR | Interrupt pin control register | R/W | 01000000 _B |
| 0FF0 _H to 0FFF _H | — | (Vacancy) | — | — |

- Read/write access symbols

R/W : Readable and Writable

R : Read only

W : Write only

- Initial value symbols

0 : The initial value of this bit is "0".

1 : The initial value of this bit is "1".

X : The initial value of this bit is undefined.

■ INTERRUPT SOURCE TABLE

| Interrupt source | Interrupt request number | Vector table address | | Bit name of interrupt level setting register | Same level priority order (at simultaneous occurrence) |
|-------------------------------------|--------------------------|----------------------|-------------------|--|---|
| | | Upper | Lower | | |
| External interrupt ch0 | IRQ0 | FFFA _H | FFFB _H | L00 [1 : 0] | <div style="display: flex; align-items: center; justify-content: center;"> <div style="margin-right: 10px;">High</div> <div style="margin-left: 10px;">Low</div> </div> |
| External interrupt ch4 | | | | | |
| External interrupt ch1 | IRQ1 | FFF8 _H | FFF9 _H | L01 [1 : 0] | |
| External interrupt ch5 | | | | | |
| External interrupt ch2 | IRQ2 | FFF6 _H | FFF7 _H | L02 [1 : 0] | |
| External interrupt ch6 | | | | | |
| External interrupt ch3 | IRQ3 | FFF4 _H | FFF5 _H | L03 [1 : 0] | |
| External interrupt ch7 | | | | | |
| UART/SIO ch0 | IRQ4 | FFF2 _H | FFF3 _H | L04 [1 : 0] | |
| 8/16-bit compound timer ch0 (Lower) | IRQ5 | FFF0 _H | FFF1 _H | L05 [1 : 0] | |
| 8/16-bit compound timer ch0 (Upper) | IRQ6 | FFEE _H | FFEF _H | L06 [1 : 0] | |
| LIN-UART (reception) | IRQ7 | FFEC _H | FFED _H | L07 [1 : 0] | |
| LIN-UART (transmission) | IRQ8 | FFEA _H | FFEB _H | L08 [1 : 0] | |
| 8/16-bit PPG ch1 (Lower) | IRQ9 | FFE8 _H | FFE9 _H | L09 [1 : 0] | |
| 8/16-bit PPG ch1 (Upper) | IRQ10 | FFE6 _H | FFE7 _H | L10 [1 : 0] | |
| (Unused) | IRQ11 | FFE4 _H | FFE5 _H | L11 [1 : 0] | |
| 8/16-bit PPG ch0 (Upper) | IRQ12 | FFE2 _H | FFE3 _H | L12 [1 : 0] | |
| 8/16-bit PPG ch0 (Lower) | IRQ13 | FFE0 _H | FFE1 _H | L13 [1 : 0] | |
| 8/16-bit compound timer ch1 (Upper) | IRQ14 | FFDE _H | FFDF _H | L14 [1 : 0] | |
| 16-bit PPG ch0 | IRQ15 | FFDC _H | FFDD _H | L15 [1 : 0] | |
| I ² C ch0 | IRQ16 | FFDA _H | FFDB _H | L16 [1 : 0] | |
| (Unused) | IRQ17 | FFD8 _H | FFD9 _H | L17 [1 : 0] | |
| 10-bit A/D converter | IRQ18 | FFD6 _H | FFD7 _H | L18 [1 : 0] | |
| Timebase timer | IRQ19 | FFD4 _H | FFD5 _H | L19 [1 : 0] | |
| Watch prescaler/counter | IRQ20 | FFD2 _H | FFD3 _H | L20 [1 : 0] | |
| (Unused) | IRQ21 | FFD0 _H | FFD1 _H | L21 [1 : 0] | |
| 8/16-bit compound timer ch1 (Lower) | IRQ22 | FFCE _H | FFCF _H | L22 [1 : 0] | |
| FLASH | IRQ23 | FFCC _H | FFCD _H | L23 [1 : 0] | |

MB95110A Series

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

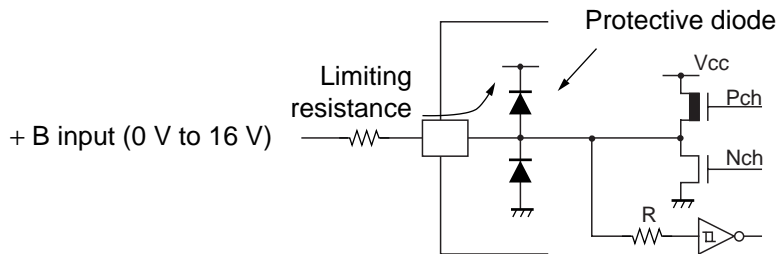
| Parameter | Symbol | Rating | | Unit | Remarks |
|--|---------------------------------------|-----------------------|-----------------------|------|---|
| | | Min | Max | | |
| Power supply voltage*1 | V _{CC} , AV _{CC} | V _{SS} – 0.3 | V _{SS} + 4.0 | V | *2 |
| | AV _R | V _{SS} – 0.3 | V _{SS} + 4.0 | | *2 MB95FV100A-101 only |
| Input voltage*1 | V _{I1} | V _{SS} – 0.3 | V _{SS} + 4.0 | V | Other than P50, P51*3 |
| | V _{I2} | V _{SS} – 0.3 | V _{SS} + 6.0 | | P50, P51 |
| Output voltage*1 | V _O | V _{SS} – 0.3 | V _{SS} + 4.0 | V | *3 |
| Maximum clamp current | I _{CLAMP} | – 2.0 | + 2.0 | mA | Applicable to pins*4 |
| Total maximum clamp current | Σ I _{CLAMP} | — | 20 | mA | Applicable to pins*4 |
| “L” level maximum output current | I _{OL1} | — | 15 | mA | Other than P00 to P07 |
| | I _{OL2} | | 15 | | P00 to P07 |
| “L” level average current | I _{OLAV1} | — | 4 | mA | Other than P00 to P07 Average output current = operating current × operating ratio (1 pin) |
| | I _{OLAV2} | | 12 | | P00 to P07 Average output current = operating current × operating ratio (1 pin) |
| “L” level total maximum output current | ΣI _{OL} | — | 100 | mA | |
| “L” level total average output current | ΣI _{OLAV} | — | 50 | mA | Total average output current = operating current × operating ratio (total of pins) |
| “H” level maximum output current | I _{OH1} | — | – 15 | mA | Other than P00 to P07 |
| | I _{OH2} | | – 15 | | P00 to P07 |
| “H” level average current | I _{OHAV1} | — | – 4 | mA | Other than P00 to P07 Average output current = operating current × operating ratio (1 pin) |
| | I _{OHAV2} | | – 8 | | P00 to P07 Average output current = operating current × operating ratio (1 pin) |
| “H” level total maximum output current | ΣI _{OH} | — | – 100 | mA | |
| “H” level total average output current | ΣI _{OHAV} | — | – 50 | mA | Total average output current = operating current × operating ratio (total of pins) |
| Power consumption | P _d | — | 320 | mW | |
| Operating temperature | T _A | – 40 | + 85 | °C | Other than MB95FV100A-101 |
| Storage temperature | T _{stg} | – 55 | + 150 | °C | |

(Continued)

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- *1 : The parameter is based on $AV_{CC} = V_{SS} = 0.0$ V.
- *2 : Apply equal potential to AV_{CC} and V_{CC} . AVR should not exceed $AV_{CC} + 0.3$ V.
- *3 : V_{I1} and V_{O} should not exceed $V_{CC} + 0.3$ V. V_{I1} must not exceed the rating voltage. However, if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_{I1} rating.
- *4 :
 - Applicable to pins : P00 to P07, P10 to P15, P20 to P24, P30 to P37, PG0
 - Use within recommended operating conditions.
 - Use at DC voltage (current).
 - The + B signal should always be applied a limiting resistance placed between the + B signal and the microcontroller.
 - The value of the limiting resistance should be set so that when the + B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
 - Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the VCC pin, and this may affect other devices.
 - Note that if the + B signal is inputted when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
 - Note that if the + B input is applied during power-on, the power supply is provided from the pins and the resulting power supply voltage may not be sufficient to operate the power-on reset.
 - Care must be taken not to leave the + B input pin open.
 - Sample recommended circuits :

• Input/Output Equivalent Circuits



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

MB95110A Series

2. Recommended Operating Conditions

(AV_{SS} = V_{SS} = 0.0 V)

| Parameter | Symbol | Value | | Unit | Remarks |
|-----------------------|---------------------------------------|-------|-------|------|--|
| | | Min | Max | | |
| Power supply voltage | V _{CC} , AV _{CC} | 1.8*1 | 3.3*2 | V | At normal operating, FLASH product, T _A = -10 °C to +85 °C |
| | | 1.8*1 | 3.6 | | At normal operating, MASK product, T _A = -10 °C to +85 °C |
| | | 2.0*1 | 3.3*2 | | At normal operating, FLASH product, T _A = -40 °C to +85 °C |
| | | 2.0*1 | 3.6 | | At normal operating, MASK product, T _A = -40 °C to +85 °C |
| | | 2.6 | 3.6 | | MB95FV100A-101 |
| | | 1.5 | 3.3*2 | | Retain status of stop operation, FLASH product |
| | | 1.5 | 3.6 | | Retain status of stop operation, MASK product |
| Operating temperature | T _A | - 40 | + 85 | °C | Other than MB95FV100A-101 |

*1 : The values vary with the operating frequency.

*2 : Consult Fujitsu separately for a guarantee of a maximum value of 3.6 V.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

MB95110A Series

3. DC Characteristics

($V_{CC} = AV_{CC} = 3.3\text{ V}$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$ [MB95FV100A-101 is $T_A = +25\text{ }^\circ\text{C}$])

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|---------------------------------------|------------|---|---------------------------|----------------|-----|----------------|------|--|
| | | | | Min | Typ | Max | | |
| "H" level input voltage | V_{IH1} | P10, P67 | *1 | 0.7 V_{CC} | — | $V_{CC} + 0.3$ | V | At selecting of CMOS input level (hysteresis input) |
| | V_{IH2} | P50, P51 | *1 | 0.7 V_{CC} | — | $V_{SS} + 5.5$ | V | At selecting of CMOS input level (hysteresis input) |
| | V_{IHS1} | P00 to P07, P10 to P15, P20 to P24, P30 to P37, P60 to P67, PG0, PG1*2, PG2*2 | *1 | 0.8 V_{CC} | — | $V_{CC} + 0.3$ | V | Hysteresis input |
| | V_{IHS2} | P50, P51 | *1 | 0.8 V_{CC} | — | $V_{SS} + 5.5$ | V | Hysteresis input |
| | V_{IHM} | $\overline{\text{RST}}$, MOD | — | 0.7 V_{CC} | — | $V_{CC} + 0.3$ | V | CMOS input (FLASH product) |
| | | | — | 0.8 V_{CC} | — | $V_{CC} + 0.3$ | V | Hysteresis input (MASK product) |
| "L" level input voltage | V_{IL} | P10, P50, P51, P67 | *1 | $V_{SS} - 0.3$ | — | 0.3 V_{CC} | V | At selecting of CMOS input level (hysteresis input) |
| | V_{ILS} | P00 to P07, P10 to P15, P20 to P24, P30 to P37, P50, P51, P60 to P67, PG0, PG1*2, PG2*2 | *1 | $V_{SS} - 0.3$ | — | 0.2 V_{CC} | V | Hysteresis input |
| | V_{ILM} | $\overline{\text{RST}}$, MOD | — | $V_{SS} - 0.3$ | — | 0.3 V_{CC} | V | CMOS input (FLASH product) |
| | | | — | $V_{SS} - 0.3$ | — | 0.2 V_{CC} | V | Hysteresis input (MASK product) |
| Open drain output application voltage | V_D | P50, P51 | — | $V_{SS} - 0.3$ | — | $V_{SS} + 5.5$ | V | |
| "H" level output voltage | V_{OH1} | Output pin other than P00 to P07 | $I_{OH} = -4.0\text{ mA}$ | 2.4 | — | — | V | MB95FV100A-101 a conditional : $I_{OH} = -2.0\text{ mA}$ |
| | V_{OH2} | P00 to P07 | $I_{OH} = -8.0\text{ mA}$ | 2.4 | — | — | V | MB95FV100A-101 a conditional : $I_{OH} = -5.0\text{ mA}$ |

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MB95110A Series

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($V_{CC} = AV_{CC} = 3.3\text{ V}$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$ [MB95FV100A-101 is $T_A = +25\text{ }^\circ\text{C}$])

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|---|--|---|---|-------|---------------|-----|---------------|---|
| | | | | Min | Typ | Max | | |
| “L” level output voltage | V_{OL1} | Output pin other than P00 to P07 | $I_{OL} = 4.0\text{ mA}$ | — | — | 0.4 | V | MB95FV100A-101 a conditional : $I_{OL} = 3.0\text{ mA}$ |
| | V_{OL2} | P00 to P07 | $I_{OL} = 12\text{ mA}$ | — | — | 0.4 | V | MB95FV100A-101 a conditional : $I_{OL} = 8.0\text{ mA}$ |
| Input leakage current (High-Z output leakage current) | I_{LI} | Port other than P50, P51 | $0.0\text{ V} < V_I < V_{CC}$ | -5 | — | +5 | μA | When no pull-up resistor is specified |
| Open drain output leakage current | I_{LIOD} | P50, P51 | $0.0\text{ V} < V_I < V_{SS} + 5.5\text{ V}$ | — | — | +5 | μA | |
| Pull-up resistor | R_{PULL} | P10 to P15, P20 to P24, P30 to P37, PG0, PG1*2, PG2*2 | $V_I = 0.0\text{ V}$ | 25 | 50 | 100 | k Ω | When pull-up resistor is specified |
| Pull-down resistor | R_{MOD} | MOD | $V_I = V_{CC}$ | 50 | 100 | 200 | k Ω | MASK product only |
| Power supply current*3 | I_{CC} | V_{CC} (external clock operation) | $F_{CH} = 20\text{ MHz}$ $f_{mp} = 10\text{ MHz}$ Main clock mode (divided by 2) | — | 11 | 14 | mA | FLASH product |
| | | | | — | 7.3 | 10 | mA | MASK product |
| | | | | — | 30 | 35 | mA | FLASH product (at FLASH writing and erasing) |
| | I_{CCS} | | $F_{CH} = 20\text{ MHz}$ $f_{mp} = 10\text{ MHz}$ Main Sleep mode (divided by 2) | — | 4.5 | 6 | mA | |
| | I_{CCL} | | $F_{CL} = 32\text{ kHz}$ $f_{mpl} = 16\text{ kHz}$ Subclock mode (divided by 2) , $T_A = +25\text{ }^\circ\text{C}$ | — | 25 | 35 | μA | |
| I_{CCLS} | $F_{CL} = 32\text{ kHz}$ $f_{mpl} = 16\text{ kHz}$ Sub sleep mode (divided by 2) , $T_A = +25\text{ }^\circ\text{C}$ | — | 7 | 15 | μA | | | |

(Continued)

MB95110A Series

(Continued)

($V_{CC} = AV_{CC} = 3.3\text{ V}$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$ [MB95FV100A-101 is $T_A = +25\text{ }^\circ\text{C}$])

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|------------------------|---|--|---|---|-----|-----|------|---------------|
| | | | | Min | Typ | Max | | |
| Power supply current*3 | I _{CCCT} | V _{CC} (external clock operation) | F _{CL} = 32 kHz Watch mode | — | 2 | 10 | μA | FLASH product |
| | | | Main stop mode T _A = +25 °C | — | 1 | 5 | μA | MASK product |
| | I _{CCMPLL} | | F _{CH} = 4 MHz f _{mp} = 10 MHz | — | 10 | 14 | mA | FLASH product |
| | | | Main PLL mode (multiplied by 2.5) | — | 6.7 | 10 | mA | MASK product |
| | I _{CCSPLL} | | F _{CL} = 32 kHz f _{mpl} = 128 kHz Sub PLL mode (multiplied by 4), T _A = +25 °C | — | 190 | 250 | μA | |
| | I _{CTS} | | F _{CH} = 10 MHz Timebase timer mode T _A = +25 °C | — | 0.4 | 0.5 | mA | |
| | I _{CCCH} | | Substop mode T _A = +25 °C | — | 1 | 5 | μA | |
| | I _A | | AV _{CC} | F _{CH} = 10 MHz At A/D converting | — | 1.3 | 2.2 | mA |
| I _{AH} | F _{CH} = 10 MHz At A/D converting stop T _A = +25 °C | — | | 1 | 5 | μA | | |
| Input capacitance | C _{IN} | Other than AV _{CC} , AV _{SS} , V _{CC} , and V _{SS} | — | 5 | 15 | pF | | |

*1 : P10, P50, P51, and P67 can switch the input level to either the “CMOS input level” or “hysteresis input level”.
The switching of the input level can be set by the input level selection register (ILSR).

*2 : Single-clock products only

*3 : The power-supply current is determined by the external clock.

- Refer to “4. AC characteristics (1) Clock Timing” for F_{CH} and F_{CL}.
- Refer to “4. AC characteristics (2) Source Clock/Machine Clock” for f_{mp} and f_{mpl}.

MB95110A Series

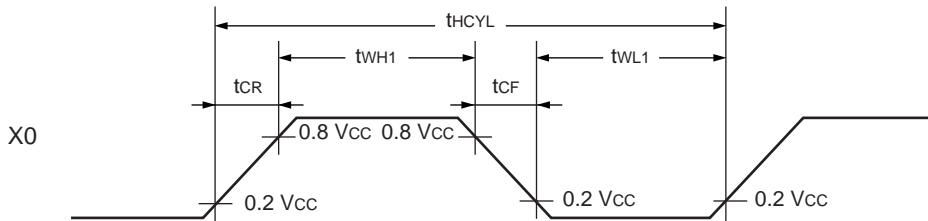
4. AC Characteristics

(1) Clock Timing

(V_{CC} = 3.3 V, AV_{SS} = V_{SS} = 0.0 V, T_A = -40 °C to +85 °C)

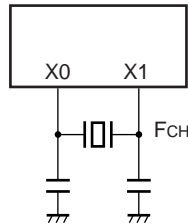
| Parameter | Symbol | Pin | Conditions | Value | | | Unit | Remarks |
|-------------------------------------|--------------------------------------|----------|------------|-------|--------|-----|--|-------------------------------------|
| | | | | Min | Typ | Max | | |
| Clock frequency | F _{CH} | X0, X1 | — | 1 | — | 10 | MHz | When using Main oscillation circuit |
| | | | | 1 | — | 20 | MHz | When using external clock |
| | | | | 3 | — | 10 | MHz | Main PLL multiplied by 1 |
| | | | | 3 | — | 5 | MHz | Main PLL multiplied by 2 |
| | | | | 3 | — | 4 | MHz | Main PLL multiplied by 2.5 |
| | F _{CL} | X0A, X1A | | — | 32.768 | — | kHz | When using Sub oscillation circuit |
| Clock cycle time | t _{H CYL} | X0, X1 | 100 | — | 1000 | ns | When using Main oscillation circuit | |
| | | | 50 | — | 1000 | ns | When using Sub oscillation circuit | |
| | t _{L CYL} | X0A, X1A | — | 30.5 | — | μs | Subclock | |
| Input clock pulse width | t _{WH1} t _{WL1} | X0 | 10 | — | — | ns | When using external clock Duty ratio is about 30% to 70%. | |
| | t _{WH2} t _{WL2} | X0A | — | 15.2 | — | μs | | |
| Input clock rise time and fall time | t _{CR} t _{CF} | X0, X0A | — | — | 5 | ns | When using external clock | |

- X0 and X1 Timing and Applying Conditions

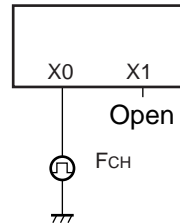


- Main Clock Applying Conditions

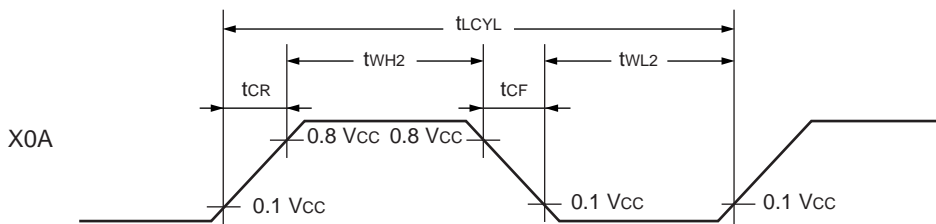
When using a crystal or ceramic oscillator



When using external clock

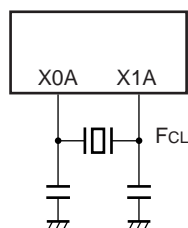


- X0A and X1A Timing and Applying Conditions

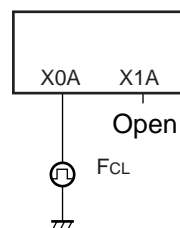


- Subclock Applying Conditions

When using a crystal or ceramic oscillator



When using external clock



MB95110A Series

(2) Source Clock/Machine Clock

(V_{CC} = 3.3 V, AV_{SS} = V_{SS} = 0.0 V, T_A = - 40 °C to + 85 °C)

| Parameter | Symbol | Pin name | Value | | | Unit | Remarks |
|---|------------------|----------|--------|-----|---------|------|---|
| | | | Min | Typ | Max | | |
| Source clock* ¹ (Clock before setting division) | SCLK | — | 100 | — | 2000 | ns | When using Main clock Min : F _{CH} = 10 MHz, PLL multiplied by 1 Max : F _{CH} = 1 MHz, divided by 2 |
| | | | 7.6 | — | 61.0 | μs | When using Subclock Min : F _{CL} = 32 kHz, PLL multiplied by 4 Max : F _{CL} = 32 kHz, divided by 2 |
| Source clock frequency | f _{sp} | — | 0.5 | — | 10.0 | MHz | When using Main clock |
| | f _{spl} | — | 16.384 | — | 131.072 | kHz | When using Subclock |
| Machine clock* ² (Minimum instruction execution time) | MCLK | — | 100 | — | 32000 | ns | When using Main clock Min : SLCK = 10 MHz, no division Max : SLCK = 0.5 MHz, divided by 16 |
| | | | 7.6 | — | 976.5 | μs | When using Subclock Min : SLCK = 131 kHz, no division Max : SLCK = 16 kHz, divided by 16 |
| Machine clock frequency | f _{mp} | — | 0.031 | — | 10.000 | MHz | When using Main clock |
| | f _{mpl} | — | 1.024 | — | 131.072 | kHz | When using Subclock |

*1 : Clock before setting division due to machine clock division ratio selection bit (SYCC : DIV1 and DIV0) . This source clock is divided by the machine clock division ratio selection bit (SYCC : DIV1 and DIV0) , and it becomes the machine clock. Further, the source clock can be selected as follow.

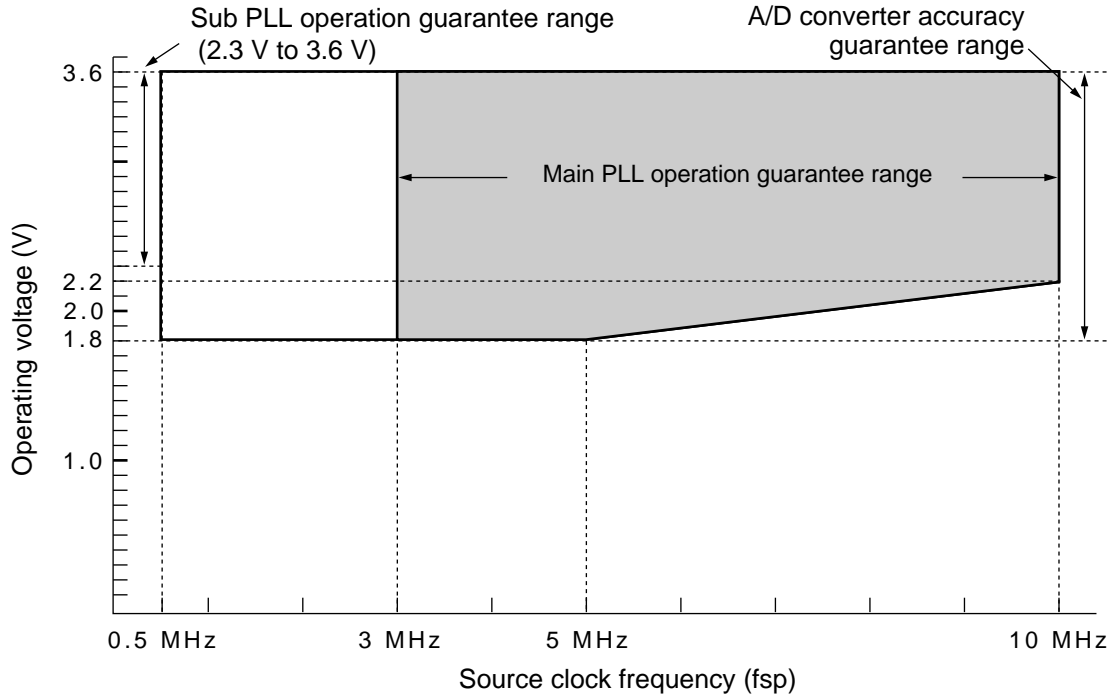
- Main clock divided by 2
- PLL multiplication of main clock (select from 1, 2, 2.5 multiplication)
- Subclock divided by 2
- PLL multiplication of subclock (select from 2, 3, 4 multiplication)

*2 : Operation clock of the microcontroller. Machine clock can be selected as follow.

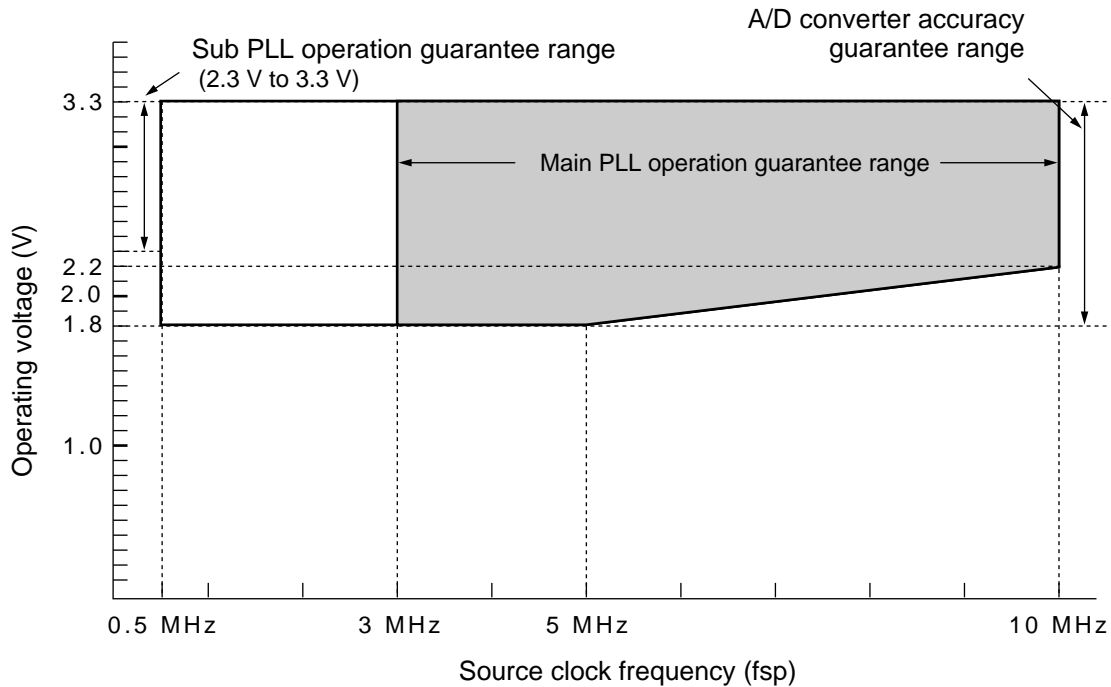
- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

• **Operating voltage – Operating frequency**

- MASK product



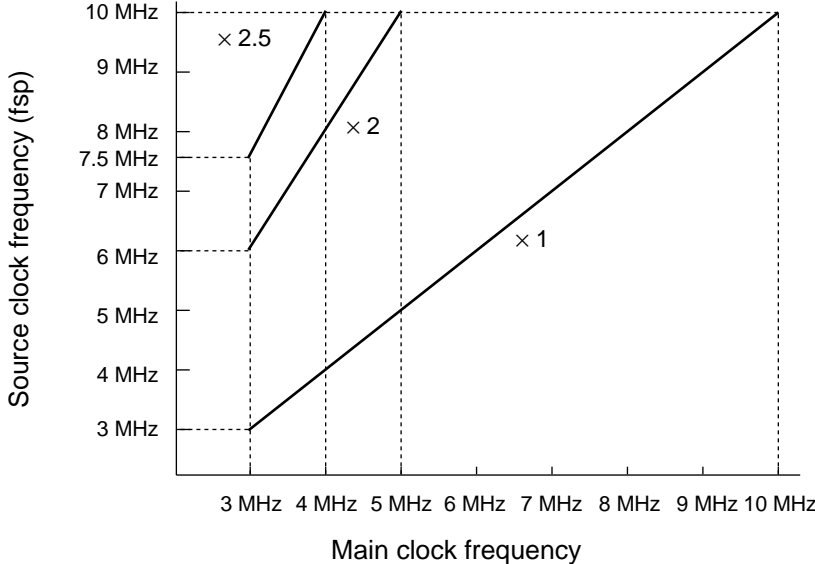
- FLASH product



Note: In operating by 2.0 V or less, only "T_A = -10 °C to +85 °C" is guaranteed.

MB95110A Series

• Main PLL operation frequency



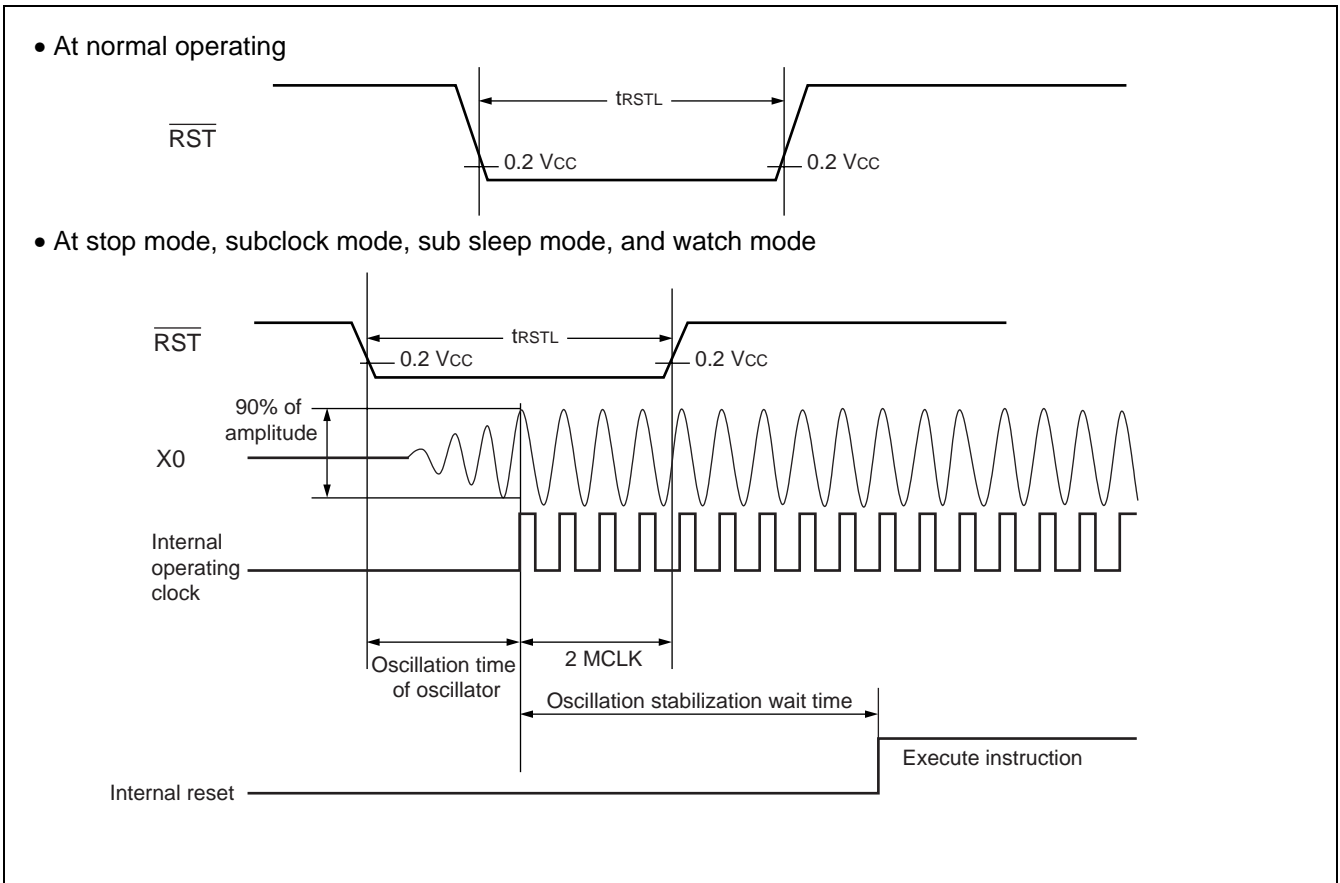
(3) Reset Timing

($V_{CC} = 3.3\text{ V}$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Value | | Unit | Remarks |
|---|-------------------|---|-----|------|---|
| | | Min | Max | | |
| $\overline{\text{RST}}$ "L" level pulse width | t_{RSTL} | 2 MCLK^{*1} | — | ns | At normal operating |
| | | Oscillation time of oscillator ^{*2} + 2 MCLK^{*1} | — | ns | At stop mode, subclock mode, Sub sleep mode, and watch mode |

*1 : Refer to "(2) Source Clock/Machine Clock" for MCLK.

*2 : Oscillation time of oscillator is the time that the amplitude reaches 90%. In the crystal oscillator, the oscillation time is between several ms and tens of ms. In FAR/ceramic oscillators, the oscillation time is between hundreds of μs and several ms. In the external clock, the oscillation time is 0 ms.



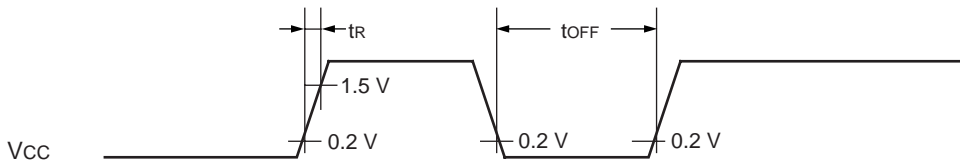
MB95110A Series

(4) Power-on Reset

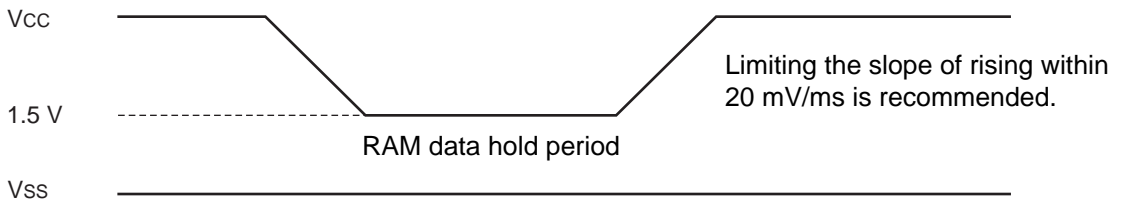
(AV_{SS} = V_{SS} = 0.0 V, T_A = - 40 °C to + 85 °C)

| Parameter | Symbol | Conditions | Value | | Unit | Remarks |
|--------------------------|------------------|------------|-------|-----|------|----------------------------|
| | | | Min | Max | | |
| Power supply rising time | t _R | — | — | 36 | ms | |
| Power supply cutoff time | t _{OFF} | — | 1 | — | ms | Due to repeated operations |

Note : The power supply must be turned on within the selected oscillation stabilization time.



Sudden change of power supply voltage may activate the power-on reset function. When changing power supply voltages during operation, set the slope of rising within 20 mV/ms as shown below. In this case, do not use PLL clock. However, if voltage drop is 1V/s or less, use of PLL clock is allowed during operation.

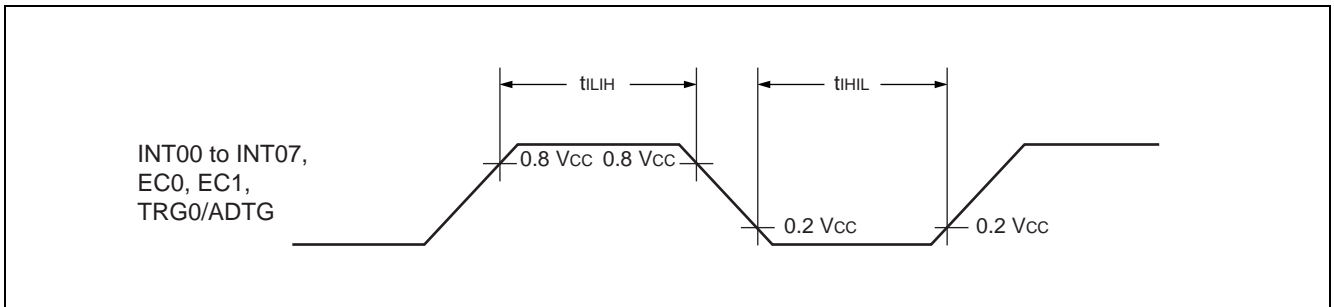


(5) Peripheral Input Timing

($V_{CC} = 3.3\text{ V}$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$)

| Parameter | Symbol | Pin name | Value | | Unit | Remarks |
|----------------------------------|-----------|-------------------------------------|---------|-----|------|---------|
| | | | Min | Max | | |
| Peripheral input "H" pulse width | t_{LIH} | INT00 to INT07, EC0, EC1, TRG0/ADTG | 2 MCLK* | — | ns | |
| Peripheral input "L" pulse width | t_{HIL} | | 2 MCLK* | — | ns | |

* : Refer to " (2) Source Clock/Machine Clock" for MCLK.



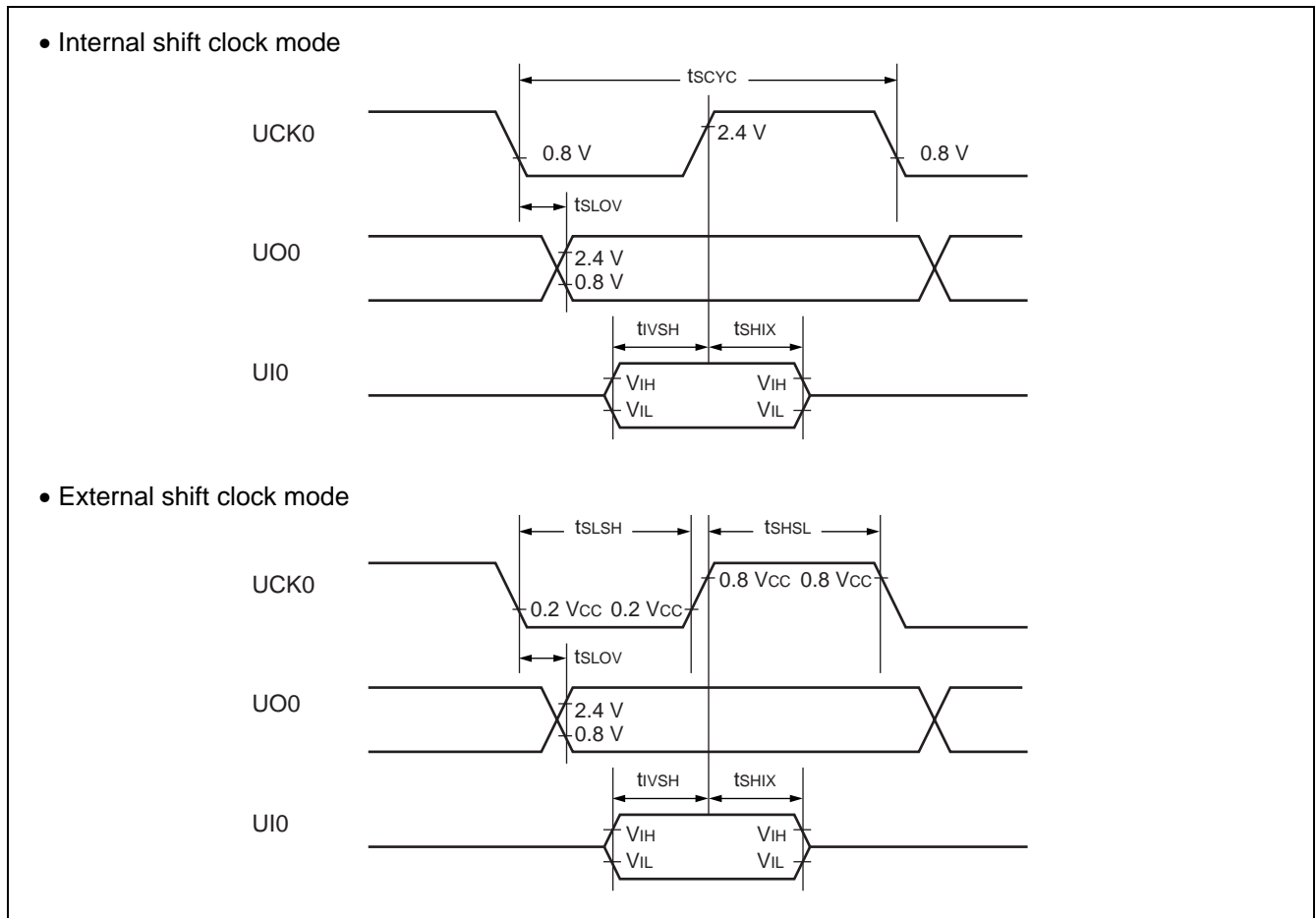
MB95110A Series

(6) UART/SIO, Serial I/O Timing

($V_{CC} = 3.3\text{ V}$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|------------------------------|------------|-----------|--------------------------|---------|-----|------|---------|
| | | | | Min | Max | | |
| Serial clock cycle time | t_{SCYC} | UCK0 | Internal clock operation | 4 MCLK* | — | ns | |
| UCK ↓ → UO time | t_{SLOV} | UCK0, UO0 | | - 190 | 190 | ns | |
| Valid UI → UCK ↑ | t_{IVSH} | UCK0, UI0 | | 2 MCLK* | — | ns | |
| UCK ↑ → valid UI hold time | t_{SHIX} | UCK0, UI0 | | 2 MCLK* | — | ns | |
| Serial clock "H" pulse width | t_{SHSL} | UCK0 | External clock operation | 4 MCLK* | — | ns | |
| Serial clock "L" pulse width | t_{SLSH} | UCK0 | | 4 MCLK* | — | ns | |
| UCK ↓ → UO time | t_{SLOV} | UCK0, UO0 | | — | 190 | ns | |
| Valid UI → UCK ↑ | t_{IVSH} | UCK0, UI0 | | 2 MCLK* | — | ns | |
| UCK ↑ → valid UI hold time | t_{SHIX} | UCK0, UI0 | 2 MCLK* | — | ns | | |

* : Refer to "(2) Source Clock/Machine Clock" for MCLK.



(7) LIN-UART Timing

ESCR : SCES = 0, ECCR : SCDE = 0

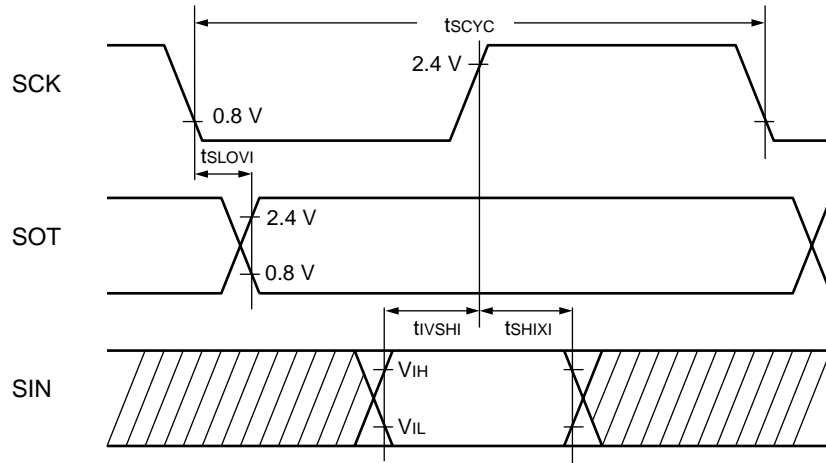
(V_{CC} = 3.3 V, AV_{SS} = V_{SS} = 0.0 V, T_A = -40 °C to +85 °C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit |
|------------------------------|--------------------|----------|---|--------------------------|--------------|------|
| | | | | Min | Max | |
| Serial clock cycle time | t _{SCYC} | SCK | Internal clock operation output pin : C _L = 80 pF + 1 TTL. | 5 MCLK* | — | ns |
| SCK ↑ → SOT delay time | t _{SLOVI} | SCK, SOT | | -95 | 95 | ns |
| Valid SIN → SCK ↑ | t _{IVSHI} | SCK, SIN | | MCLK* + 190 | — | ns |
| SCK ↑ → valid SIN hold time | t _{SHIXI} | SCK, SIN | | 0 | — | ns |
| Serial clock "L" pulse width | t _{LSLH} | SCK | External clock operation output pin : C _L = 80 pF + 1 TTL. | 3 MCLK* - t _r | — | ns |
| Serial clock "H" pulse width | t _{SHSL} | SCK | | MCLK* + 95 | — | ns |
| SCK ↓ → SOT delay time | t _{SLOVE} | SCK, SOT | | — | 2 MCLK* + 95 | ns |
| Valid SIN → SCK ↑ | t _{IVSHE} | SCK, SIN | | 190 | — | ns |
| SCK ↑ → Valid SIN hold time | t _{SHIXE} | SCK, SIN | | MCLK* + 95 | — | ns |
| SCK fall time | t _f | SCK | | — | 10 | ns |
| SCK rise time | t _r | SCK | | — | 10 | ns |

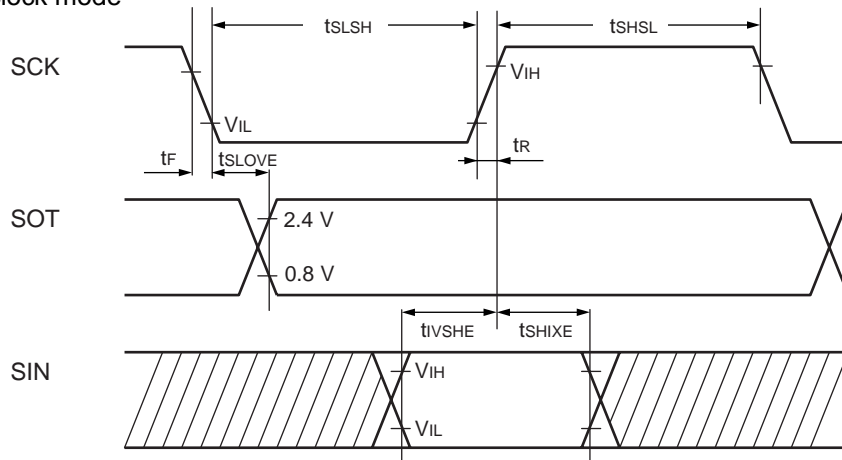
* : Refer to "(2) Source Clock/Machine Clock" for MCLK.

MB95110A Series

- Internal shift clock mode



- External shift clock mode



MB95110A Series

ESCR : SCES = 1, ECCR : SCDE = 0

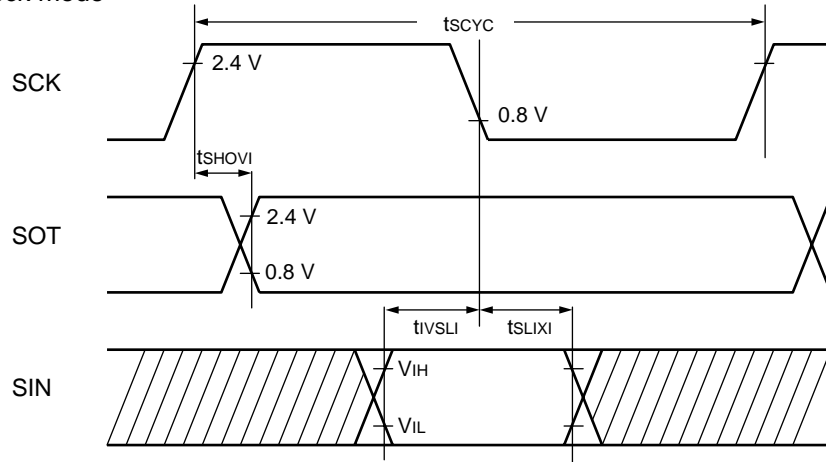
(V_{CC} = 3.3 V, AV_{SS} = V_{SS} = 0.0 V, T_A = -40 °C to + 85 °C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit |
|------------------------------|--------------------|----------|---|-----------------------------|-----------------|------|
| | | | | Min | Max | |
| Serial clock cycle time | t _{SCYC} | SCK | Internal clock operation output pin : C _L = 80 pF + 1 TTL. | 5 MCLK* | — | ns |
| SCK ↑ → SOT delay time | t _{SHOVI} | SCK, SOT | | -95 | 95 | ns |
| Valid SIN → SCK ↓ | t _{IVSLI} | SCK, SIN | | MCLK* + 190 | — | ns |
| SCK ↓ → Valid SIN hold time | t _{SLIXI} | SCK, SIN | | 0 | — | ns |
| Serial clock "H" pulse width | t _{SHSL} | SCK | External clock operation output pin : C _L = 80 pF + 1 TTL. | 3 MCLK* - t _R | — | ns |
| Serial clock "L" pulse width | t _{LSLH} | SCK | | MCLK* + 95 | — | ns |
| SCK ↑ → SOT delay time | t _{SHOVE} | SCK, SOT | | — | 2 MCLK* + 95 | ns |
| Valid SIN → SCK ↓ | t _{IVSLE} | SCK, SIN | | 190 | — | ns |
| SCK ↓ → Valid SIN hold time | t _{SLIXE} | SCK, SIN | | MCLK* + 95 | — | ns |
| SCK fall time | t _F | SCK | | — | 10 | ns |
| SCK rise time | t _R | SCK | | — | 10 | ns |

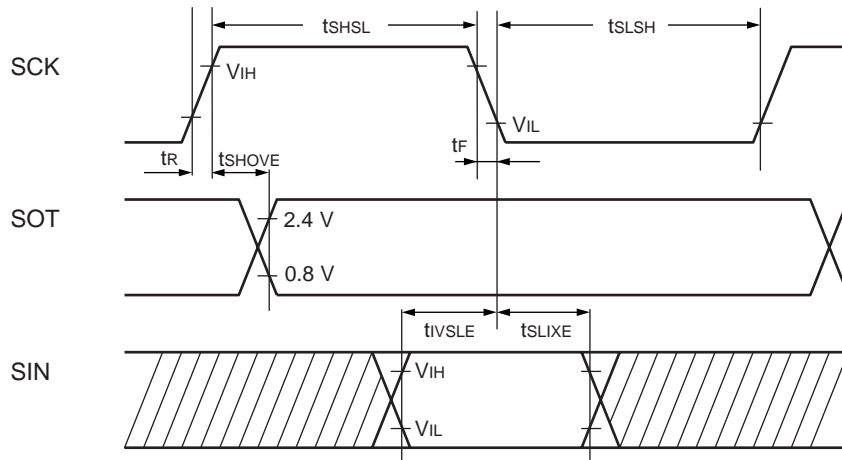
* : Refer to "(2) Source Clock/Machine Clock" for MCLK.

MB95110A Series

- Internal shift clock mode



- External shift clock mode



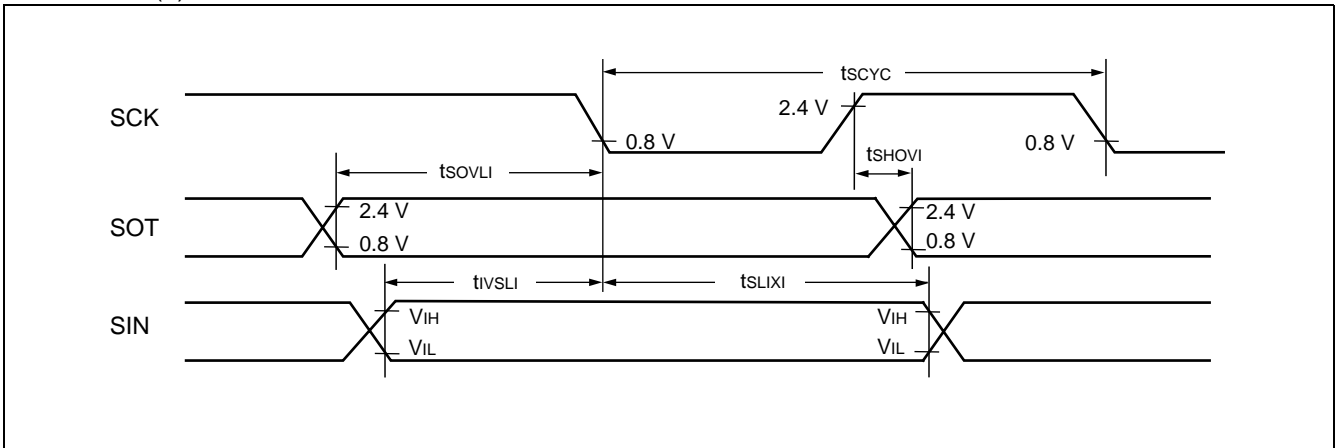
MB95110A Series

ESCR : SCES = 0, ECCR : SCDE = 1

(V_{CC} = 3.3 V, AV_{SS} = V_{SS} = 0.0 V, T_A = -40 °C to +85 °C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit |
|-----------------------------|--------------------|----------|--|-------------|---------|------|
| | | | | Min | Max | |
| Serial clock cycle time | t _{SCYC} | SCK | Internal clock operation output pin : C _L = 80 pF + 1 TTL. | 5 MCLK* | — | ns |
| SCK ↑ → SOT delay time | t _{SHOVI} | SCK, SOT | | -95 | 95 | ns |
| Valid SIN → SCK ↓ | t _{IVSLI} | SCK, SIN | | MCLK* + 190 | — | ns |
| SCK ↓ → valid SIN hold time | t _{SLIXI} | SCK, SIN | | 0 | — | ns |
| SOT → SCK ↓ delay time | t _{SOVLI} | SCK, SOT | | — | 4 MCLK* | ns |

* : Refer to “(2) Source Clock/Machine Clock” for MCLK.



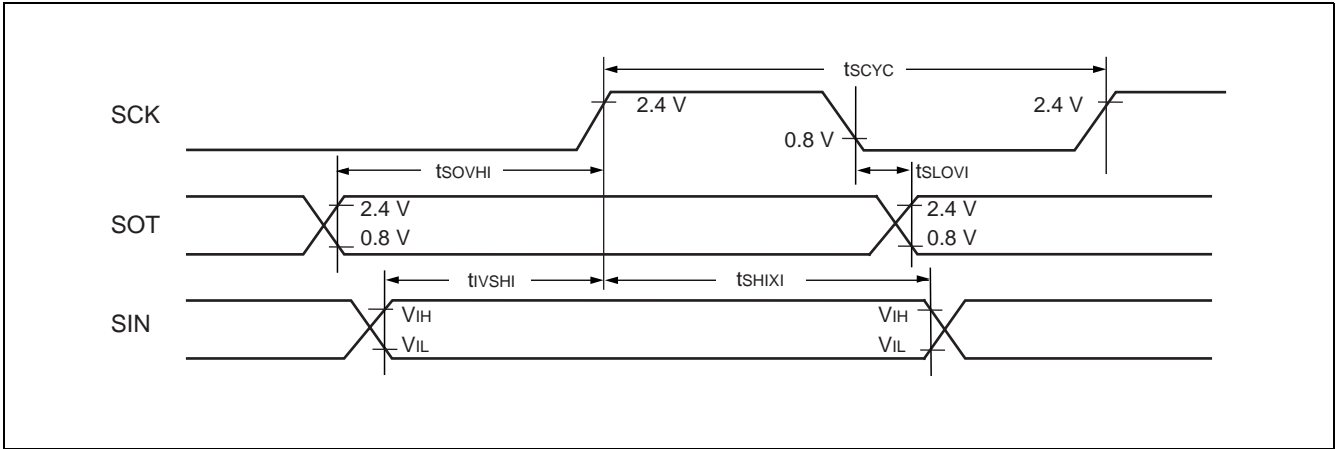
MB95110A Series

ESCR : SCES = 1, ECCR : SCDE = 1

(V_{CC} = 3.3 V, AV_{SS} = V_{SS} = 0.0 V, T_A = -40 °C to +85 °C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit |
|-----------------------------|--------------------|----------|--|-------------|---------|------|
| | | | | Min | Max | |
| Serial clock cycle time | t _{SCYC} | SCK | Internal clock operation output pin : C _L = 80 pF + 1 TTL. | 5 MCLK* | — | ns |
| SCK ↓ → SOT delay time | t _{SLOVI} | SCK, SOT | | -95 | 95 | ns |
| Valid SIN → SCK ↑ | t _{IVSHI} | SCK, SIN | | MCLK* + 190 | — | ns |
| SCK ↑ → valid SIN hold time | t _{SHIXI} | SCK, SIN | | 0 | — | ns |
| SOT → SCK ↑ delay time | t _{SOVHI} | SCK, SOT | | — | 4 MCLK* | ns |

* : Refer to “(2) Source Clock/Machine Clock” for MCLK.



(8) I²C Timing

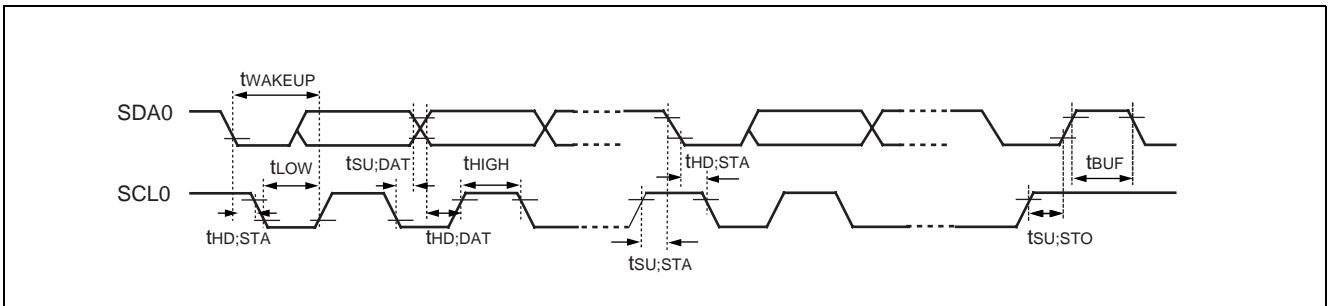
(V_{CC} = 3.3 V, AV_{SS} = V_{SS} = 0.0 V, T_A = -40 °C to +85 °C)

| Parameter | Symbol | Conditions | Value | | | | Unit | Remarks |
|---|---------------------|----------------------------|---------------|--------|-----------|-------|------|---------|
| | | | Standard-mode | | Fast-mode | | | |
| | | | Min | Max | Min | Max | | |
| SCL clock frequency | f _{SCL} | | 0 | 100 | 0 | 400 | kHz | |
| (Repeat) Start condition hold time SDA ↓ → SCL ↓ | t _{HD;STA} | R = 1.7 kΩ, C = 50 pF*1 | 4.0 | — | 0.6 | — | μs | |
| SCL clock "L" width | t _{LOW} | | 4.7 | — | 1.3 | — | μs | |
| SCL clock "H" width | t _{HIGH} | | 4.0 | — | 0.6 | — | μs | |
| (Repeat) Start condition setup time SCL ↑ → SDA ↓ | t _{SU;STA} | | 4.7 | — | 0.6 | — | μs | |
| Data hold time SCL ↓ → SDA ↓ ↑ | t _{HD;DAT} | | 0 | 3.45*2 | 0 | 0.9*3 | μs | |
| Data setup time SDA ↓ ↑ → SCL ↑ | t _{SU;DAT} | | 0.25 | — | 0.1 | — | μs | |
| Stop condition setup time SCL ↑ → SDA ↑ | t _{SU;STO} | | 4 | — | 0.6 | — | μs | |
| Bus free time between stop condition and start condition | t _{BUF} | | 4.7 | — | 1.3 | — | μs | |

*1 : R, C : Pull-up resistor and load capacitor of the SCL and SDA lines.

*2 : The maximum t_{HD;DAT} have only to be met if the device dose not stretch the "L" width (t_{LOW}) of the SCL signal.

*3 : A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement t_{SU;DAT} ≥ 250 ns must then be met.



MB95110A Series

(V_{CC} = 3.3 V, AV_{SS} = V_{SS} = 0.0 V, T_A = -40 °C to + 85 °C)

| Parameter | Symbol | I/O Timing | | Unit | Remarks |
|--|---------------------|---|---|------|--|
| | | Min | Max | | |
| SCL clock "L" width | t _{LOW} | $(2 + nm^{*2} / 2)$ MCLK ^{*1} - 20 | — | ns | Master mode |
| SCL clock "H" width | t _{HIGH} | $(nm^{*2} / 2)$ MCLK ^{*1} - 20 | $(nm^{*2} / 2)$ MCLK ^{*1} + 20 | ns | Master mode |
| Start condition hold time | t _{HD;STA} | $(-1 + nm^{*2} / 2)$ MCLK ^{*1} - 20 | $(-1 + nm^{*2})$ MCLK ^{*1} + 20 | ns | Master mode Maximum value is applied when m, n = 1, 8. Otherwise, the minimum value is applied. |
| Stop condition setup time | t _{SU;STO} | $(1 + nm^{*2} / 2)$ MCLK ^{*1} - 20 | $(1 + nm^{*2} / 2)$ MCLK ^{*1} + 20 | ns | Master mode |
| Start condition setup time | t _{SU;STA} | $(1 + nm^{*2} / 2)$ MCLK ^{*1} - 20 | $(1 + nm^{*2} / 2)$ MCLK ^{*1} + 20 | ns | Master mode |
| Bus free time between stop condition and start condition | t _{BUF} | $(2 nm^{*2} + 4)$ MCLK ^{*1} - 20 | — | ns | |
| Data hold time | t _{HD;DAT} | 3 MCLK ^{*1} - 20 | — | ns | Master mode |
| Data setup time | t _{SU;DAT} | $(-2 + nm^{*2} / 2)$ MCLK ^{*1} - 20 | $(-1 + nm^{*2} / 2)$ MCLK ^{*1} + 20 | ns | Master mode When assuming that "L" of SCL is not extended, the minimum value is applied to first bit of continuous data. Otherwise, the maximum value is applied. |
| Setup time between clearing interrupt and SCL rising | t _{SU;INT} | $(nm^{*2} / 2)$ MCLK ^{*1} - 20 | $(1 + nm^{*2} / 2)$ MCLK ^{*1} + 20 | ns | Minimum value is applied to interrupt at 9th SCL↓. Maximum value is applied to interrupt at 8th SCL↓. |
| SCL clock "L" width | t _{LOW} | 4 MCLK ^{*1} - 20 | — | ns | At reception |
| SCL clock "H" width | t _{HIGH} | 4 MCLK ^{*1} - 20 | — | ns | At reception |
| Start condition detection | t _{HD;STA} | 2 MCLK ^{*1} - 20 | — | ns | Undetected when 1 MCLK is used at reception |
| Stop condition detection | t _{SU;STO} | 2 MCLK ^{*1} - 20 | — | ns | Undetected when 1 MCLK is used at reception |
| Restart condition detection condition | t _{SU;STA} | 2 MCLK ^{*1} - 20 | — | ns | Undetected when 1 MCLK is used at reception |
| Bus free time | t _{BUF} | 2 MCLK ^{*1} - 20 | — | ns | At reception |
| Data hold time | t _{HD;DAT} | 2 MCLK ^{*1} - 20 | — | ns | At slave transmission mode |
| Data setup time | t _{SU;DAT} | t _{LOW} - 3 MCLK ^{*1} - 20 | — | ns | At slave transmission mode |
| Data hold time | t _{HD;DAT} | 0 | — | ns | At reception |
| Data setup time | t _{SU;DAT} | MCLK ^{*1} - 20 | — | ns | At reception |

(Continued)

(Continued)

| Parameter | Symbol | I/O Timing | | Unit | Remarks |
|------------------------------------|----------------------|--|-----|------|---------|
| | | Min | Max | | |
| SDA↓→SCL↑ (at wakeup function) | t _{WAKE-UP} | Oscillation stabilization wait time + 2 MCLK*1 – 20 | — | ns | |

*1 : Refer to “ (2) Source Clock/Machine Clock” for MCLK.

- *2 :
- m is CS4 bit and CS3 bit (bit 4 and bit 3) of clock control register (ICCR) .
 - n is CS2 bit to CS0 bit (bit 2 to bit 0) of clock control register (ICCR) .
 - Actual timing of I²C is determined by m and n values set by the machine clock (MCLK) and ICCR [4 : 0].
 - Standard-mode :
m and n can be set at the range : 0.9 MHz < MCLK (machine clock) < 10 MHz.
Setting of m and n determines the machine clock that can be used below.

| | |
|--|---------------------------|
| (m, n) = (1, 8) | : 0.9 MHz < MCLK ≤ 1 MHz |
| (m, n) = (1, 22), (5, 4), (6, 4), (7, 4), (8, 4) | : 0.9 MHz < MCLK ≤ 2 MHz |
| (m, n) = (1, 38), (5, 8), (6, 8), (7, 8), (8, 8) | : 0.9 MHz < MCLK ≤ 4 MHz |
| (m, n) = (1, 98) | : 0.9 MHz < MCLK ≤ 10 MHz |
 - Fast-mode :
m and n can be set at the range : 3.3 MHz < MCLK (machine clock) < 10 MHz.
Setting of m and n determines the machine clock that can be used below.

| | |
|--------------------------|---------------------------|
| (m, n) = (1, 8) | : 3.3 MHz < MCLK ≤ 4 MHz |
| (m, n) = (1, 22), (5, 4) | : 3.3 MHz < MCLK ≤ 8 MHz |
| (m, n) = (6, 4) | : 3.3 MHz < MCLK ≤ 10 MHz |

MB95110A Series

5. A/D Converter

(1) A/D Converter Electrical Characteristics

(AVcc = Vcc = 1.8 V to 3.3 V [FLASH product], AVcc = Vcc = 1.8 V to 3.6 V [MASK product], AVss = Vss = 0.0 V, TA = -40 °C to +85 °C)

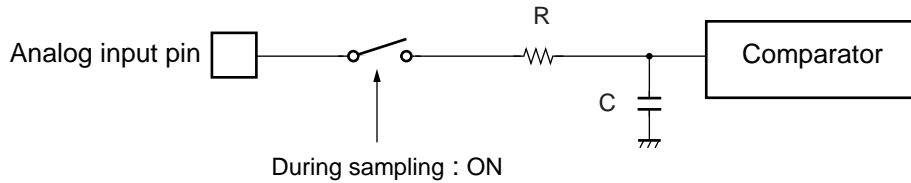
| Parameter | Symbol | Value | | | Unit | Remarks |
|----------------------------------|------------------|-------------------|-------------------|-------------------|------|--|
| | | Min | Typ | Max | | |
| Resolution | — | — | — | 10 | bit | |
| Total error | | -3.0 | — | +3.0 | LSB | |
| Linearity error | | -2.5 | — | +2.5 | LSB | |
| Differential linear error | | -1.9 | — | +1.9 | LSB | |
| Zero transition voltage | V _{OT} | AVss - 1.5 LSB | AVss + 0.5 LSB | AVss + 2.5 LSB | V | FLASH product : 2.7 V ≤ AVcc ≤ 3.3 V MASK product : 2.7 V ≤ AVcc ≤ 3.6 V |
| | | AVss - 0.5 LSB | AVss + 1.5 LSB | AVss + 3.5 LSB | V | 1.8 V ≤ AVcc < 2.7 V |
| Full-scale transition voltage | V _{FST} | AVcc - 3.5 LSB | AVcc - 1.5 LSB | AVcc + 0.5 LSB | V | FLASH product : 2.7 V ≤ AVcc ≤ 3.3 V MASK product : 2.7 V ≤ AVcc ≤ 3.6 V |
| | | AVcc - 2.5 LSB | AVcc - 0.5 LSB | AVcc + 1.5 LSB | V | 1.8 V ≤ AVcc < 2.7 V |
| Compare time | — | 0.6 | — | 16,500 | μs | FLASH product : 2.7 V ≤ AVcc ≤ 3.3 V MASK product : 2.7 V ≤ AVcc ≤ 3.6 V |
| | | 20 | — | 16,500 | μs | 1.8 V ≤ AVcc < 2.7 V |
| Sampling time | — | 0.4 | — | ∞ | μs | FLASH product : 2.7 V ≤ AVcc ≤ 3.3 V MASK product : 2.7 V ≤ AVcc ≤ 3.6 V external impedance < at 1.8 kΩ |
| | | 30 | — | ∞ | μs | 1.8 V ≤ AVcc < 2.7 V external impedance < at 14.8 kΩ |
| Analog input current | I _{AIN} | -0.3 | — | 0.3 | μA | |
| Analog input voltage range | V _{AIN} | AVss | — | AVcc | V | |
| Reference voltage | — | AVss + 1.8 | — | AVcc | V | AVcc pin |
| Reference voltage supply current | I _R | — | 400 | 600 | μA | AVcc pin, During A/D operation |
| | I _{RH} | — | — | 5 | μA | AVcc pin, at stop mode |

(2) Notes on Using A/D Converter

• About the external impedance of analog input and its sampling time

- A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

• Analog input circuit model

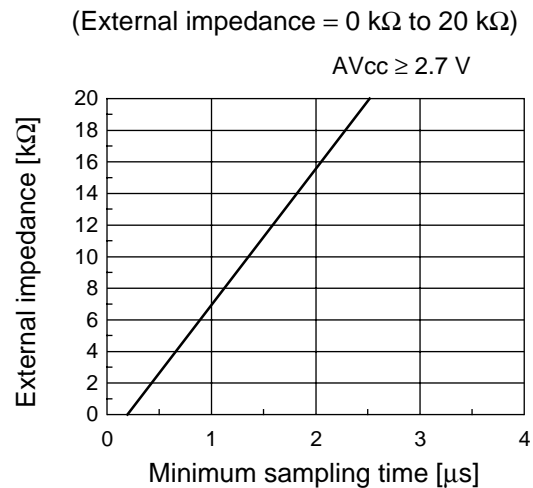
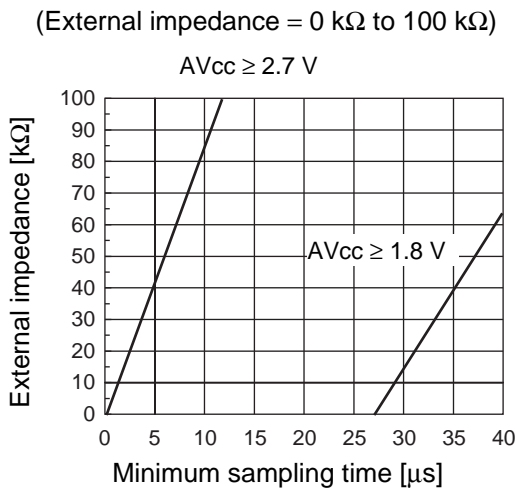


| | R | C |
|---|----------------------|---------------|
| $2.7\text{ V} \leq AV_{CC} \leq 3.6\text{ V}$ | 1.7 k Ω (Max) | 14.5 pF (Max) |
| $1.8\text{ V} \leq AV_{CC} < 2.7\text{ V}$ | 84 k Ω (Max) | 25.2 pF (Max) |

Note : The values are reference values.

- To satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.

• The relationship between external impedance and minimum sampling time



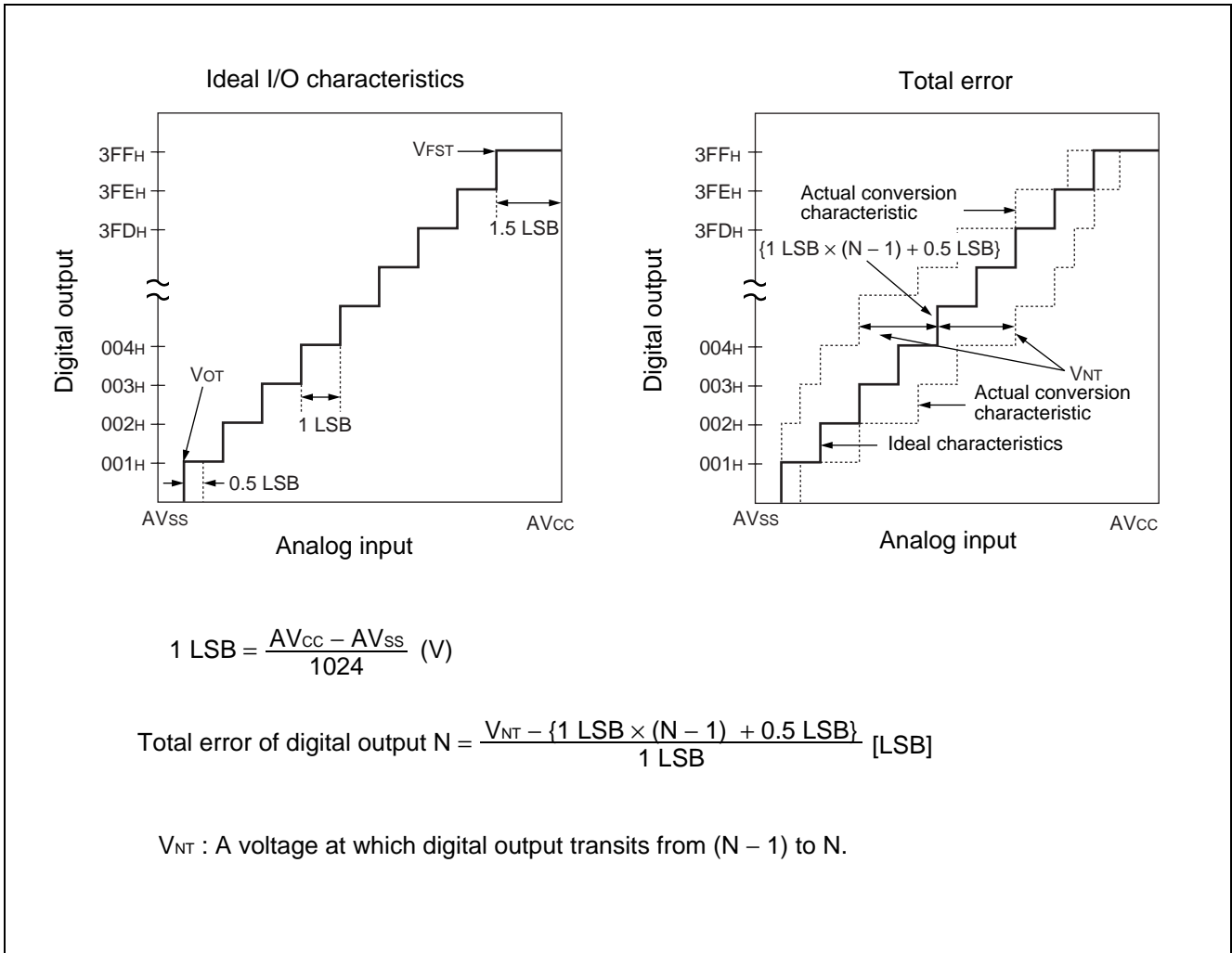
- If the sampling time cannot be sufficient, connect a capacitor of about 0.1 μF to the analog input pin.

• About errors

As $|AV_{CC} - AV_{SS}|$ becomes smaller, values of relative errors grow larger.

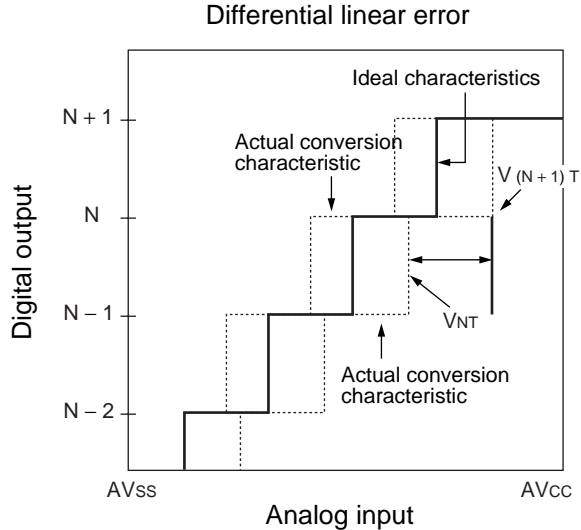
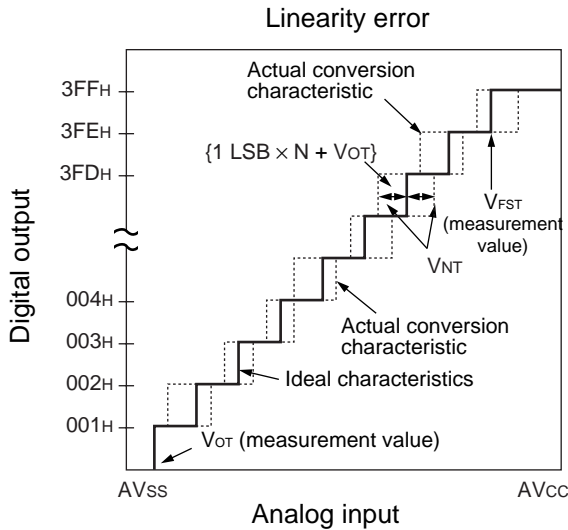
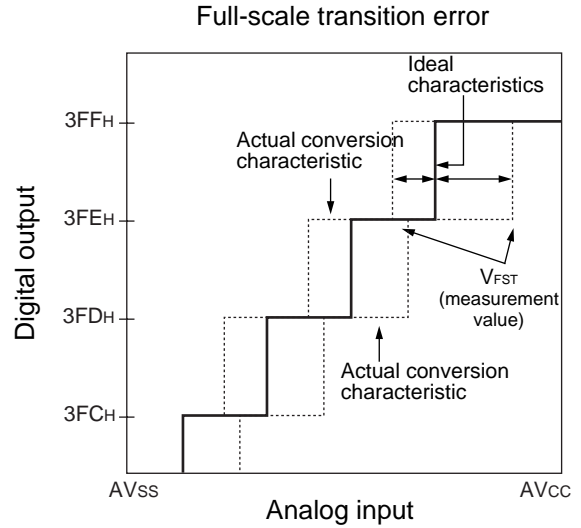
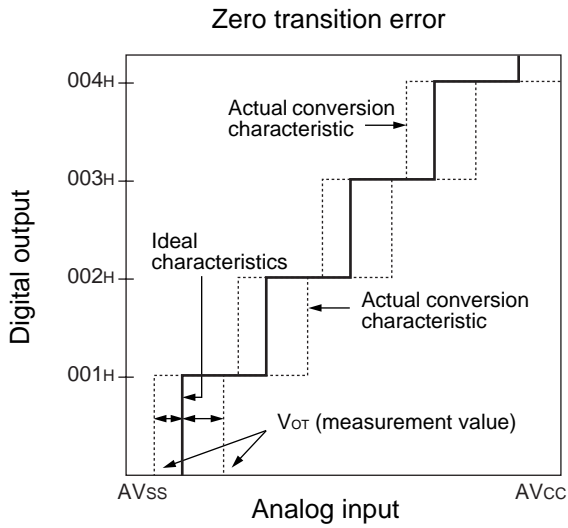
(3) Definition of A/D Converter Terms

- Resolution
The level of analog variation that can be distinguished by the A/D converter.
When the number of bits is 10, analog voltage can be divided into $2^{10} = 1024$.
- Linearity error (unit : LSB)
The deviation between the value along a straight line connecting the zero transition point (“00 0000 0000” ← → “00 0000 0001”) of a device and the full-scale transition point (“11 1111 1111” ← → “11 1111 1110”) compared with the actual conversion values obtained.
- Differential linear error (Unit : LSB)
Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
- Total error (unit: LSB)
Difference between actual and theoretical values, caused by a zero transition error, full-scale transition error, linearity error, quantum error, and noise.



(Continued)

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$$\text{Linear error in digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times N + V_{OT}\}}{1 \text{ LSB}}$$

$$\text{Differential linear error in digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1$$

V_{NT} : A voltage at which digital output transits from (N - 1) to N.

V_{OT} (Ideal value) = $AV_{SS} + 0.5 \text{ LSB}$ [V]

V_{FST} (Ideal value) = $AV_{CC} - 1.5 \text{ LSB}$ [V]

MB95110A Series

6. Flash Memory Program/Erase Characteristics

| Parameter | Value | | | Unit | Remarks |
|--|------------------|-------------------|------------------|-------|--|
| | Min | Typ | Max | | |
| Sector erase time (4 Kbytes sector) | — | 0.2* ¹ | 3* ² | s | Excludes 00 _H programming prior erasure |
| Sector erase time (16 Kbytes sector) | — | 0.5* ¹ | 12* ² | s | Excludes 00 _H programming prior erasure |
| Byte programming time | — | 32 | 3600 | μs | Excludes system-level overhead |
| Erase/program cycle | 10,000 | — | — | cycle | |
| Power supply voltage at erase/program | 2.7 | — | 3.3 | V | |
| Flash data retention time | 20* ³ | — | — | year | Average T _A = +85 °C |

*1 : T_A = +25 °C, V_{CC} = 3.0 V, 10,000 cycles

*2 : T_A = +85 °C, V_{CC} = 2.7 V, 10,000 cycles

*3 : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C) .

■ MASK OPTIONS

| No | Part number | MB95116A | MB95F118AS | MB95F118AW | MB95FV100A-101 |
|----|--|---|---|---|---|
| | Specifying procedure | Specify when ordering MASK | Setting disabled | Setting disabled | Setting disabled |
| 1 | Clock mode select • Single-system clock mode • Dual-system clock mode | Selectable | Single-system clock mode | Dual-system clock mode | Changing by the switch on MCU board |
| 2 | Selection of oscillation stabilization wait time • Selectable the initial value of main clock oscillation stabilization wait time | Selectable 1 : $(2^2 - 2) / F_{CH}$ 2 : $(2^{12} - 2) / F_{CH}$ 3 : $(2^{13} - 2) / F_{CH}$ 4 : $(2^{14} - 2) / F_{CH}$ | Fixed to oscillation stabilization wait time of $(2^{14}-2) / F_{CH}$ | Fixed to oscillation stabilization wait time of $(2^{14}-2) / F_{CH}$ | Fixed to oscillation stabilization wait time of $(2^{14}-2) / F_{CH}$ |

■ ORDERING INFORMATION

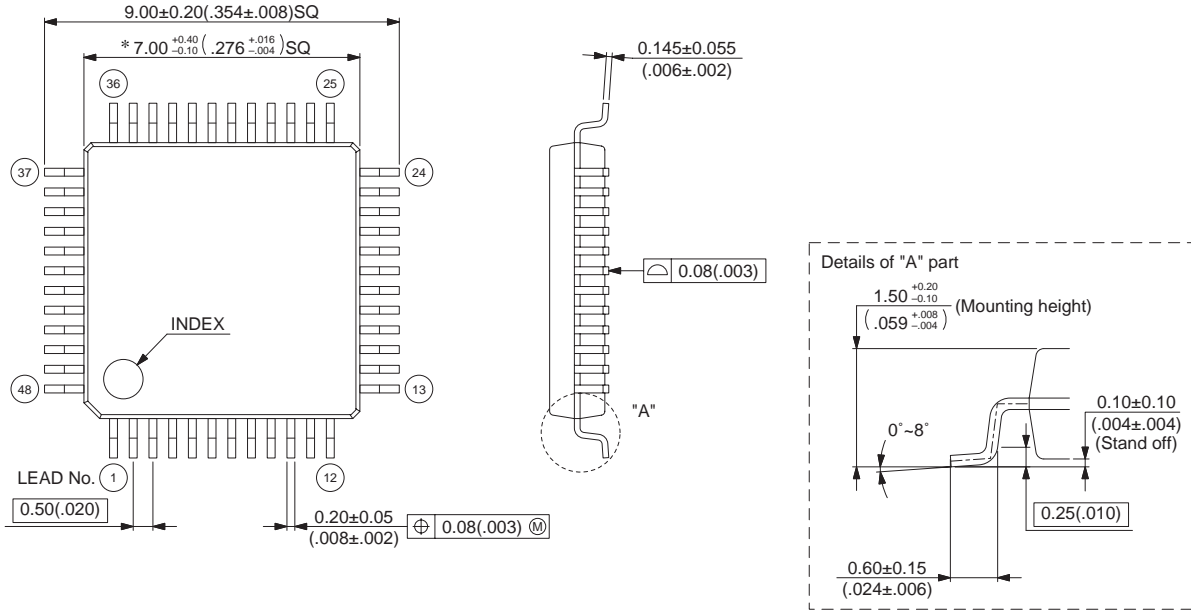
| Part number | Package | Remarks |
|---|--|---------|
| MB95116APV MB95F118ASPV MB95F118AWPV | 48-pin plastic BCC (LCC-48P-M09) | |
| MB95116APMT MB95F118ASPMT MB95F118AWPMT | 48-pin plastic LQFP (FPT-48P-M26) | |
| MB2146-301 (MB95FV100A-101PBT) | MCU board (244-pin plastic PFBGA) (BGA-244P-M08) | |

MB95110A Series

(Continued)

48-pin plastic LQFP
(FPT-48P-M26)

Note 1) * : These dimensions do not include resin protrusion.
 Note 2) Pins width and pins thickness include plating thickness.
 Note 3) Pins width do not include tie bar cutting remainder.



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Dimensions in mm (inches).
 Note: The values in parentheses are reference values.

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