

Structure Silicon Monolithic Integrated Circuit

Product Name Luminous Control IC

Type **BD6092GU**

Features
 Photo Sensor Interface
 Auto Luminous Control
 LED Driver Control by PWM Output

○Absolute Maximum Ratings (Ta=25 °C)

Parameter	Symbol	Limits	Unit	Condition
Maximum Applied voltage	VMAX	7	V	
Power Dissipation	Pd	1250	mW	
Operating Temperature Range	Topr	-40 ~ +85	°C	
Storage Temperature Range	Tstg	-55 ~ +150	°C	

note) Power dissipation deleting is 10.0mW/°C, when it's used in over 25 °C.

(It's deleting is on the board that is ROHM's standard)

○Operating conditions (VBAT≥VIO, Ta=-40~85 °C)

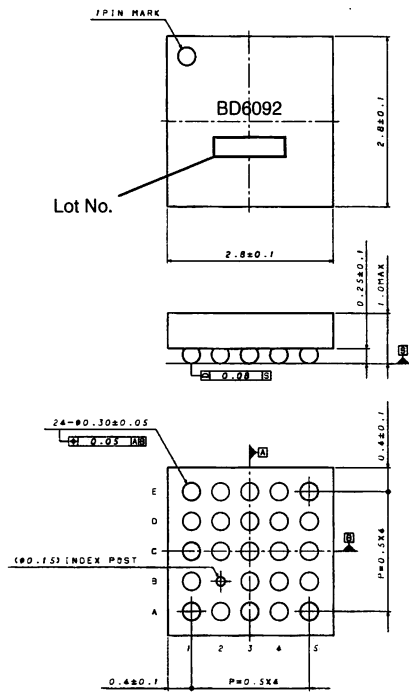
Parameter	Symbol	Limits	Unit	Condition
VBAT input voltage	VBAT1, 2	2.7~5.5	V	
VIO pin voltage	VIO	1.65~3.3	V	

*This chip is not designed to protect itself against radioactive rays.

○Electrical Characteristics (Unless otherwise specified, Ta=25°C, VBAT1,2=3.6V, VIO=1.8V)

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Circuit Current						
VBAT Circuit current 1	IBAT1	-	0.1	3.0	μA	RESETB=0V, VIO=0V
VBAT Circuit current 2	IBAT2	-	0.5	3.0	μA	RESETB=0V, VIO=1.8V
VBAT Circuit current 3	IBAT3	-	0.17	1.0	mA	ALC mode ADCYC=0.5s setting Except sensor current
Sensor Interface						
SBIAS Output voltage	VoS	2.85	3.0	3.15	V	Io=200μA
		2.47	2.6	2.73	V	Io=200μA
SBIAS Maximum Output current	IomaxS	30	-	-	mA	Vo=2.6V setting
SBIAS Discharge resistor at OFF	ROFFS	-	1.0	1.5	kΩ	
SSENS Input voltage range	VISS	0	-	VoS × 255/256	V	
ADC Resolution	ADRES	8			bit	
ADC Integral Non-linearity	ADINL	-3	-	+3	LSB	
ADC Differential Non-linearity	ADDNL	-1	-	+1	LSB	
Oscillator						
Oscillator frequency	FOSC	0.8	1.0	1.2	MHz	
UVLO						
UVLO Detect voltage	VUVLO1	1.5	1.95	-	V	At VBAT decreasing
UVLO Release voltage	VUVLO2	-	2.15	2.65	V	At VBAT Increasing
UVLO Release voltage hysteresis	UVLOHYS	50	200	-	mV	
SDA, SCL (I²C Interface)						
L Level Input voltage	VILI	-0.3	-	0.25 × VIO	V	
H Level Input voltage	VIHI	0.75 × VIO	-	VBAT+0.3	V	
Hysteresis of schmitt trigger Input	Vhysl	0.05 × VIO	-	-	V	
L Level Output voltage	VOLI	-	-	0.3	V	SDA, IOL=3mA
Input current	Iinl	-10	-	10	μA	Input voltage= 0.1×VIO~0.9×VIO
RESETB, EXPWMIN (CMOS Input)						
L Level Input voltage	VIL	-0.3	-	0.25 × VIO	V	
H Level Input voltage	VIH	0.75 × VIO	-	VBAT+0.3	V	
Input current	Iin	-10	-	10	μA	Input voltage = 0.1×VIO~0.9×VIO
PWM Input frequency range	fpwm	-	-	1000	kHz	PWMIN, Duty=50% Input
DCDCOK (CMOS Input)						
L Level Input voltage	VIL	-0.3	-	0.25 × VIO	V	
H Level Input voltage	VIH	0.75 × VIO	-	VBAT+0.3	V	
Input current	Iin	-10	-	10	μA	Input voltage = 0.1×VIO~0.9×VIO
PWMOUT (CMOS Output)						
L Level Output voltage	VOLPW	-	-	0.2	V	IOL=1mA
H Level Output voltage	VOHPW	VIO - 0.2	-	-	V	IOH=1mA
Output Duty Resolution	DTYRES	8			bit	
GC1, GC2 (Sensor Gain Control CMOS Output)						
L Level Output voltage	VOLGC	-	-	0.2	V	IOL=1mA
H Level Output voltage	VOHGC	VoS - 0.2	-	-	V	IOH=1mA

External dimensions

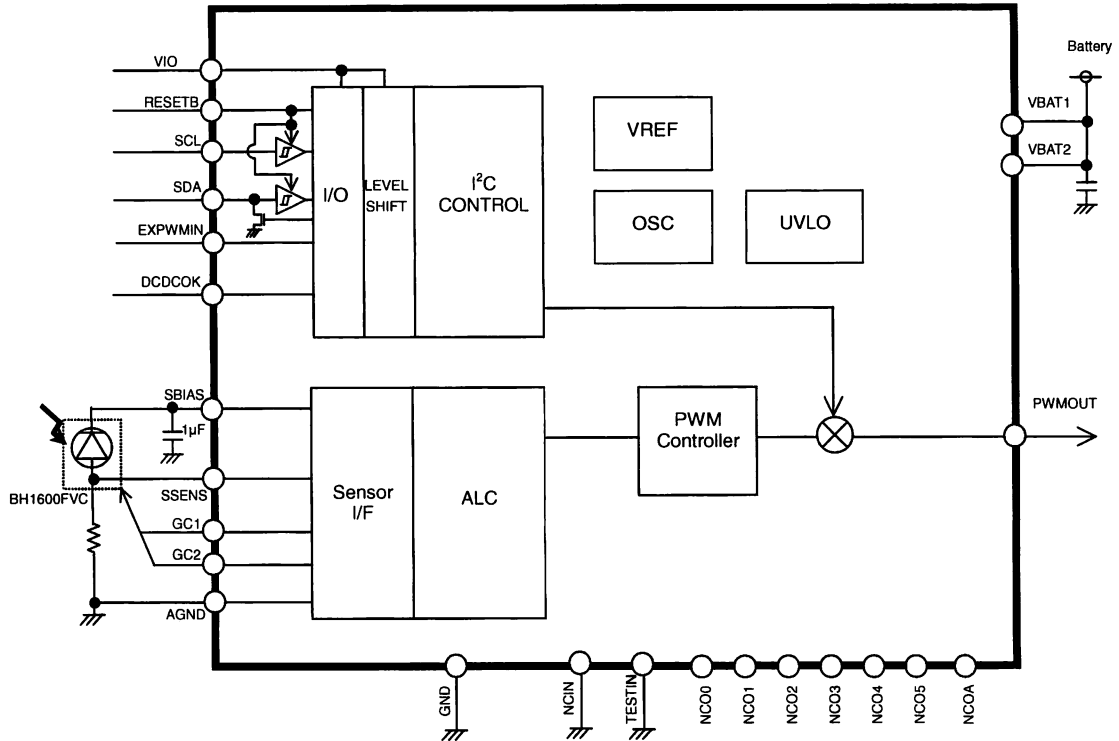


VCSP85H2 (24pins) (Unit:mm)

Terminals

PIN	PIN Name	PIN	PIN Name
B1	VBAT1	C4	EXPWMIN
B3	VBAT2	E4	PWMOUT
A3	GND	E3	DCDCOK
D2	AGND	A2	TESTIN
C5	VIO	E1	NCIN
A4	RESETB	D3	NCO0
D5	SDA	E5	NCO1
D4	SCL	C3	NCO2
D1	SBIAS	A5	NCO3
E2	SSENS	B5	NCO4
C1	GC1	B4	NCO5
C2	GC2	A1	NCOA

Block diagram



○Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Power supply and ground line

Design PCB pattern to provide low impedance for the wiring between the power supply and the ground lines. Pay attention to the interference by common impedance of layout pattern when there are plural power supplies and ground lines. Especially, when there are ground pattern for small signal and ground pattern for large current included the external circuits, please separate each ground pattern. Furthermore, for all power supply pins to ICs, mount a capacitor between the power supply and the ground pin. At the same time, in order to use a capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(3) Ground voltage

Make setting of the potential of the ground pin so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no pins are at a potential lower than the ground voltage including an actual electric transient.

(4) Short circuit between pins and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between pins or between the pin and the power supply or the ground pin, the ICs can break down.

(5) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(6) Input pins

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input pin. Therefore, pay thorough attention not to handle the input pins, such as to apply to the input pins a voltage lower than the ground respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input pins a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(7) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(8) Thermal design

Perform thermal design in which there are adequate margins by taking into account the permissible dissipation (Pd) in actual states of use.

(9) LDO

Use each output of LDO by the independence. Don't use under the condition that each output is short-circuited because it has the possibility that an operation becomes unstable.

(10) About the pin for the test, the un-use pin

Prevent a problem from being in the pin for the test and the un-use pin under the state of actual use. Please refer to a function manual and an application notebook. And, as for the pin that doesn't specially have an explanation, ask our company person in charge.

(11) About the rush current

For ICs with more than one power supply, it is possible that rush current may flow instantaneously due to the internal powering sequence and delays. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of wiring.

(12) About the function description or application note or more.

The function description and the application notebook are the design materials to design a set. So, the contents of the materials aren't always guaranteed. Please design application by having fully examination and evaluation include the external elements.

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