

# Am29520A/Am29521A

## Multilevel Pipeline Registers

### DISTINCTIVE CHARACTERISTICS

- Four 8-bit wide registers
- Provides temporary storage for data/instruction delay/queuing
- Single 4 level or dual 2 level structure
- High-speed IMOX™ ECL internal technology, TTL compatible I/O
- All 4 registers available at three state output
- 24 pin slim (0.3") DIP packages
- 28 pin chip carrier packages

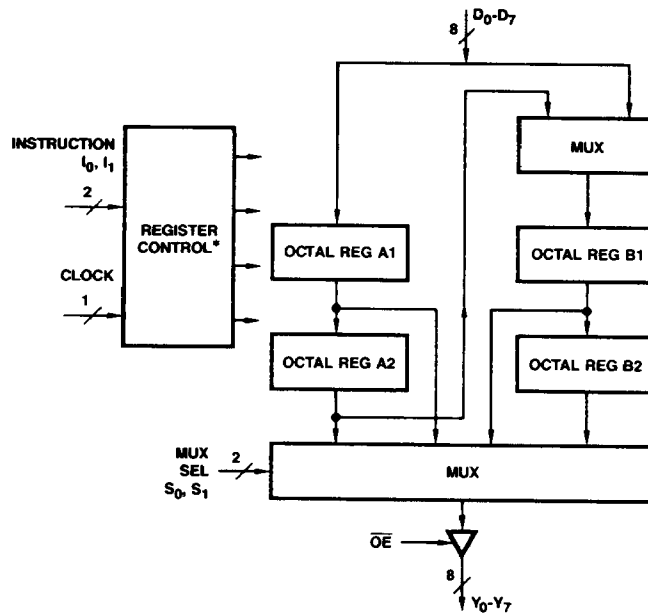
### GENERAL DESCRIPTION

The Am29520A and Am29521A are high speed, dual stack, register files that differ only in the way data is loaded (see Table 1). Both devices contain four 8-bit wide registers whose flexible architecture lends itself to virtually any system. The high output drive allows layout of the devices directly on the system bus for bit slice and array or digital signal processing applications.

In the Am29520A, data may be microprogrammed to cascade through the 4 registers in push-down pattern, no-op to hold data in the registers, or push-down data through one 2 level stack while holding data in the other stack.

The Am29521A also has the cascadable 4 register push-down and no-op features. It can also be microprogrammed to write over the first level register of one stack, while holding data in the other 3 registers.

### BLOCK DIAGRAM



BDR02270

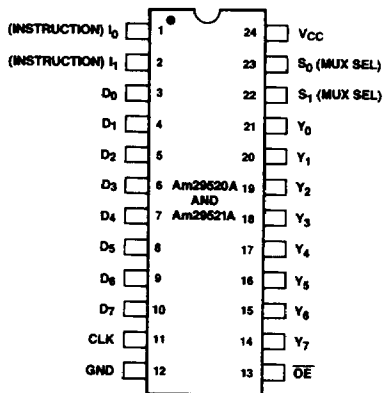
\*Multilevel Pipeline Register

## RELATED PRODUCTS

Part No.	Description
Am29540	FFT Address Sequencer
Am29116	16-bit Bipolar Microprocessor
Am29325	32-bit Floating Point Processor
Am29517A	16 x 16-bit Multiplier
Am29501	8-bit Multi-Port Pipeline Microprocessor
Am29C509	12 x 12 MAC
Am6108	8-bit A/D Converter
Am9128	2K x 8 Static RAM
Am21L47	4K x 1 Static RAM
Am29524	Dual 7 Deep Pipeline Register with 0 and Feedthrough

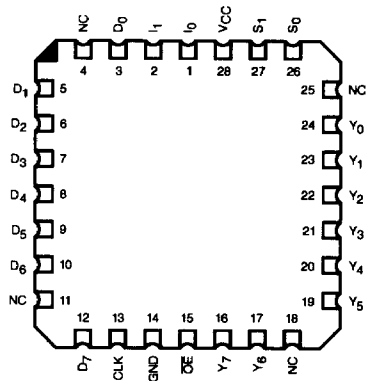
## CONNECTION DIAGRAM Top View

**CD3024  
PD3024**



CDR04471

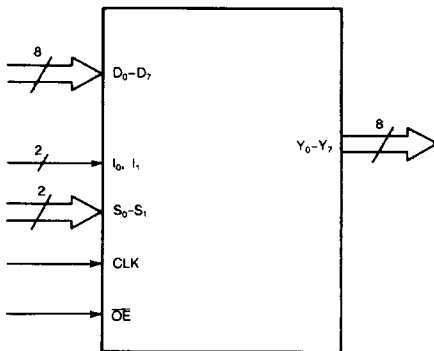
**CL 028  
PL 028**



CD010120

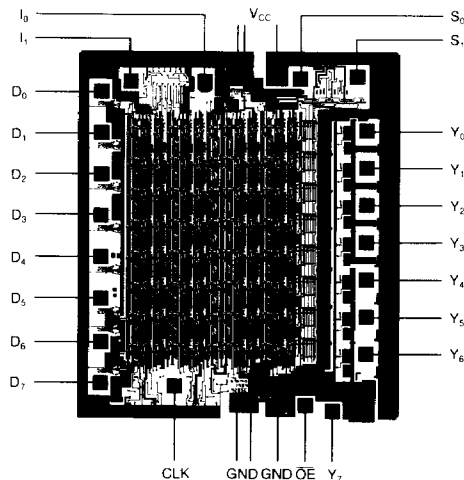
Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL



LS002301

### METALLIZATION AND PAD LAYOUT



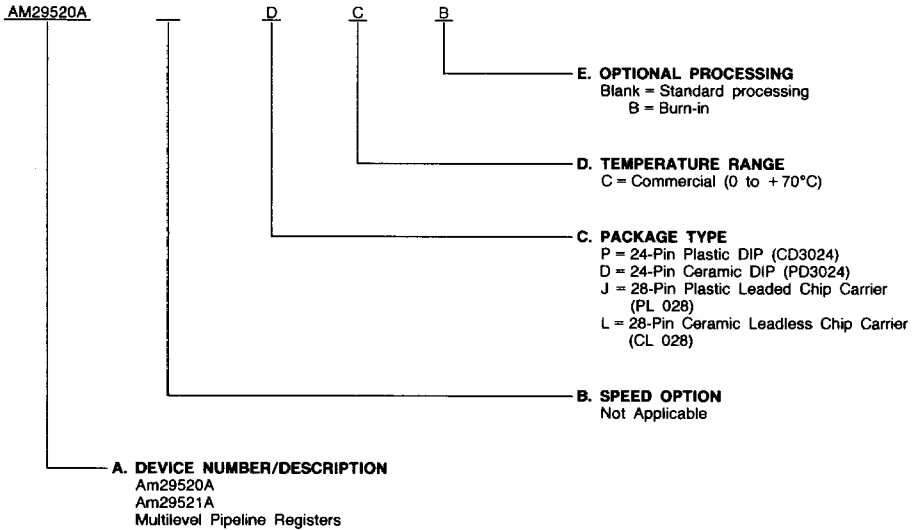
DIE SIZE: 0.117" x 0.133"  
Approximate Gate Count = 362

# ORDERING INFORMATION

## Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- A. Device Number**
- B. Speed Option** (if applicable)
- C. Package Type**
- D. Temperature Range**
- E. Optional Processing**



Valid Combinations	
AM29520A	DC, DCB, PC, PCB, LC, JC
AM29521A	DC, DCB, PC, PCB, LC, JC

### Valid Combinations

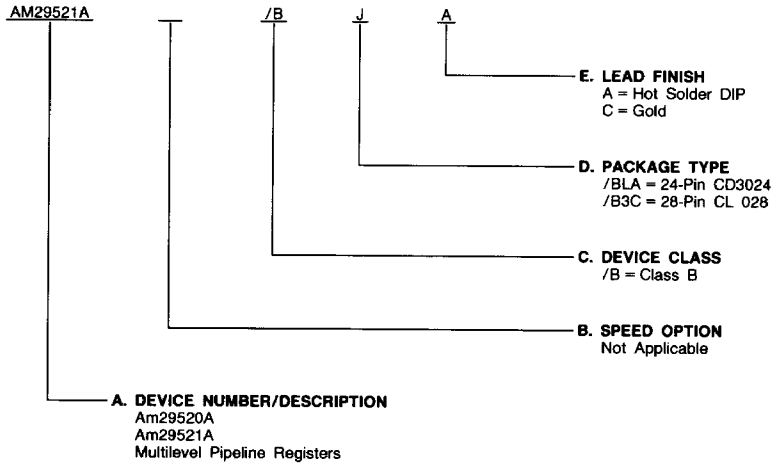
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

# ORDERING INFORMATION

## APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of:

- A. Device Number**
- B. Speed Option** (if applicable)
- C. Device Class**
- D. Package Type**
- E. Lead Finish**



### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Valid Combinations	
AM29520A	BLA, B3C
AM29521A	BLA, B3C

## PIN DESCRIPTION

**D<sub>0</sub> - D<sub>7</sub> Register Input Port (Input, Active HIGH)**

Data to be written to the internal registers is input via this port.

**Y<sub>0</sub> - Y<sub>7</sub> Register Output Port (Output, Three-State)**

Data to be read out of any of the internal registers is output via this three-state port.

**I<sub>0</sub>, I<sub>1</sub> Instruction Inputs (Input, Active HIGH)**

Operational control of the device is determined by these inputs. See Tables 1 and 2 for details.

**S<sub>0</sub>, S<sub>1</sub> Register Output Select (Input, Active HIGH)**

These inputs select which register appears on the Register Output Port. See Table 3 for details.

**CLK Clock (Input)**

The rising edge of the clock loads data into the appropriate registers as determined by the Instruction Inputs.

**OE Output Enable (Input, Active LOW)**

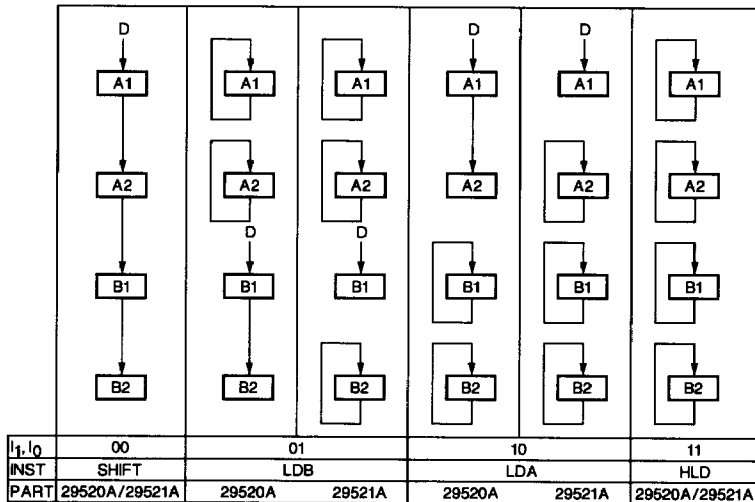
When LOW, the register selected by the Register Output Select Inputs appears on the Register Output Port. When HIGH, the Register Output Port is three-stated.

## FUNCTIONAL DESCRIPTION

The following tables describe the operation of the Am29520A/29521A. Table 1 illustrates register operation in response to instruction inputs I<sub>0</sub> and I<sub>1</sub>. Note that in the Am29521A, Instructions "LDB" and "LDA" write over register B<sub>1</sub> or A<sub>1</sub>

respectively, and hold resident data in the other 3 registers. The Am29520A instead pushes data down the two level stack. Table 2 gives the operand values corresponding to the operations illustrated in Table 1. Table 3 gives the Register Output Select codes required to access a specific register, which then appears at the Register Output Port.

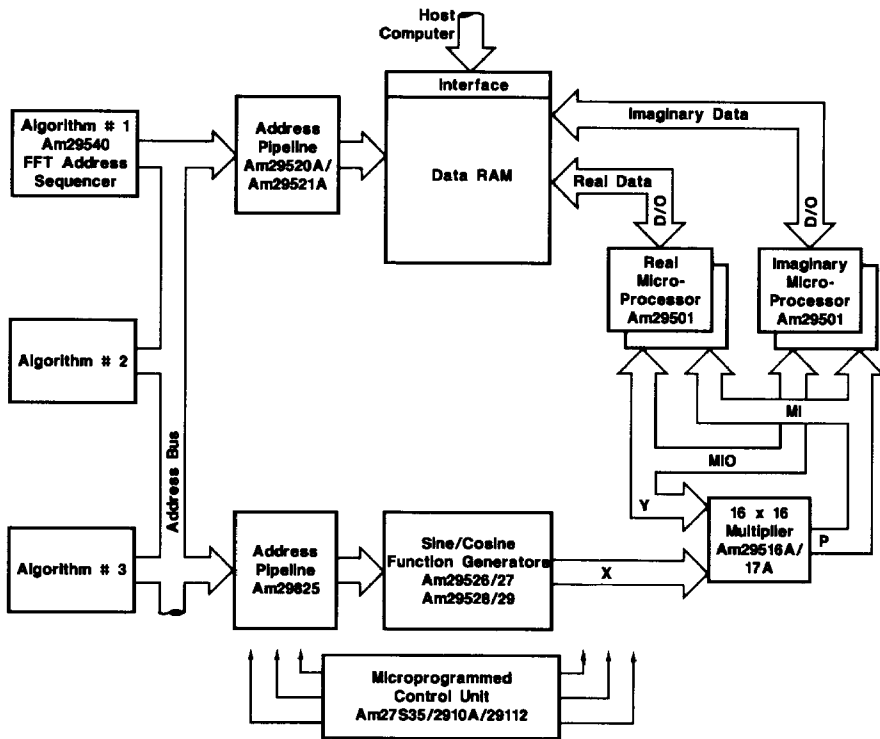
### Am29520A/29521A INSTRUCTIONS



TB000240

**TABLE 1. REGISTER LOAD OPERATIONS**  
(See Table 2 for instruction codes)

# Am29500 PROCESSOR



BD002712

Mnemonic	Inputs		Description	
	I <sub>1</sub>	I <sub>0</sub>	Am29520A Only	Am29521A Only
Shift	0	0	Push A & B	Push A & B
LDB	0	1	Push B	Write Over B <sub>1</sub>
LDA	1	0	Push A	Write Over A <sub>1</sub>
HLD	1	1	No-Op	No-Op

TABLE 2. INSTRUCTION SET DESCRIPTIONS

S0	S1	Y0 - Y7
1	1	A <sub>1</sub>
1	0	A <sub>2</sub>
0	1	B <sub>1</sub>
0	0	B <sub>2</sub>

TABLE 3. SELECT OPERATION DESCRIPTIONS &vc<2>

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature .....	-65 to +150°C
Temperature Under Bias- $T_C$ .....	-55 to +125°C
Supply Voltage to Ground Potential	
Continuous .....	-0.5 to +7.0V
DC Voltage Applied to Outputs For	
High Output State .....	-0.5V to + $V_{CC}$ max
DC Input Voltage .....	-0.5 to +5.5V
DC Output Current, Into Outputs .....	30mA
DC Input Current .....	-30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## OPERATING RANGES

Commercial (C) Devices	
Temperature .....	$T_A = 0^\circ\text{C}$ to +70°C
Supply Voltage .....	+4.75 V to +5.25 V
Military (M) Devices	
Temperature .....	$T_C = -55^\circ\text{C}$ to +125°C
Supply Voltage .....	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

## DC CHARACTERISTICS over operating range unless otherwise specified

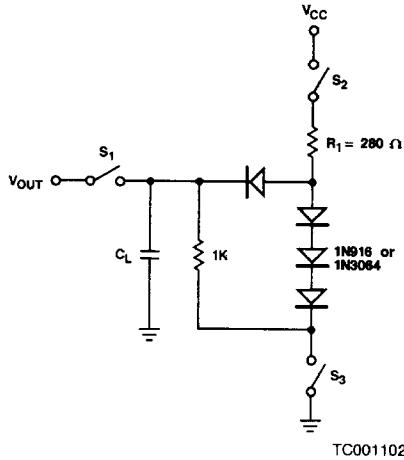
Parameters	Description	Test Conditions (Note 1)		Min.	Max.	Units
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{MIN}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -6.5 \text{ mA (COM'L)}$	2.4		Volts
			$I_{OH} = -2.0 \text{ mA (MIL)}$	2.4		
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{MIN}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 12 \text{ mA}$		0.45	Volts
			$I_{OL} = 20 \text{ mA}$		0.50	
$V_{IH}$	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0		Volts
$V_{IL}$	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
$V_I$	Input Clamp Voltage	$V_{CC} = \text{MIN}$ , $I_{IN} = -18 \text{ mA}$			-1.2	Volts
$I_{IL}$	Input LOW Current	$V_{CC} = \text{MAX}$ , $V_{IN} = 0.5\text{V}$	OE		-2.0	mA
			Other Inputs		-0.4	
$I_{IH}$	Input HIGH Current	$V_{CC} = \text{MAX}$ , $V_{IN} = 2.7\text{V}$			50	$\mu\text{A}$
$I_I$	Input HIGH Current	$V_{CC} = \text{MAX}$ , $V_{IN} = 5.5 \text{ V}$			1.0	mA
$I_{OZH}$ $I_{OZL}$	Off State (High Impedance)	$V_{CC} = \text{MAX}$		$V_O = 2.7 \text{ V}$	50	$\mu\text{A}$
	Output Current			$V_O = 0.5 \text{ V}$	-50	
$I_{SC}$	Output Short Circuit Current (Note 2)	$V_{CC} = \text{MAX}$		-30	-100	mA
$I_{CC}$	Power Supply Current (Note 3)	COM'L Only	$V_{CC} = \text{MAX}$	$T_A = 0$ to +70°C	185	mA
				$T_A = +70^\circ\text{C}$	155	
		MIL Only	$V_{CC} = \text{MAX}$	$T_C = -55$ to +125°C	200	
				$T_C = +125^\circ\text{C}$	150	

- Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.  
 2. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.  
 3. All inputs LOW.

**SWITCHING CHARACTERISTICS** over operating range unless otherwise specified

No.	Parameters Symbols		Parameter Description	Test Conditions	COMMERCIAL		MILITARY		Units	
					Min.	Max.	Min.	Max.		
1	t <sub>PD</sub>	t <sub>PLH</sub>	Clock to Data Output	R <sub>L</sub> = 280Ω C <sub>L</sub> = 50pF		21		24	ns	
		t <sub>PHL</sub>				22		24		
2	t <sub>PDSEL</sub>	t <sub>PLH</sub>	S <sub>0</sub> , S <sub>1</sub> to Data Output			20		22	ns	
		t <sub>PHL</sub>				20		22		
3	t <sub>S</sub>		Input Data to Clock				10		ns	
4	t <sub>H</sub>					3		3		
5	t <sub>S</sub>		Instruction (Register Enable) to Clock				10		ns	
6	t <sub>H</sub>					3		3		
7	t <sub>PHZ</sub>		OE to Output		C <sub>L</sub> = 5 pF		13		14	ns
8	t <sub>PLZ</sub>		OE to Output		C <sub>L</sub> = 5 pF		15		16	ns
9	t <sub>PZH</sub>		OE to Output		R <sub>L</sub> = 280 Ω C <sub>L</sub> = 50 pF		20		22	ns
10	t <sub>PZL</sub>		OE to Output					21		22
11	t <sub>PWH</sub>		Clock Pulse Width HIGH			10		10		ns
12	t <sub>PWL</sub>		Clock Pulse Width LOW		10		10		ns	

**SWITCHING TEST CIRCUITS**

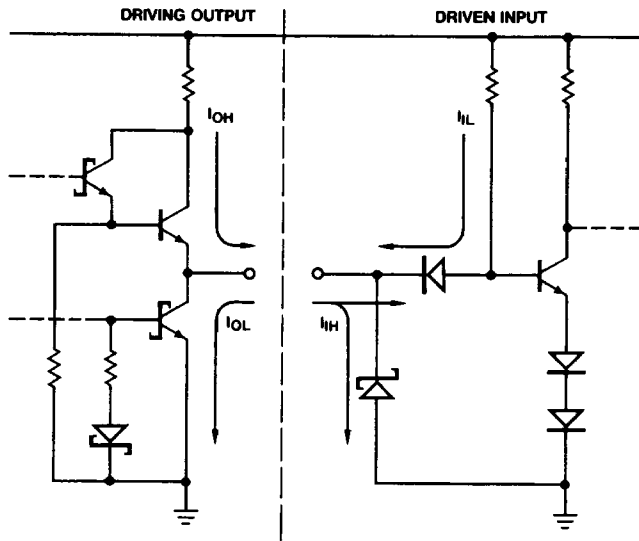


**Three-State Outputs**

- Notes: 1. C<sub>L</sub> = 50 pF includes scope probe, wiring and stray capacitances without device in test fixture.
- 2. S<sub>1</sub>, S<sub>2</sub>, S<sub>3</sub> are closed during function tests and all AC tests except output enable tests.
- 3. S<sub>1</sub> and S<sub>3</sub> are closed while S<sub>2</sub> is open for t<sub>PZH</sub> test.  
S<sub>1</sub> and S<sub>2</sub> are closed while S<sub>3</sub> is open for t<sub>PZL</sub> test.
- 4. C<sub>L</sub> = 5.0 pF for output disable tests.



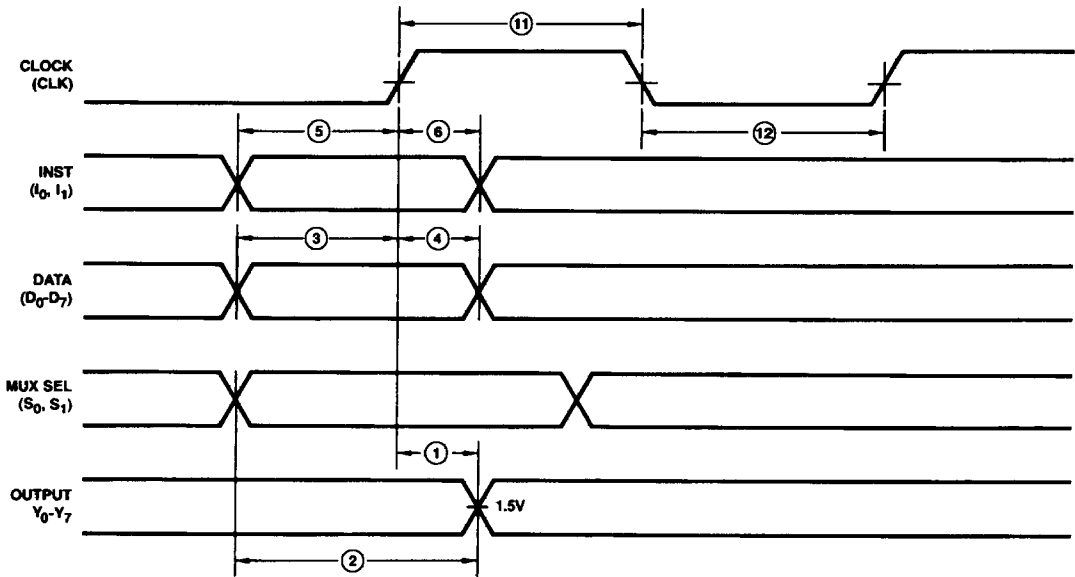
# INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



ICR00510

## SWITCHING WAVEFORMS

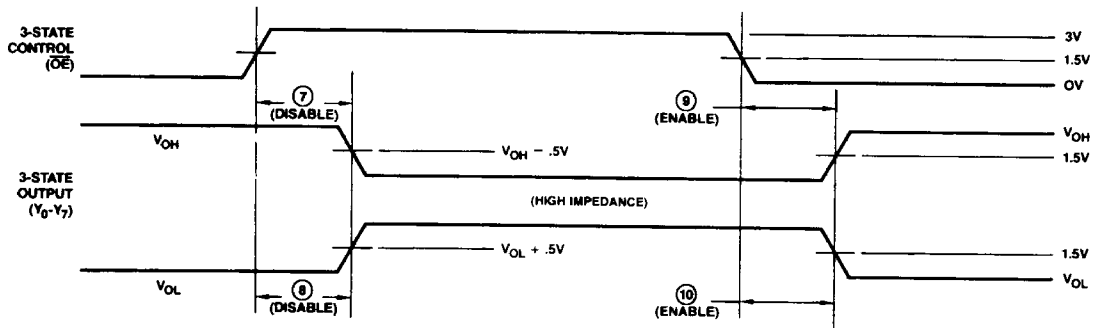
Am29520A/Am29521A



WFR02934

## SWITCHING WAVEFORMS (Cont'd.)

### THREE STATE TIMING Am29520A/Am29521A



WFR02942

### Test Philosophy and Methods

The following points give the general philosophy that we apply to tests that must be properly engineered if they are to be implemented in an automatic testing environment. The specifics of what philosophies are applied to which test are shown in the data sheet and the data-sheet reconciliation that follow.

#### Capacitive Loading for AC Testing

Automatic testers and their associated hardware have stray capacitance that varies from one type of tester to another, but is generally around 50 pF. This, of course, makes it impossible to make direct measurements of parameters that call for smaller capacitive load than the associated stray capacitance. Typical examples of this are the so-called "float delays" that measure the propagation delays in to and out of the high-impedance state and are usually specified at a load capacitance of 5.0 pF. In these cases, the test is performed at the higher load capacitance (typically 50 pF) and engineering correlations based on data taken with a bench set up are used to determine the result at the lower capacitance.

Similarly, a product may be specified at more than one capacitive load. Since the typical automatic tester is not capable of switching loads in mid-test, it is impractical to make measurements at both capacitances even though they may both be greater than the stray capacitance. In these cases, a measurement is made at one of the two capacitances. The result at the other capacitance is determined from engineering correlations based on data taken with a bench setup and the knowledge that certain DC tests are performed in order to facilitate this correlation.

AC loads specified in the data sheet are used for bench testing. Automatic tester loads, which simulate the data-sheet loads, may be used during production testing.

#### Threshold Testing

The noise associated with automatic testing, the long inductive cables, and the high gain of bipolar devices frequently give rise to oscillations when testing high-speed circuits. These oscillations are not indicative of a reject device, but instead, of an overtaxed system. To minimize this problem, thresholds are tested at least once for each input pin. Thereafter, "hard" high and low levels are used for other tests. Generally this means that function and AC testing are performed at "hard" input levels.

#### AC Testing

AC parameters are specified that cannot be measured accurately on automatic testers because of tester limitations. Data-input hold times fall into this category. In these cases, the parameter in question is tested by correlating the tester to bench data or oscilloscope measurements made on the tester by engineering (supporting data on file).

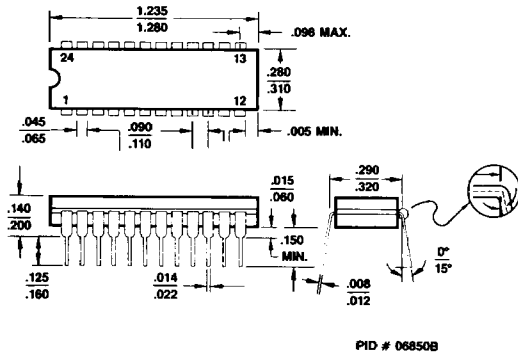
Certain AC tests are redundant since they can be shown to be predicted by other tests that have already been performed. In these cases, the redundant tests are not performed.

#### Output Short-Circuit Current Testing

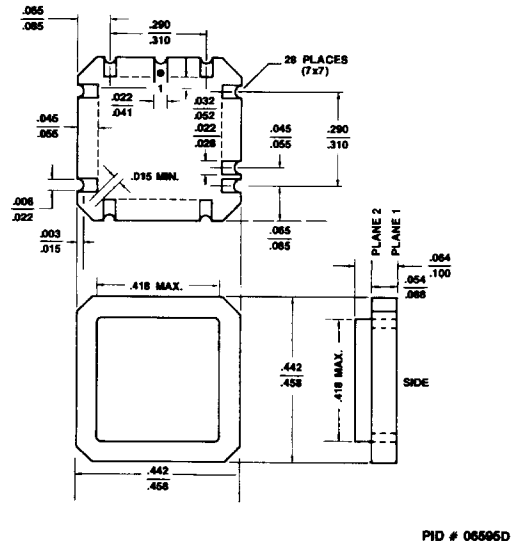
When performing I<sub>OS</sub> tests on devices containing RAM or registers, great care must be taken that undershoot caused by grounding the high-state output does not trigger parasitic elements which in turn cause the device to change state. In order to avoid this effect, it is common to make the measurement at a voltage (V<sub>output</sub>) that is slightly above the ground. The V<sub>CC</sub> is raised by the same amount so that the result (as confirmed by Ohm's law and precise bench testing) is identical to the V<sub>OUT</sub> = 0, V<sub>CC</sub> = Max. case.

PHYSICAL DIMENSIONS\*

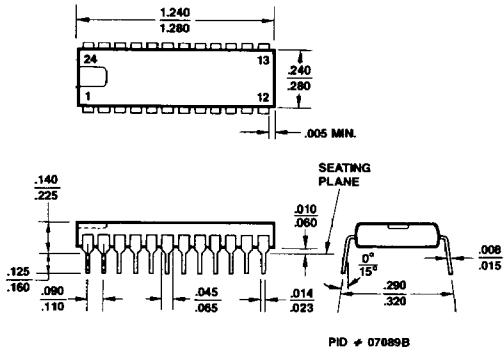
CD3024



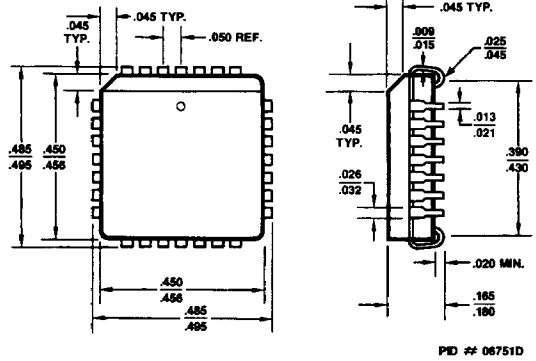
CL 028



PD3024



PL 028



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