AKM6208H Series

65536-Word × 4-Bit High Speed CMOS Static RAM

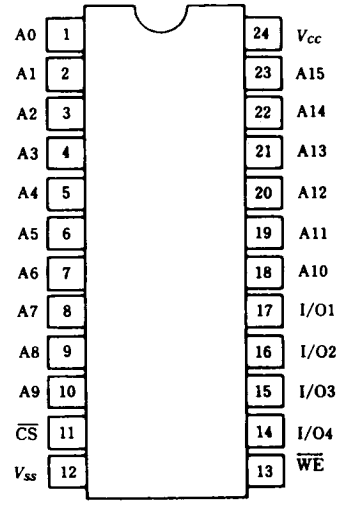
The AKM6208H is a high speed 256k static RAM organized as 64-kword x 4-bit. It realizes high speed access time (25/35 ns) and low power consumption, employing CMOS process technology and high speed circuit designing technology. It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU.

The AKM6208H, packaged in a 300-mil 24-pin plastic SOJ and DIP are available for high density mounting. Low power version retains the data with battery back up.

Features

- Single 5 V supply and high density 24-pin package
- High speed: Access time 25/35 ns (max)
- Low power
  - Operation: 300 mW (typ)
  - Standby: 100 μW (typ)
    30 μW (typ) (L-version)
- Completely static memory required
  - No clock or timing strobe required
- Equal access and cycle time
- Directly TTL compatible: All inputs and outputs
- Capability of battery back up operation (L-version)

PIN CONFIGURATION



(Top View)

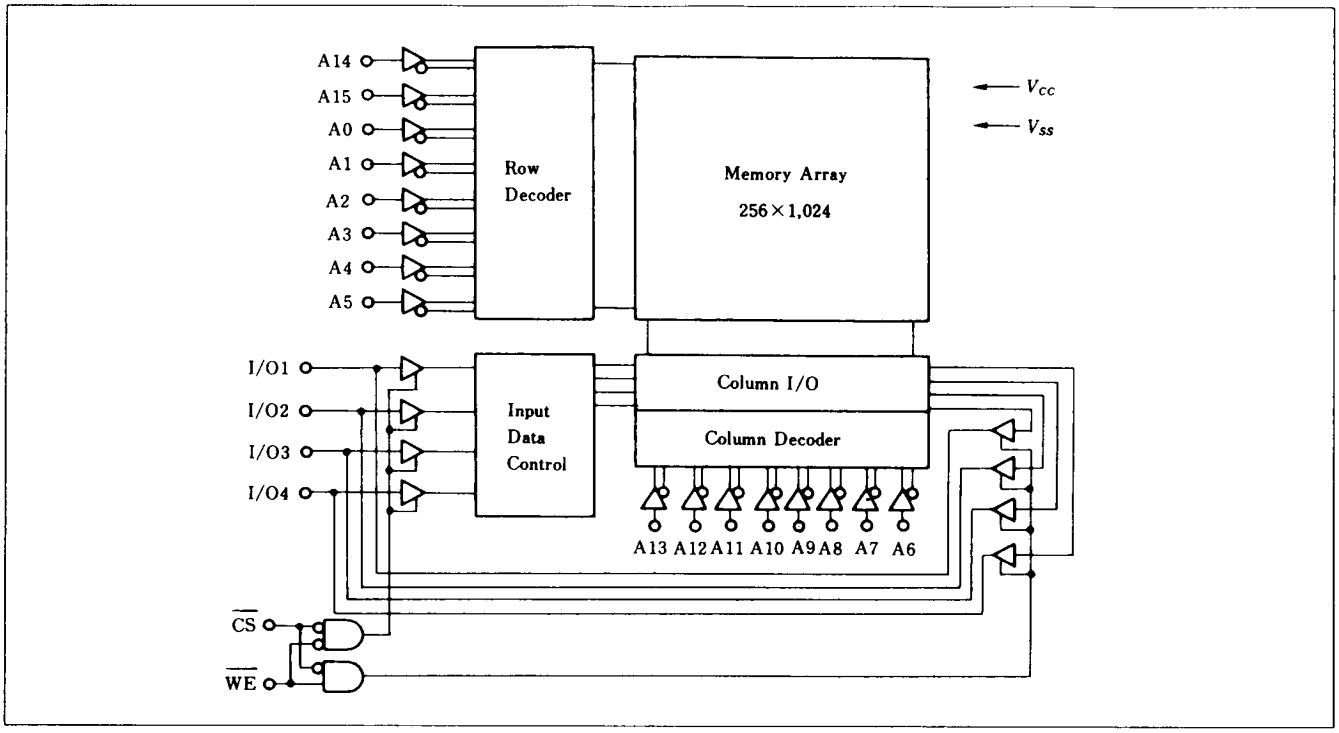
Ordering Information

Type No.	Access Time	Package
AKM6208HP-25	25 ns	300-mil 24-pin plastic DIP (DP-24NC)
AKM6208HP-35	35 ns	
AKM6208HLP-25	25 ns	
AKM6208HLP-35	35 ns	
AKM6208HJP-25	25 ns	300-mil 24-pin plastic SOJ (CP-24D)
AKM6208HJP-35	35 ns	
AKM6208HLJP-25	25 ns	
AKM6208HLJP-35	35 ns	

Pin Description

Pin Name	Function
A0 – A15	Address
I/O1 – I/O4	Input/Output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
Vcc	Power supply
Vss	Ground

Block Diagram



Function Table

$\overline{CS}$	$\overline{WE}$	Mode	Vcc Current	I/O Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High-Z	—
L	H	Read	Icc	Dout	Read cycle
L	L	Write	Icc	Din	Write cycle

Note: × means don't care.

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to Vss	Vin	−0.5*1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	−55 to +125	°C
Storage temperature range under bias	Tbias	−10 to +85	°C

Note: *1. Vin min = −2.5 V for pulse width ≤ 10 ns.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	–0.5*1	—	0.8	V

Note: *1. V_{IL} min = –2.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Item	Symbol	Min	Typ*1	Max	Unit	Test Conditions	Note
Input leakage current	I_{LI}	—	—	2.0	µA	V_{CC} = Max Vin = Vss to Vcc	
Output leakage current	I_{LO}	—	—	10.0	µA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = Vss to Vcc	
Operating power supply current	I_{CC}	—	60	120	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA, Min cycle, duty = 100%	
Standby power supply current	I_{SB}	—	20	40	mA	$\overline{CS}$ = V_{IH}, Min cycle	
Standby power supply current (1)	I_{SB1}	—	0.02	2.0	mA	$\overline{CS}$ ≥ Vcc – 0.2 V 0 V ≤ Vin ≤ 0.2 V or Vin ≥ Vcc – 0.2V	
		—	0.006	0.1			L-version
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA	
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –4.0 mA	

Note: *1. Typical limits are at V_{CC} = 5.0 V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1MHz)*1

Item	Symbol	Min	Max	Unit	Test Conditions
Input capacitance	Cin	—	6	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	11	pF	$V_{I/O}$ = 0 V

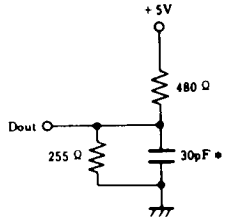
Note: *1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

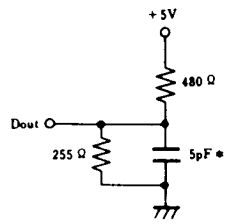
Test Conditions

- Input pulse levels: Vss to 3.0 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels : 1.5 V
- Output load: See Figures

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



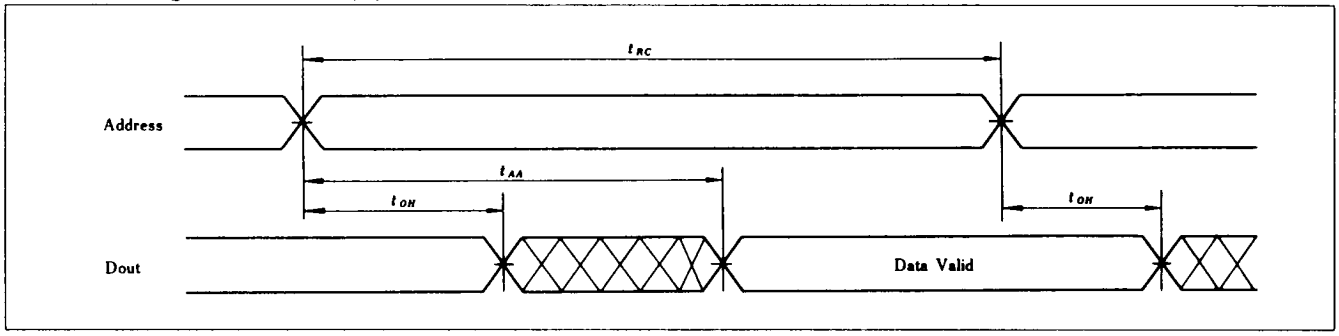
Note: * Including scope & jig.

Read cycle

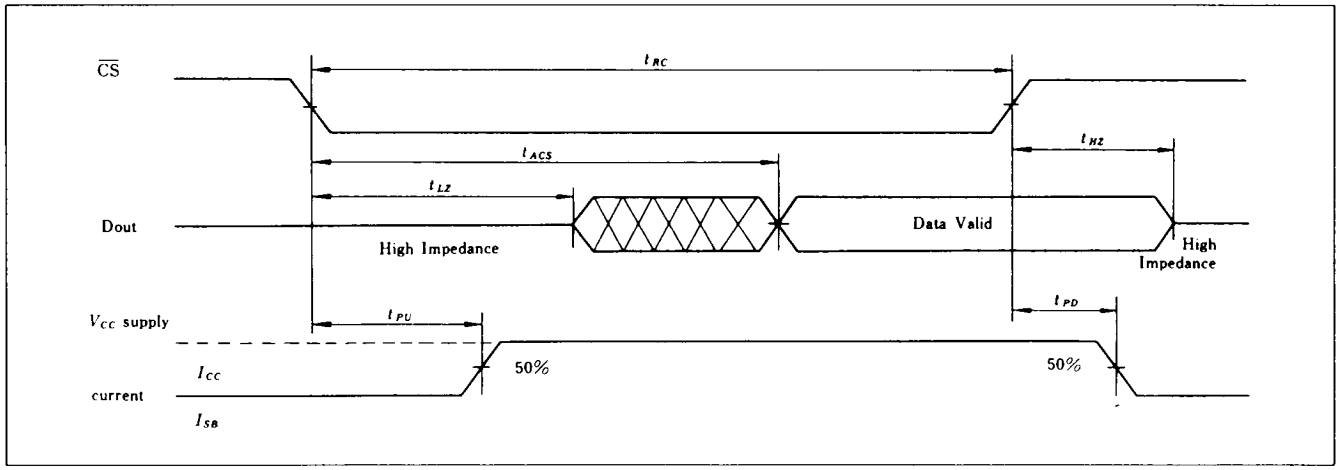
Item	Symbol	AKM6208H-25		AKM6208H-35		Unit
		Min	Max	Min	Max	
Read cycle time	t_{RC}	25	—	35	—	ns
Address access time	t_{AA}	—	25	—	35	ns
Chip select access time	t_{ACS}	—	25	—	35	ns
Output hold from address change	t_{OH}	5	—	5	—	ns
Chip selection to output in low-Z	t_{LZ}*1	5	—	5	—	ns
Chip deselection to output in high-Z	t_{HZ}*1	0	15	0	20	ns
Chip selection to power up time	t_{PU}	0	—	0	—	ns
Chip deselection to power down time	t_{PD}	—	15	—	25	ns

Note: *1 Transition is measured ±200 mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

Read Timing Waveform (1) *1, *2



Read Timing Waveform (2) *1, *3



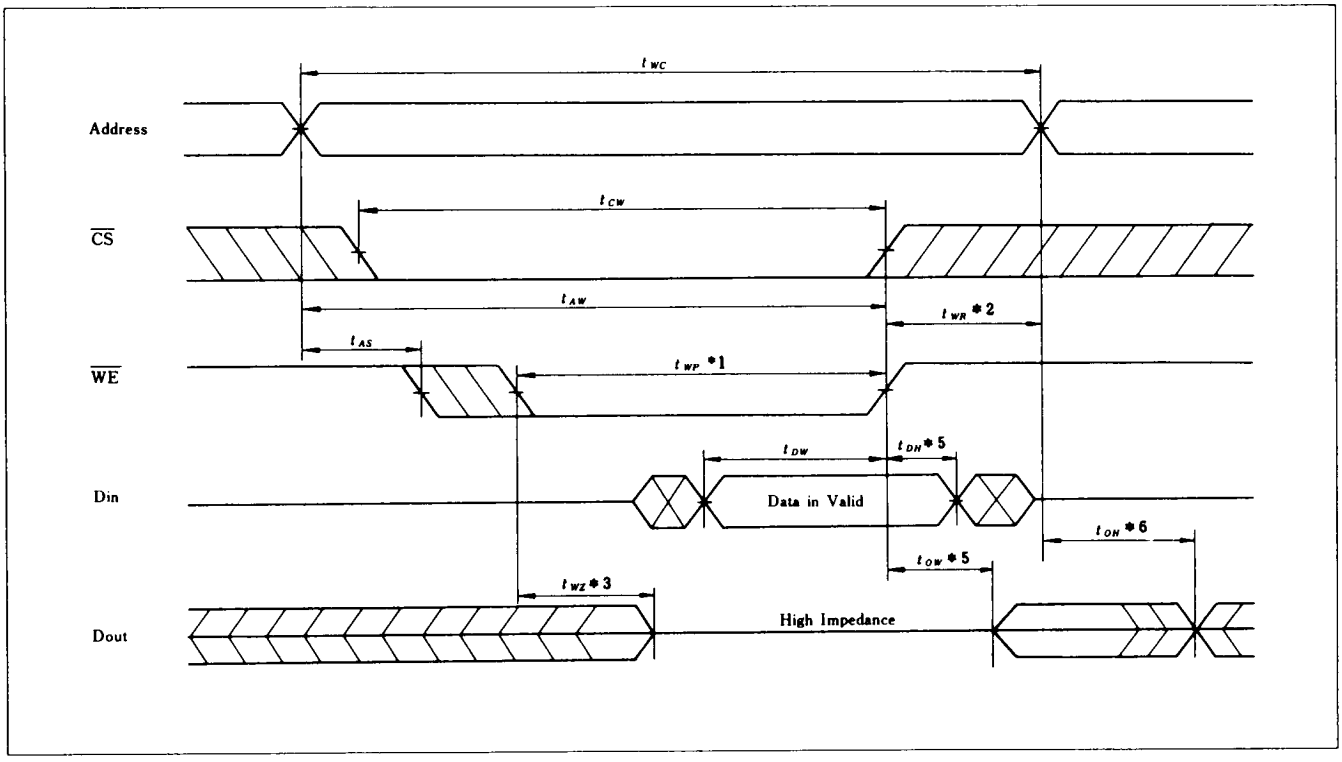
Notes: *1. $\overline{WE}$ is high for read cycle.
*2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
*3. Address valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle

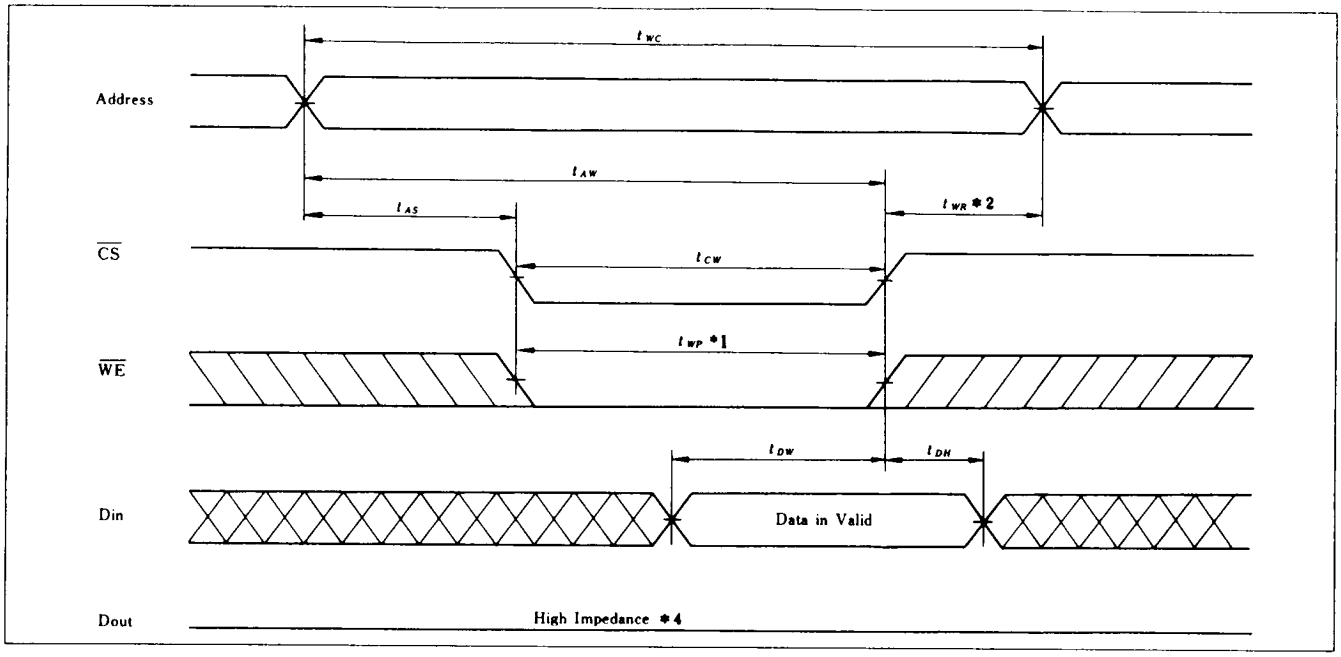
Item	Symbol	AKM6208H-25		AKM6208H-35		Unit
		Min	Max	Min	Max	
Write cycle time	twc	25	—	35	—	ns
Chip selection to end of write	tcw	20	—	30	—	ns
Address valid to end of write	taw	20	—	30	—	ns
Address setup time	tas	0	—	0	—	ns
Write pulse width	twp	20	—	25	—	ns
Write recovery time	twr	3	—	3	—	ns
Data valid to end of write	tdw	15	—	20	—	ns
Data hold time	tdh	0	—	0	—	ns
Write enabled to output in high-Z	twz*1	0	8	0	10	ns
Output active from end of write	tow*1	0	—	0	—	ns

Note: *1 Transition is measured ±200 mV from high impedance voltage with Load (B). This parameter is sampled and not 100% tested.

Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Write Timing Waveform (2) ($\overline{CS}$ Controlled)



Notes: *1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP})
*2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
*3. During this period, I/O pins are in the output state. The input signals of the opposite phase to the outputs must not be applied.
*4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
*5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. The data input signals of opposite phase to the outputs must not be applied to them.
*6. Dout is the same phase of write data of this write cycle.

Low Vcc Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L-version.

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Vcc for data retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq Vcc - 0.2$ V, Vin ≥ Vcc – 0.2 V or 0 V ≤ Vin ≤ 0.2 V
Data retention current	I_{CCDR}	—	1	50*1	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	
Operation recovery time	t_R	5	—	—	ms	

Notes: *1. Vcc = 3.0 V.

Low Vcc Data Retention Timing Waveform