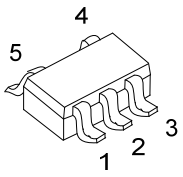
# MONOLITHIC IC 82XX SERIES




SOT-25

## ■ DESCRIPTION

The normal operation of the UTC **82XX** is that while the power is turned on or interrupted, detect power supply voltage and then reset the system accurately.

The internal circuits of the UTC **82XX** include a built-in fixed delay time generating circuit. With a counter timer using an analog/digital hybrid circuit, the UTC **82XX** as new low reset type system reset ICs expands the delay time series.

These ICs can be used in a variety of CPU systems and other logic systems.

## ■ FEATURES

* Internal Fixed Delay Time Setting by Counter Timer
* Grate Delay Time Temperature Characteristics:±800ppm/°C
* Operating Limit Voltage as 0.65V(Typ.)
* Hysteresis Voltage Provided: 50mV(Typ.)
* Circuit Current While On $I_{CCL}$=300μA(Typ.)
* Circuit Current While Off $I_{CCH}$=200μA(Typ.)
* Halogen Free

## ■ ORDERING INFORMATION

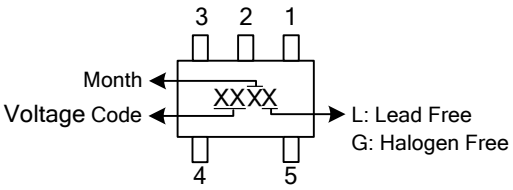
| Ordering Number | Package | Packing |
|---|---|---|
| 82XXG-x-AF5-R | SOT-25 | Tape Reel |

Notes: xx: Output Voltage, refer to Marking Information.
x : Delay Time, refer to Electrical Characteristics of "H" Transport Delay Time

82XX G-x-AF5-R
(1) Packing Type
(2) Package Type
(3) Delay Time
(4) Halogen Free
(5) Output Voltage Code

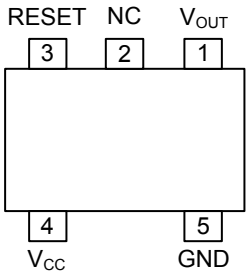
(1) R: Tape Reel
(2) AF5: SOT-25
(3) x: Refer to Electrical Charactreistics of "H" Transport Delay Time
(4) G: Halogen Free
(5) xx: Refer to Marking Information

## ■ MARKING INFORMATION

| PACKAGE | VOLTAGE CODE | MARKING |
|---|---|---|
| SOT-25 | 25:2.5V<br>27:2.7V<br>2K:2.93V |  |



## ■ PIN CONFIGURATION

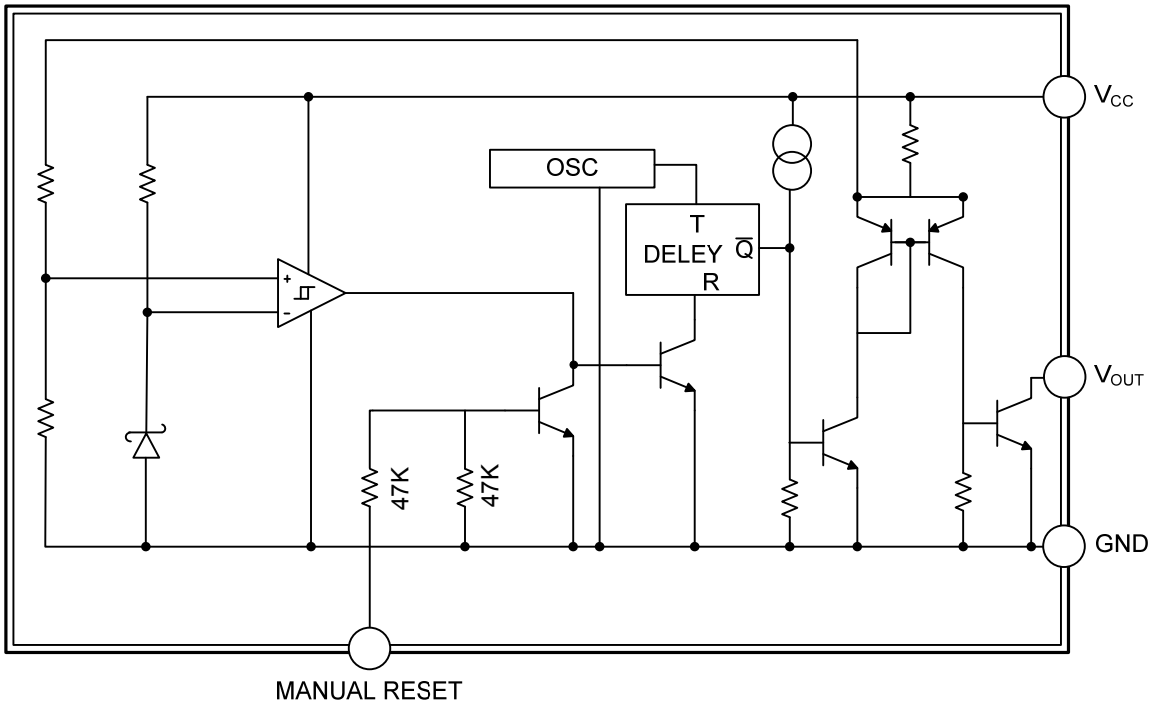




## ■ PIN DESCRIPTION

| PIN NO. | PIN NAME | DESCRIPTION |
|---|---|---|
| 1 | $V_{OUT}$ | Output pin |
| 2 | NC | Connected nothing |
| 3 | RESET | Reset control pin |
| 4 | $V_{CC}$ | Supply voltage |
| 5 | GND | Ground |

■ BLOCK DIAGRAM



## ■ ABSOLUTE MAXIMUM RATING (Ta=25°C)

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | -0.3~+10 | V |
| Manual Reset Input Voltage | $V_{RESET}$ | -0.3~+10 | V |
| Power Dissipation | $P_D$ | 400 | mW |
| Operating Temperature | $T_{OPR}$ | -20~+75 | °C |
| Storage Temperature | $T_{STG}$ | -40~+125 | °C |

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

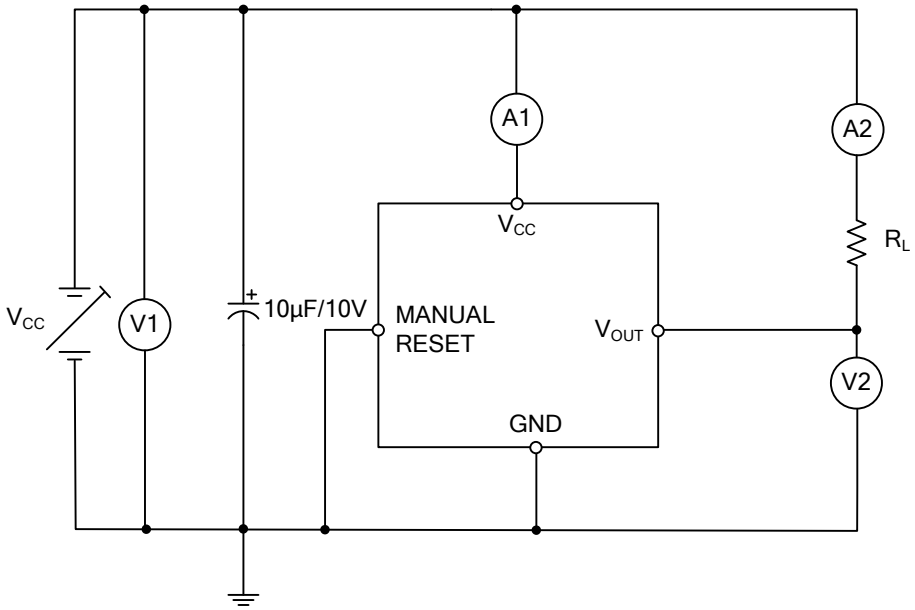
## ■ ELECTRICAL CHARACTERISTICS (Ta=25°C, Unless otherwise specified)

**$V_S$=2.5V~2.93V**

| PARAMETER | | SYMBOL | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| Detection Voltage | | $V_S$ | $V_{OL}$≤0.4V, $V_{CC}$=H→L, $R_L$=470Ω (See Test Circuit 1) | | $V_S$ -0.15V | $V_S$ | $V_S$ +0.15V | V |
| Low-Level Output Voltage | | $V_{OL}$ | $V_{CC}$=$V_{S(min)}$-0.05V, $R_L$=470Ω (See Test Circuit 1) | | | 0.1 | 0.4 | V |
| Operating Power Supply Voltage | | $V_{OPL}$ | $R_L$=4.7kΩ, $V_{OL}$≤0.4V | | | 0.65 | 0.85 | V |
| Hysteresis Voltage | | $\Delta V_S$ | $V_{CC}$=L→H→L , $R_L$=470Ω (See Test Circuit 1) | | 30 | 50 | 100 | mV |
| Detection Voltage Temperature Coefficient | | $\frac{V_S}{\Delta T}$ | $R_L$=470Ω, Ta=-20°C~+75°C (See Test Circuit 1) | | | ±0.01 | | %/°C |
| Output Leakage Current | | $I_{OH}$ | $V_{CC}$=10V (See Test Circuit 1) | | | | ±0.1 | μA |
| Circuit Current | On | $I_{CCL}$ | $V_{CC}$= $V_{S(min)}$-0.05V, $R_L$=∞ (See Test Circuit 1) | | | 300 | 600 | μA |
| | Off | $I_{CCH}$ | $V_{CC}$=$V_{S(Typ)}$/0.85V, $R_L$=∞ (See Test Circuit 1) | | | 200 | 350 | μA |
| "H" Transport Delay Time | | $t_{PLH}$ | $R_L$=4.7KΩ, $C_L$=100PF (Note 1) (See Test Circuit 2) | P | 30 | 50 | 75 | mS |
| | | | | Q | 60 | 100 | 150 | mS |
| | | | | R | 120 | 200 | 300 | mS |
| | | | | S | 240 | 400 | 600 | mS |
| | | | | T | 480 | 800 | 1200 | mS |
| "L" Transport Delay Time | | $t_{PHL}$ | $R_L$=4.7kΩ, $C_L$=100PF (Note 1) (See Test Circuit 2) | | | 10 | | μS |
| Output Current While on 1 | | $I_{OL1}$ | $V_{CC}$=VS min.-0.05V, $R_L$=0Ω (See Test Circuit 1) | | 8 | | | mA |
| Output Current While on 2 | | $I_{OL2}$ | Ta=-20°C ~+75°C, $R_L$=0Ω(Note 2) (See Test Circuit 1) | | 6 | | | mA |
| Manual Reset Pin | Input High Voltage | $V_{RESH}$ | | | 2.0 | | | V |
| | Input High Current | $I_{RESH}$ | $V_{RESET}$=2V | | | | 80 | μA |
| | Input Low Voltage | $V_{RESL}$ | | | | | 0.8 | V |

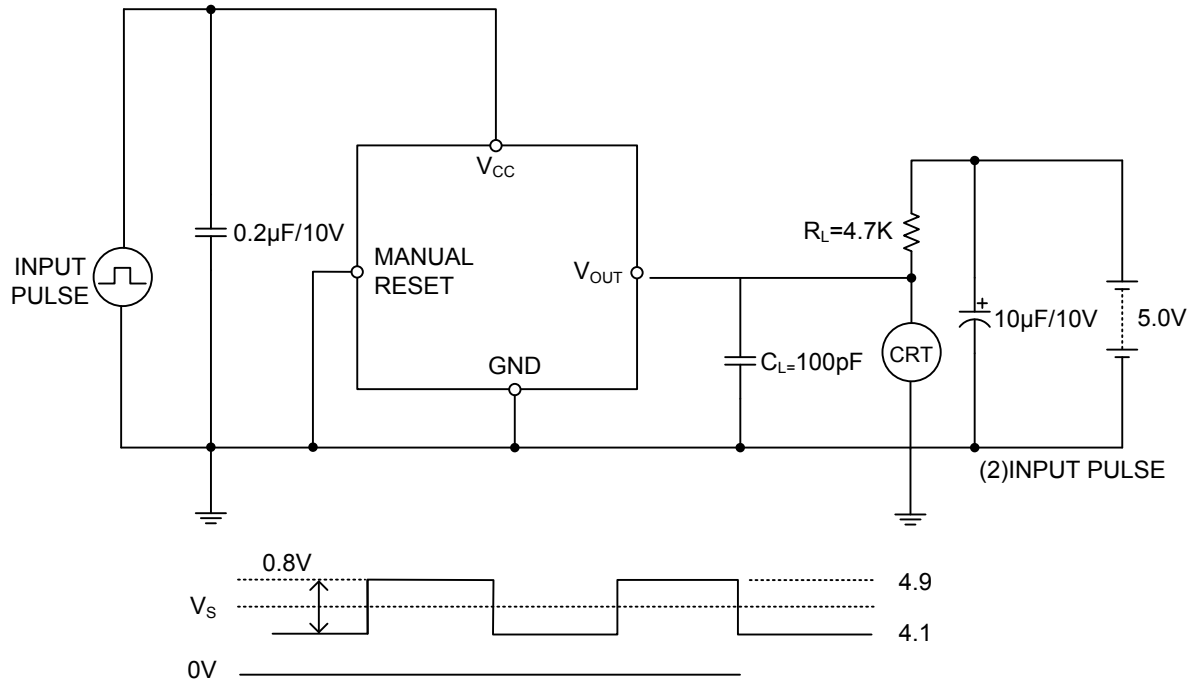
Notes: 1. $t_{PLH}$: $V_{CC}$= ($V_{S(TYP)}$-0.4V)→($V_{S(TYP)}$+0.4V)
$t_{PHL}$: $V_{CC}$= ($V_{S(TYP)}$+0.4V)→($V_{S(TYP)}$-0.4V)
2. $V_{CC}$=$V_{S(MIN)}$-0.15V
3. $V_{OUT}$ pin is low when manual reset pin is high.
$V_{OUT}$ pin is high when manual reset pin is low.

## ■ TEST CIRCUITS




**Test Circuit 1**

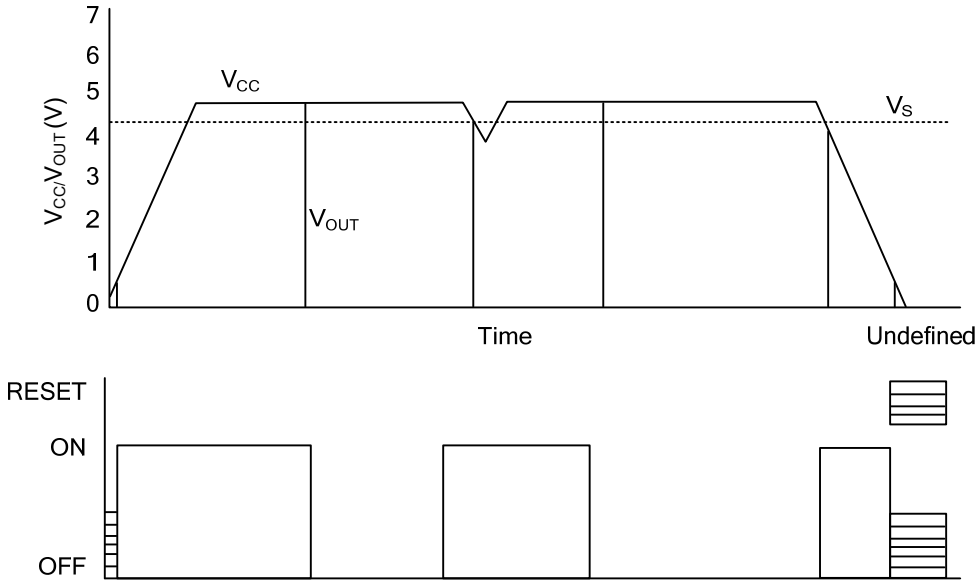
A: DC ammeter
V: DC voltmeter
CRT: Oscilloscope




Note Input model is an example for 82XX

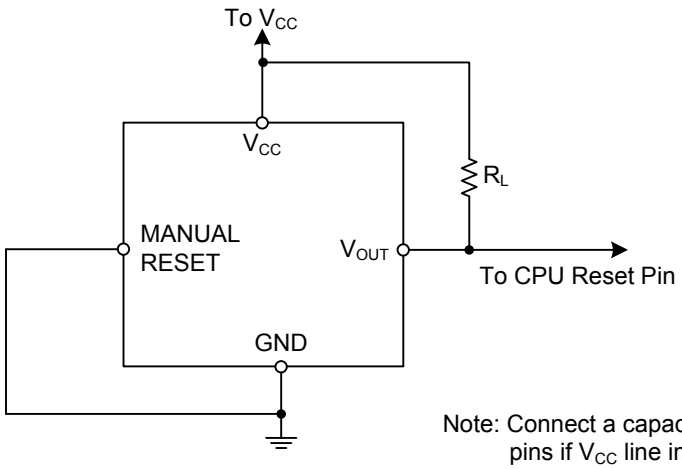
**Test Circuit 2**

■ TIMING CHART



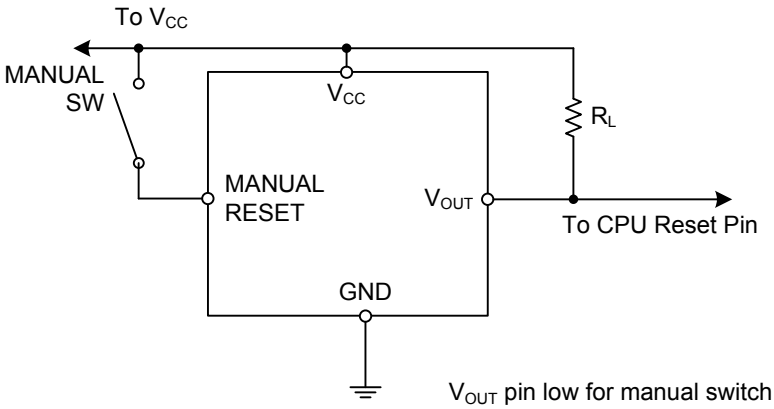
## ■ TYPICAL APPLICATION CIRCUITS

1. Normal hard reset




Note: Connect a capacitor between IC $V_{CC}$ and GND pins if $V_{CC}$ line impedance is high.

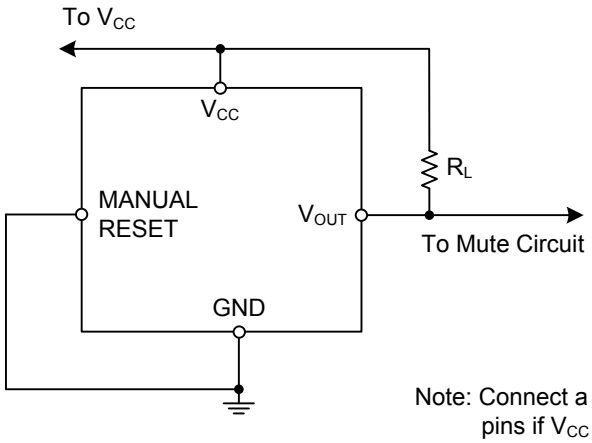
2. Manual reset




$V_{OUT}$ pin low for manual switch ON.
$V_{OUT}$ pin high for manual switch OFF.

Note: Connect a capacitor between IC $V_{CC}$ and GND pins if $V_{CC}$ line impedance is high.

3. Mute circuit




Note: Connect a capacitor between IC $V_{CC}$ and GND pins if $V_{CC}$ line impedance is high.