NEC

MOS FIELD EFFECT TRANSISTOR
2SK3109

SWITCHING
N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK3109 is N-channel MOS FET device that features a low on-state resistance and excellent switching characteristics, and designed for high voltage applications such as DC/DC converter.

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3109	TO-220AB (MP-25)
2SK3109-S	TO-262 (MP-25 Fin Cut)
2SK3109-ZJ	TO-263 (MP-25ZJ)

FEATURES

- Gate voltage rating ±30 V
- Low on-state resistance
  $R_{DS(on)}$ = 0.4 Ω MAX. (V_{GS} = 10 V, I_D = 5.0 A)
- Low input capacitance
  C_{iss} = 400 pF TYP. (V_{DS} = 10 V, V_{GS} = 0 V)
- Avalanche capability rated
- Built-in gate protection diode
- Surface mount device available

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	200	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±30	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±10	A
Drain Current (pulse) **Note1**	$I_{D(pulse)}$	±30	A
Total Power Dissipation (T_A = 25°C)	P_{T1}	1.5	W
Total Power Dissipation (T_C = 25°C)	P_{T2}	50	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current **Note2**	I_{AS}	10	A
Single Avalanche Energy **Note2**	E_{AS}	35	mJ

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Starting T_{ch} = 25°C, V_{DD} = 100 V, R_G = 25 Ω, V_{GS} = 20 → 0 V

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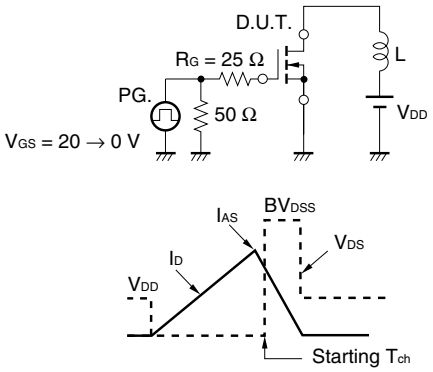
The mark ★ shows major revised points.

★ ELECTRICAL CHARACTERISTICS (T_A = 25°C)

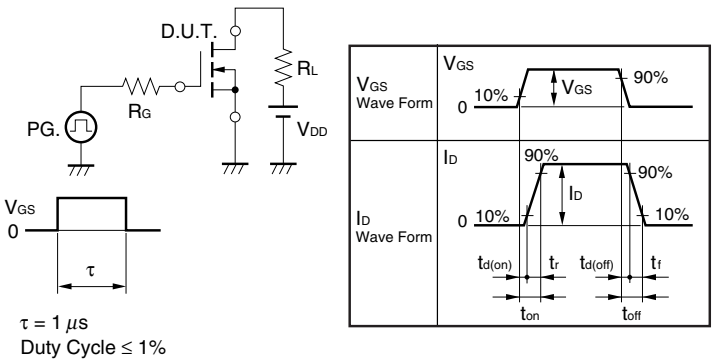
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 200 V, V_{GS} = 0 V			100	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0 V			±10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	2.5		4.5	V
Forward Transfer Admittance **Note**	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 5.0 A	1.5			S
Drain to Source On-state Resistance **Note**	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 5.0 A		0.32	0.4	Ω
Input Capacitance	C_{iss}	V_{DS} = 10 V,		400		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V,		110		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		55		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 100 V, I_D = 5.0 A,		12		ns
Rise Time	t_r	V_{GS} = 10 V,		34		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 10 Ω		40		ns
Fall Time	t_f			20		ns
Total Gate Charge	Q_G	V_{DD} = 160 V,		18		nC
Gate to Source Charge	Q_{GS}	V_{GS} = 10 V,		3.5		nC
Gate to Drain Charge	Q_{GD}	I_D = 10 A		10		nC
Body Diode Forward Voltage **Note**	$V_{F(S-D)}$	I_F = 10 A, V_{GS} = 0 V		1.0		V
Reverse Recovery Time	t_{rr}	I_F = 10 A, V_{GS} = 0 V,		250		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 50 A/μs		1.0		μC

Note Pulsed

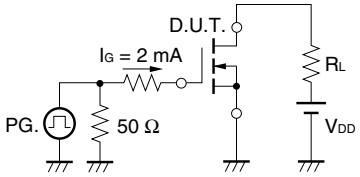
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

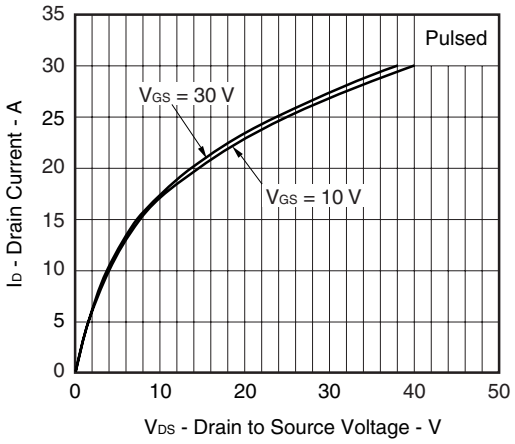


TEST CIRCUIT 3 GATE CHARGE

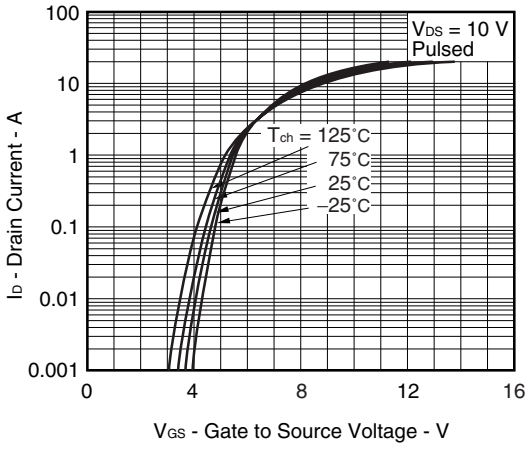


TYPICAL CHARACTERISTICS (T_A = 25°C)

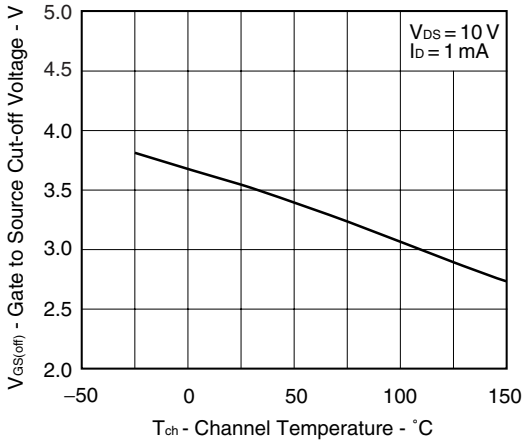
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



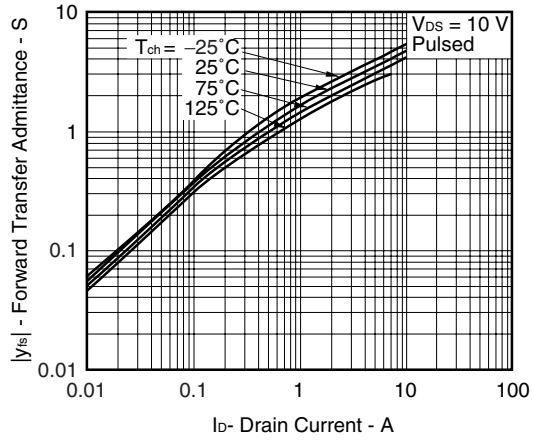
FORWARD TRANSFER CHARACTERISTICS



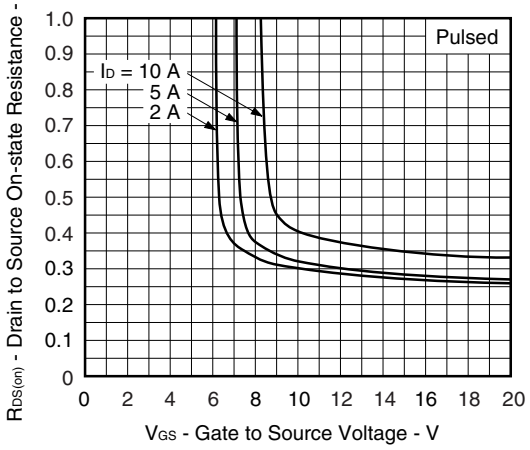
GATE TO SOURCE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



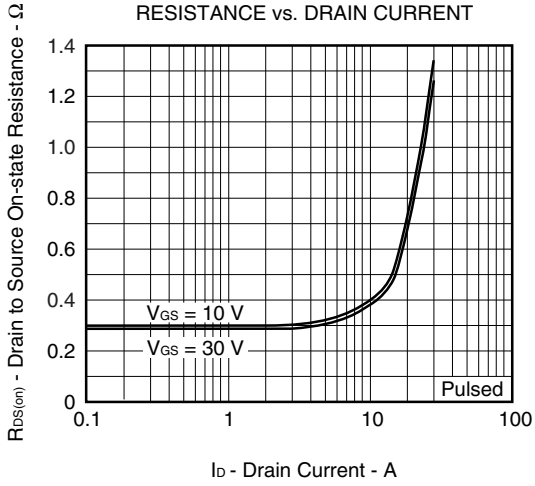
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



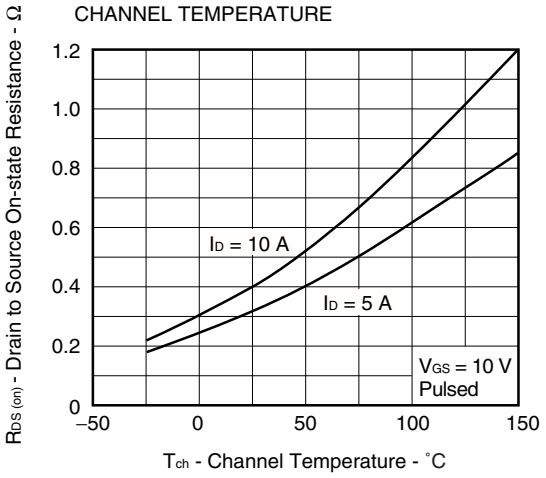
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



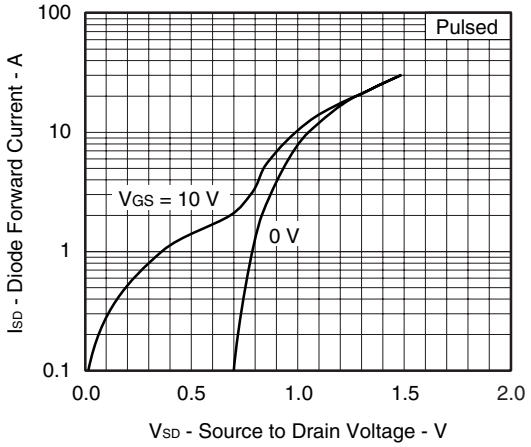
DRAIN TO SOURCE ON-STATE
RESISTANCE vs. DRAIN CURRENT



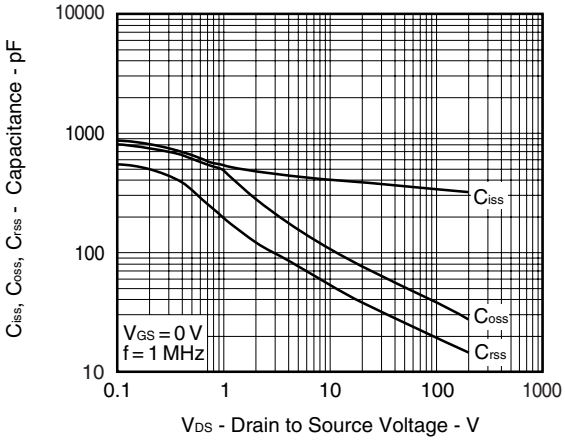
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



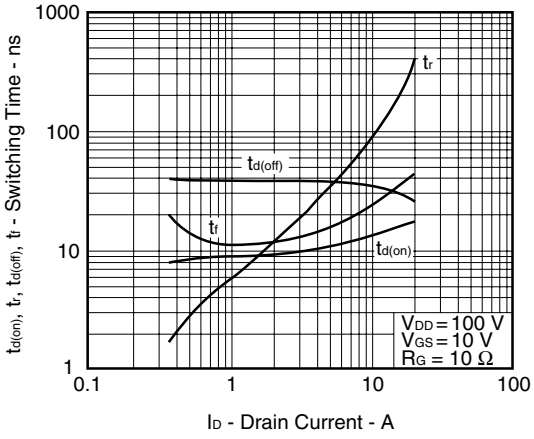
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



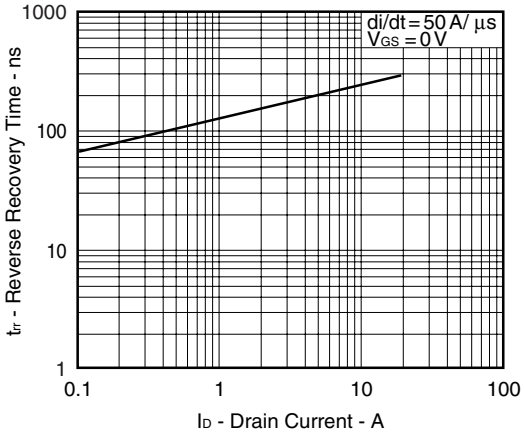
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



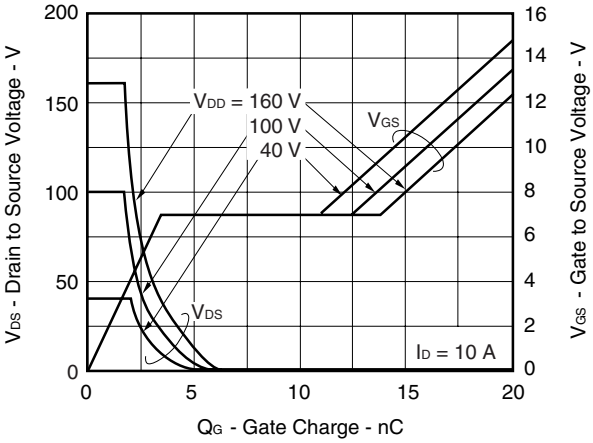
SWITCHING CHARACTERISTICS



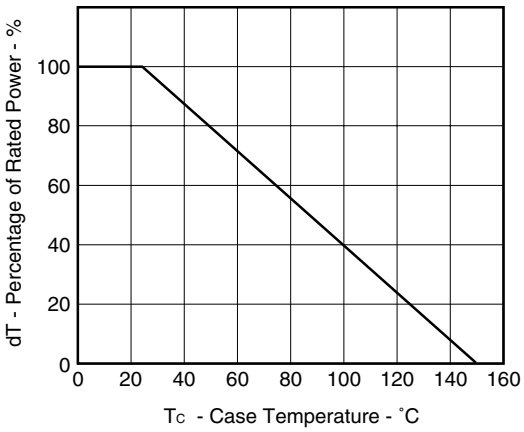
REVERSE RECOVERY TIME vs. DRAIN CURRENT



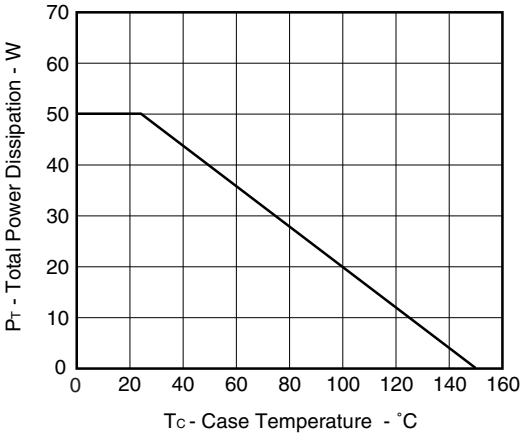
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



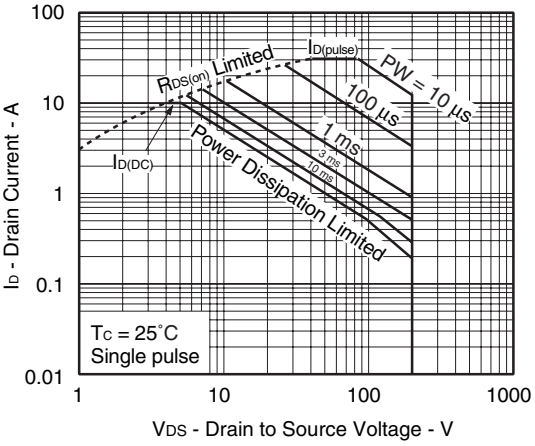
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



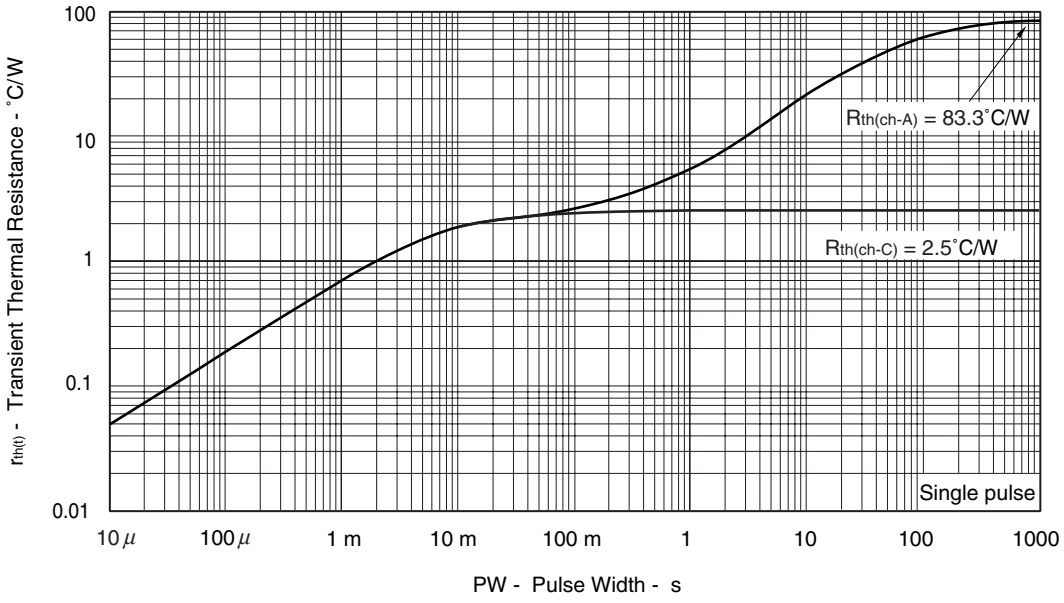
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



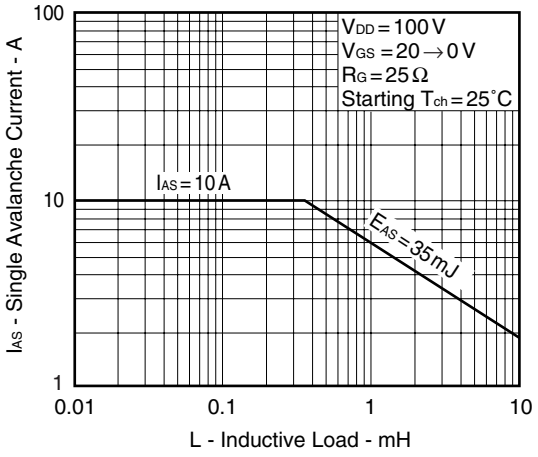
FORWARD BIAS SAFE OPERATING AREA



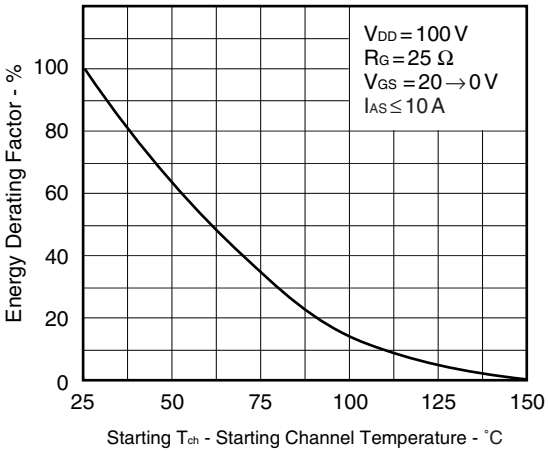
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD

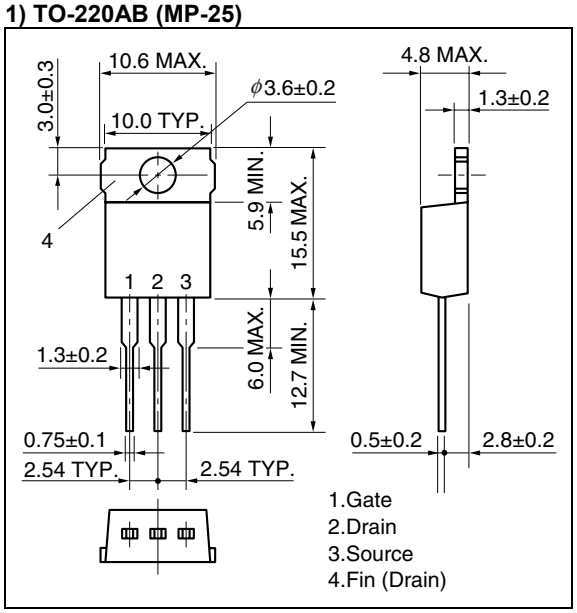


SINGLE AVALANCHE ENERGY
DERATING FACTOR

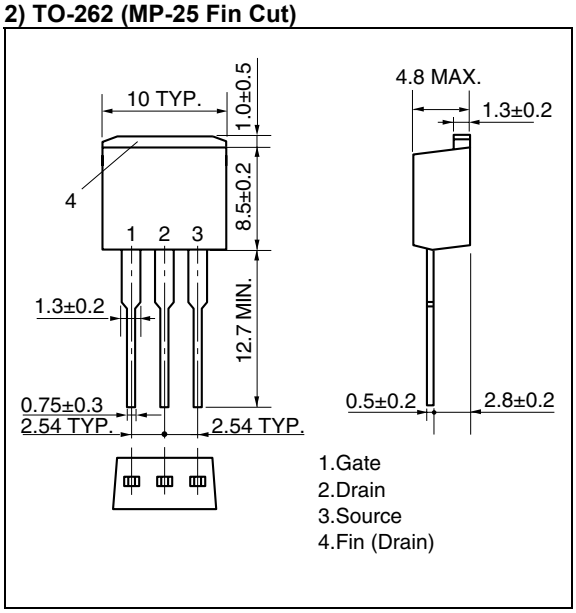


★ PACKAGE DRAWINGS (Unit: mm)

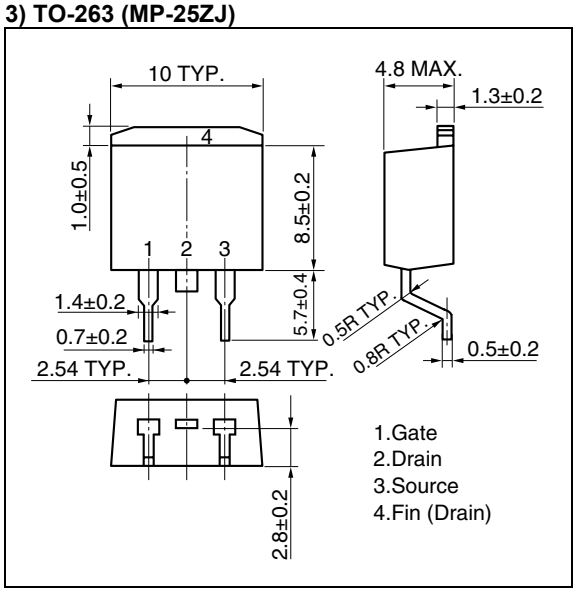
1) TO-220AB (MP-25)



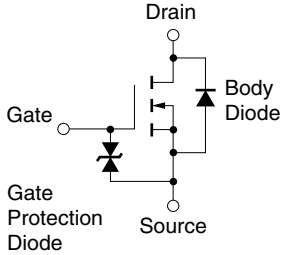
2) TO-262 (MP-25 Fin Cut)



3) TO-263 (MP-25ZJ)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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