16-BIT DIGITAL-TO-RESOLVER CONVERTER

DESCRIPTION

The DR-11800 is a small size, high accuracy, 16-bit digital-to-sine/cosine converter. Available in accuracies up to 1 arc minute, the DR-11800 is contained in a 28-pin, one-square-inch hermetically sealed package and requires +15 Vdc and -15 Vdc power supplies. The reference conditioner allows for either 115 Vrms or 26 Vrms reference input for a 6.8 Vrms sin/cos output. Two registers for the input of the 16-bit (CMOS/TTL) natural binary angle data allow for compatibility with an 8-bit or 16-bit data bus.

Internally, the DR-11800 has a multiplying digital-to-sin/cos converter made of two function generators and a quadrant select network. Quadrant information is available from the two most significant bits. The two function generators use the remaining angular data along with the buffered reference voltage. Similar to a multiplying DAC (digital-to-analog converter), the DR-11800 uses high accuracy resistive ladder networks and solid state switching to control the attenuation of the reference voltage. The output buffer amplifiers allow for up to 2 mA output drive.

APPLICATIONS

High accuracy, high reliability, small size, low power consumption and MIL-PRF-38534 processing availability, make the DR-11800 suitable for industrial and military ground or avionics applications. Possible applications include digital remote positioning, resolver angle simulators, flight trainer, flight instrumentation, radar and navigational systems, and PPI displays including moving target indicators. Other applications are synchro/resolver system development and test, and wraparound test of synchro/resolver-to-digital converters.

FEATURES

- ***28-Pin Square Package***
- ***1 Arc Minute Accuracy***
- ***0.03% Radius Accuracy***
- ***Microprocessor Compatible - 8- and 16-Bit***
- ***Double-Buffered Inputs***
- ***Pin-Programmable Reference Input (for 26 and 115 Vrms)***
- ***DC-Coupled Reference and Outputs***
- ***Requires Only ±15 V Power Supplies***
- ***TTL and CMOS Compatible***
- ***Pin-for-Pin Replacement for Natel's HDR2406***

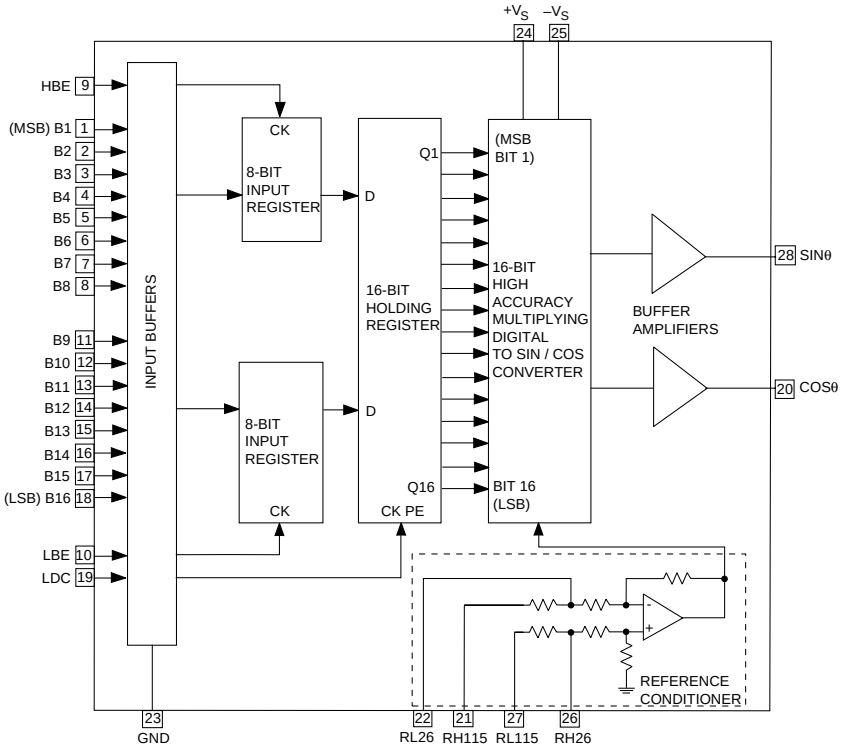


FIGURE 1. DR-11800 BLOCK DIAGRAM

TABLE 1. DR-11800 SPECIFICATIONS		
PARAMETER	**VALUE**	**REMARKS**
DIGITAL ANGULAR		
Resolution	16 Bits	Bit 1 = MSB, Bit 16 = LSB
Accuracy	±4 arc-minutes ±2 arc-minutes ±1 arc-minutes	Accuracy applies over operating temperature range.
SCALE FACTOR VARIATION		
Scale Factor Variation	±0.1% max	Simultaneous amplitude variation in both outputs as a function of digital angle.
REFERENCE INPUT (RH-RL)		
Voltage	115 V rms or 26 V rms	Differential solid-state input.
Frequency Range	dc to 1000 Hz	
Input Resistance	Differential 230 kΩ Differential 52 kΩ	115 V rms reference 26 V rms reference
ANALOG OUTPUTS		
Max SIN θ, COS θ	6.8 V rms, ±1.5 %	Output voltage varies in direct proportion to reference voltage.
Output Current	2 mA rms	
Output Impedance	< 1 ohm	Op amp output.
Zero Offset (dc)	±10 mV typical ±25 mV max	
Offset Drift	25 µV/°C typical, 50 µV/°C max	
Output Settling Time	50 µsec max to accuracy of converter.	For any digital step change.
DIGITAL INPUTS		
Logic Levels		No external logic voltages required.
Logic 0	-0.3 Vdc to 0.8 V dc	
Logic 1	2.4 Vdc to 5.5 V dc	
Loading	0.1 TTL load	CMOS transient protected.
Input Current		
Data Bits (B1-B16)	15 µA typ, “active” pull-down to gnd	For less than 16 bits, unused pins can float.
HBE, LBE, LDC	-15 µA typ, “active” pull-up to internal logic supply	Unused pins can float.
REGISTER CONTROLS		
HBE	Logic 1 Logic 0	8 MSBs enter high byte input register. High byte register remains unaffected.
LBE	Logic 1 Logic 0	8 LSBs enter low byte input register. Low byte register remains unaffected
LDC	Logic 1 Logic 0	Data from input registers transferred to holding register. Data in holding register remains unaffected
Pulse Width	600 ηsec min	For guaranteed data transfer.

TABLE 1. DR-11800 SPECIFICATIONS (CONTINUED)		
PARAMETER	**VALUE**	**REMARKS**
REGISTER CONTROLS (Continued)		
Data Set-up Time	200 ηsec min	Before data transfer.
Data Hold Time	200 ηsec min	Before input data changes.
POWER SUPPLIES		
Supply Voltages (±Vs)	±15 V dc ±10%	Without output clipping.
Supply Current	±35 mA max	
Supply Rejection	70 db	Typ.
TEMPEATURE RANGES		
Operating Case		
-3XXX and -8XXX	0°C to +70°C	
-1XXX and -4XXX	-55°C to +125°C	
Storage	-65°C to +135°C	
PHYSICAL CHARACTERISTICS		
Type	28 Pin Square	
Size	1.0 x 1.0 x 0.21 in. (25 x 25 x 5.3) mm	
Weight	0.6 oz (17 g) max	
ABSOLUTE MAXIMUM RATINGS		
Reference Input:	Twice Normal Voltage	
Power Supply Voltage (±Vs):	±18 V dc	
Digital Inputs:	-0.3 V dc to +6.5 V dc	

NOTE. Although digital inputs are CMOS protected, storage in conductive foam is recommended.

ANALOG OUTPUT PHASING

The DR-11800 provides an output of 6.8V sinθ and 6.8V cosθ for either a 26 Vrms reference (use pin 26; RH26, and pin 22; RL26) or 115 Vrms reference (use pin 21; RH115, and pin 27; RL115). FIGURE 2 illustrates the input connection for a 26V or 115V reference. FIGURE 3 illustrates the output phasing.

DIGITAL INTERFACE

The DR-11800 has double-buffered input registers which allow for easy implementation of an interface with 8-bit or 16-bit data buses. The DR-11800 can also be set up for asynchronous data inputs. If the LBE, HBE and LDC input pins are left open, the internal pull-up circuitry will set these pins to a high state and the information at the data inputs (B1-B16) will be continuously converted to sinθ and cosθ at the analog outputs. In applications requiring less than 16-bit resolution, the unused pins can be left open. The data bits (B1-B16) are internally pulled-down to apply a logic 0 to unconnected data inputs.

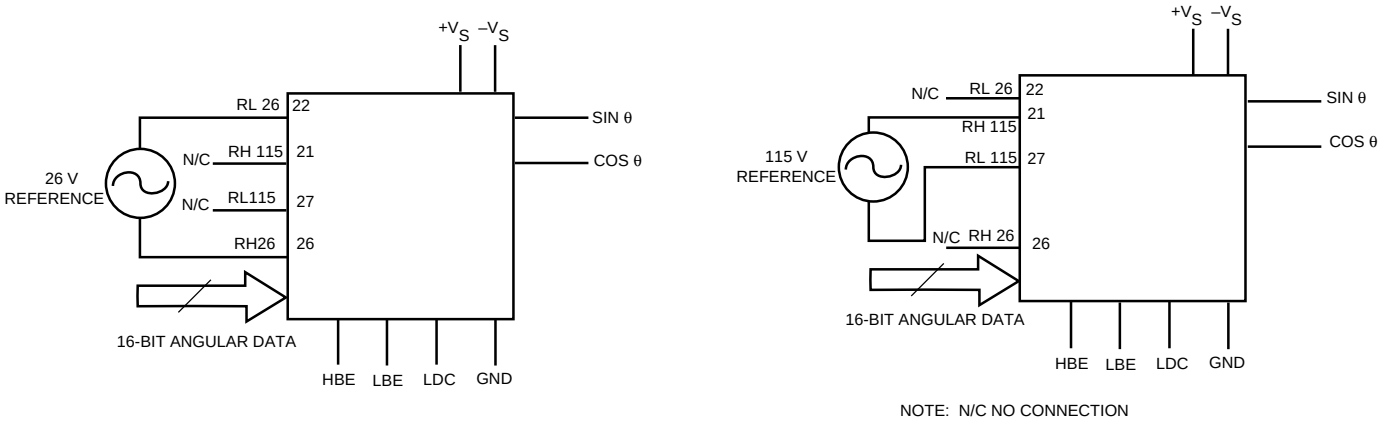
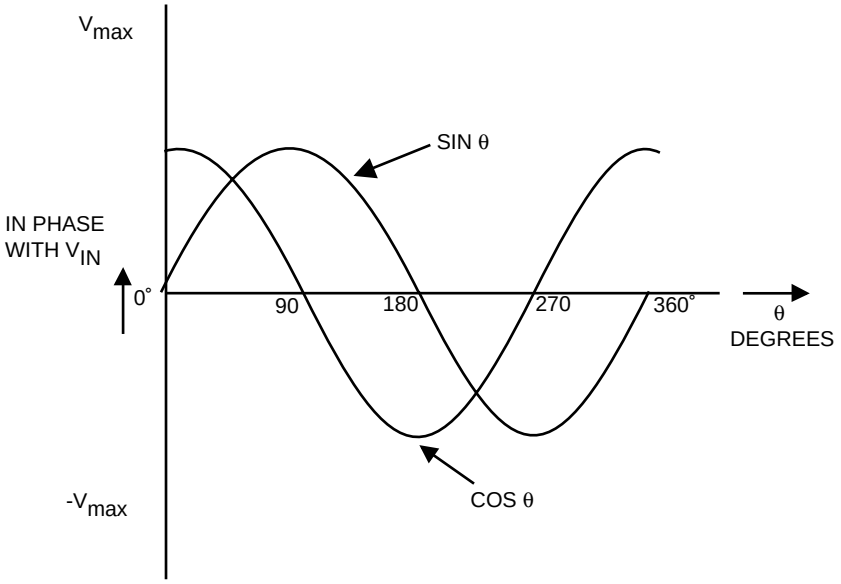


FIGURE 2. CONNECTIONS TO 26 V/115 V REFERENCE



SIN OUTPUT = 6.8V rms(1+n)SINθ

COS OUTPUT = 6.8V rms(1+n)COSθ

n IS THE SCALE FACTOR VARIATION AS A FUNCTION OF DIGITAL ANGLE(± 0.1%)

FIGURE 3. OUTPUT PHASING

DATA TRANSFER FROM AN 8-BIT DATA BUS

Applications with an 8-bit data bus require two-byte loading of the digital input (see FIGURE 4).

FIGURE 5 shows the timing for two-byte data transfers.

1. LDC is low (logic 0) so that the contents of the holding register are latched and will remain unaffected by the changes on the input registers.

2.When the LBE is set high (logic 1) the 8 LSBs (B9-B16) are transferred to the low byte. The LBE must remain high for a minimum of 800 nsec after the data is stable. The data should remain stable for 200 nsec after the LBE is set low (logic 0).

3.When the HBE is set high (logic 1) the 8 MSBs (B1-B8) are transferred to the low byte. The HBE must remain high for a minimum of 800 nsec after the data is stable. The data should remain stable for 200 nsec after the HBE is set low (logic 0).

4.When the LDC is set high (logic 1) the data is transferred from the two input registers to the holding register. The LDC should be held high for 600 nsec minimum. Once the LDC is set low, the cycle can begin again.

Note: LBE, HBE, and LDC are level-actuated functions.

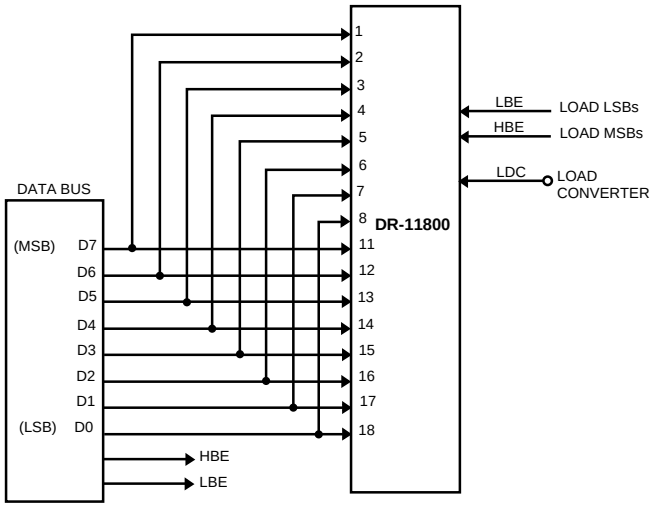


FIGURE 4. DATA TRANSFER FROM 8-BIT BUS

DATA TRANSFER FROM A 16-BIT DATA BUS

Applications interfacing with a 16-bit data bus require only single byte loading, as shown in FIGURE 6. LBE and HBE are either unconnected or tied together and pulsed high to load data.

As shown in the timing diagram (see FIGURE 7) 200 nsec after the data is stable the LDC is set high (logic 1) to transfer the data to the holding register. Since LDC is level actuated, it must remain high for the time specified (600 nsec) to transfer the data.

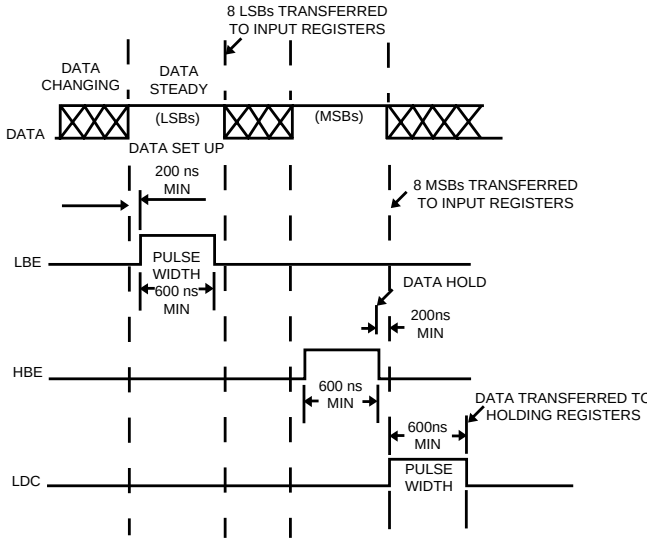


FIGURE 5. TIMING FOR 8-BIT BUS TRANSFER

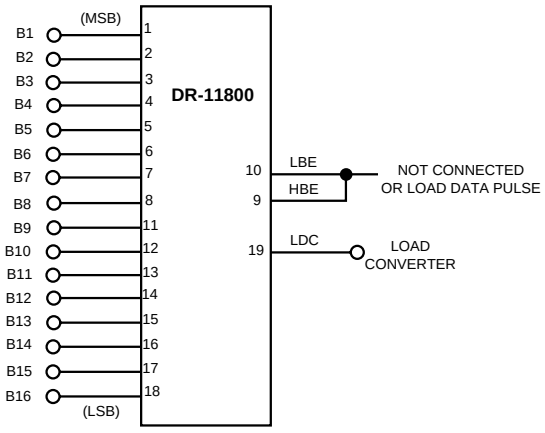


FIGURE 6. DATA TRANSFER FROM 16-BIT BUS

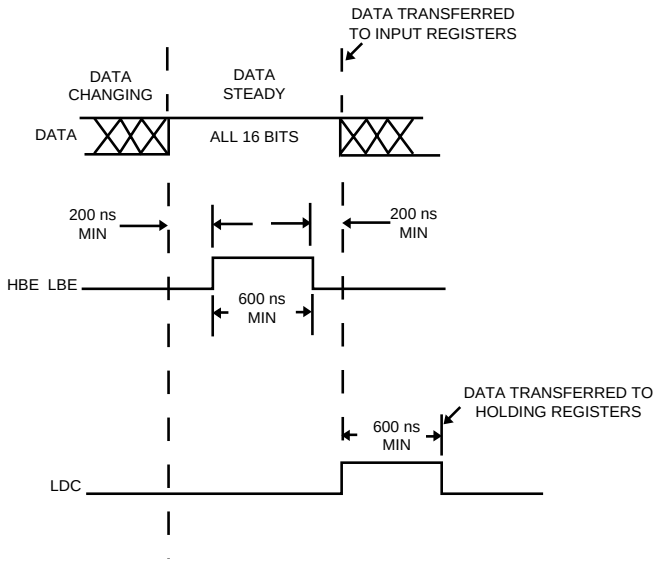


FIGURE 7. TIMING FOR 16-BIT BUS TRANSFER

DIGITAL-TO-RESOLVER/SYNCHRO CONVERTERS

The DR-11800 provides single-ended sin/cos outputs. FIGURE 8 shows the DR-11800 connected as a 4-Wire Digital-to-Resolver Converter (S1, S2, S3, and S4) using external Power Amplifiers and transformers.

FIGURE 9 shows the DR-11800 connected as a 3-Wire Digital-to-Synchro Converter (S1, S2, and S3) using external Power Amplifiers and transformers.

POWER SUPPLY DECOUPLING

Decoupling capacitors are recommended on the $+V_S$ and $-V_S$ supplies. A 1 μF tantalum capacitor in parallel with a 0.01 μF ceramic capacitor should be mounted as close to the supply as possible.

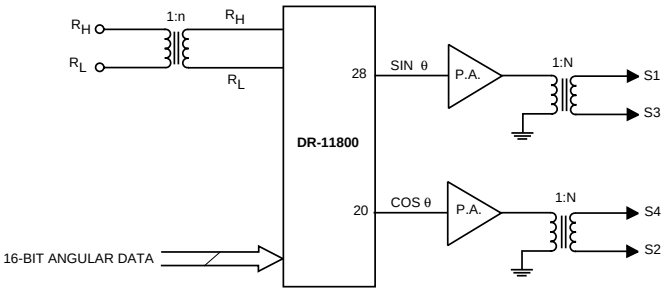


FIGURE 8. 4-WIRE DIGITAL-TO-RESOLVER CONVERTER

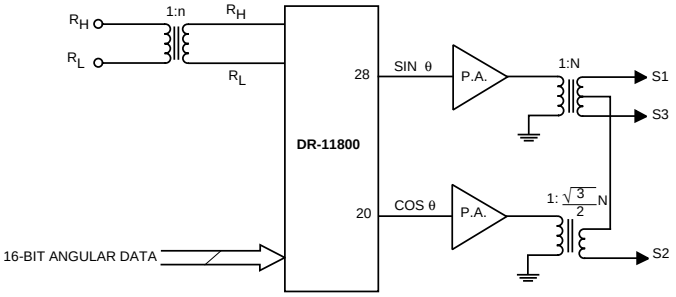


FIGURE 9. 3-WIRE DIGITAL-TO-SYNCHRO CONVERTER

TABLE 2. DR-11800 PINOUTS			
PIN	**FUNCTION**	**PIN**	**FUNCTION**
1	B1	15	B13
2	B2	16	B14
3	B3	17	B15
4	B4	18	B16
5	B5	19	LDC
6	B6	20	COS θ
7	B7	21	RL115
8	B8	22	RL26
9	HBE	23	GND
10	LBE	24	+Vs
11	B9	25	-Vs
12	B10	26	RH26
13	B11	27	RH115
14	B12	28	SIN θ

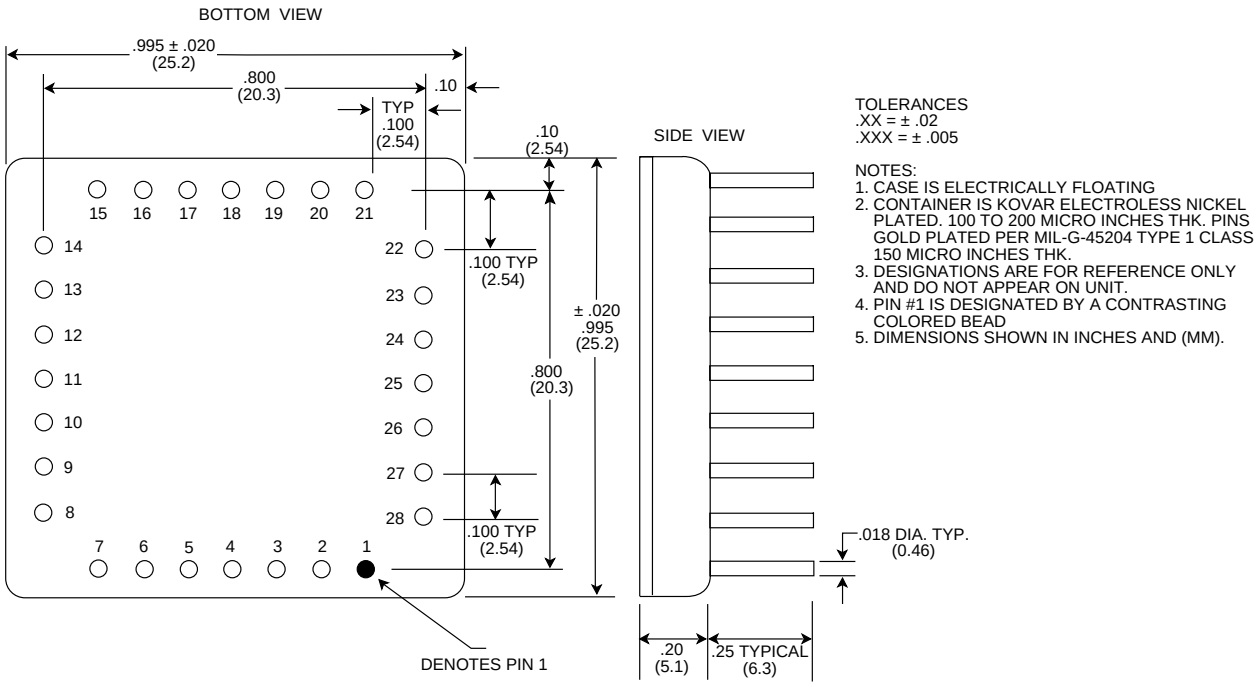


FIGURE 10. DR-11800 MECHANICAL OUTLINE

ORDERING INFORMATION

DR-11800DX-XXXX

Supplemental Process Requirements:
- S = Pre-Cap Source Inspection
- L = Pull Test
- Q = Pull Test and Pre-Cap Inspection
- K = One Lot Date Code
- W = One Lot Date Code and PreCap Source
- Y = One Lot Date Code and 100% Pull Test
- Z = One Lot Date Code, PreCap Source and 100% Pull Test
- Blank = None of the Above

Accuracy:
- 3 = ±4 Minutes
- 4 = ±2 Minutes
- 5 = ±1 Minute

Process Requirements*:
- 0 = Standard DDC Processing, no Burn-In (See table below.)
- 2 = B*
- 6 = B* with PIND Testing
- 7 = B* with Solder Dip
- 8 = B* with PIND Testing and Solder Dip
- 9 = Standard DDC Processing with Solder Dip, no Burn-In (See table below.)

Temperature Grade/Data Requirements:
- 1 = -55°C to +125°C
- 2 = -40°C to +85°C
- 3 = 0°C to +70°C
- 4 = -55°C to +125°C with Variables Test Data
- 5 = -40°C to +85°C with Variables Test Data
- 8 = 0°C to +70°C with Variables Test Data

Frequency Range:
- 4 = DC to 1 kHz

* For availability of Fully Compliant MIL-PRF-38534 parts, please contact the DDC office nearest you.
**Standard DDC Processing with burn-in and full temperature test — see table below.

STANDARD DDC PROCESSING		
TEST	**MIL-STD-883**	
	METHOD(S)	**CONDITION(S)**
INSPECTION	2009, 2010, 2017, and 2032	—
SEAL	1014	A and C
TEMPERATURE CYCLE	1010	C
CONSTANT ACCELERATION	2001	A
BURN-IN	1015, Table 1	—

105 Wilbur Place, Bohemia, New York 11716-2482

For Technical Support - 1-800-DDC-5757 ext. 7389 or 7413

Headquarters - Tel: (631) 567-5600 ext. 7389 or 7413, Fax: (631) 567-7358
Southeast - Tel: (703) 450-7900, Fax: (703) 450-6610
West Coast - Tel: (714) 895-9777, Fax: (714) 895-4988
Europe - Tel: +44-(0)1635-811140, Fax: +44-(0)1635-32264
Asia/Pacific - Tel: +81-(0)3-3814-7688, Fax: +81-(0)3-3814-7689
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