

Features

- SRAM Cache Memory for 10ns Random Reads Within a Page
- Fast 4Mbit DRAM Array for 25ns Access to Any New Page
- Write Posting Register for 10ns Random Writes and Burst Writes Within a Page (Hit or Miss)
- On-chip Cache Hit/Miss Comparators Maintains Cache Coherency on Writes

- Up to 100MHz Non-interleave Burst Rate
- Hidden Precharge and Refresh Cycles
- Extended 64ms Refresh Period for Low Standby Power
- Standard CMOS/TTL Compatible I/O Levels and +5 Volt Supply

Description

Enhanced Memory Systems has reduced the production feature size of the enhanced DRAM products now in production. This improvement results in higher speed 10ns EDRAM products operating a lower power and with less I/O capacitance. These products provide 10ns random access read or write cycle time within a page of memory. Random data in other pages can be accessed in just 25ns. The 10ns EDRAM products support read or write burst rates of up to 100MHz without interleaving. The 10ns EDRAM approaches the random access speed of fast SRAM products but with higher density and lower cost/bit. The new EDRAM enables high performance applications previously unattainable due to the slow performance of standard DRAM or cache plus DRAM systems or due to the high cost and low density of fast SRAM.

This product addendum describes the product nomenclature, switching characteristics, I/O capacitance, and operating current specifications for the new products. For detailed architecture and functional descriptions, other electrical characteristics, timing diagrams, and package outline drawings, please refer to the datasheets for the 12ns versions of each EDRAM product.

Products

Part Number	Organization
DM2200J-10	4Mx1 EDRAM
DM2202J-10	1Mx4 EDRAM
DM2212J-10	1Mx4 EDRAM
DM1M32SJ-10	1Mx32 EDRAM
DM1M36SJ-10	1Mx36 EDRAM
DM2M32SJ-10	2Mx32 EDRAM
DM2M36SJ-10	2Mx36 EDRAM
DM4M36SJ-10	4Mx32 EDRAM
DM2240J-10	4Mx1 Multibank EDO EDRAM
DM2242J-10	1Mx4 Multibank EDO EDRAM
DM2252J-10	1Mx4 Multibank EDO EDRAM
DM1M32SJ6-10	1Mx32 Multibank EDO EDRAM
DM1M36SJ6-10	1Mx36 Multibank EDO EDRAM
DM2M32SJ6-10	2Mx32 Multibank EDO EDRAM
DM2M36SJ6-10	2Mx36 Multibank EDO EDRAM
DM4M36SJ6-10	4Mx32 Multibank EDO EDRAM

Comparison of Key DRAM Specifications

Spec	EDRAM (-10)	SDRAM (-10)	RDRAM (-600)	EDO DRAM (-50)	Fast Page DRAM (-50)	Comment
t _{RAC}	25	58.5	72.6	50	50	Row Access Time (ns)
t _{AA} (t _{AC})	10	28.5	46.1	25	25	Column Access Time (ns)
t _{CAC} (t _{GQV})	5	8.5	1.2	13	13	Output Enable Access Time (ns)
Page Miss Access	25	90	99	90	90	Page Miss Access Time (ns)
t _{PC}	10	10	1.65	20	30	Page Cycle Time (ns)
t _{RP}	15	30	26.5	30	30	Precharge Time (ns)
t _C	45	90	99	90	90	Cycle Time (ns)
Sustained B/W	582	267	231	230	178	Page Miss + 32 Bytes (MB/Sec)
t _{REF}	64 ms	64 ms	32 ms	64 ms	64 ms	Refresh Time (ms)

Switching Characteristics

V_{CC} = 5V ± 5%, T_A = 0 to 70°C, C_L = 50 pf

Symbol	Description	-10		-12		Units
		Min	Max	Min	Max	
t _{AC} ⁽¹⁾	Column Address Access Time for Addresses A ₀₋₈		10		12	ns
t _{AC1} ⁽¹⁾	Column Address Access Time for Addresses A ₉ and A ₁₀		8		8	ns
t _{ACH}	Column Address Valid to /CAL Inactive (Write Cycle)	10		12		ns
t _{AQX}	Column Address Change to Output Data Invalid for Addresses A ₀₋₈	5		5		ns
t _{AQX1}	Column Address Change to Output Data Invalid for Addresses A ₉ and A ₁₀	1		1		ns
t _{ASC}	Column Address Setup Time	3		5		ns
t _{ASR}	Row Address Setup Time	3		5		ns
t _C	Row Enable Cycle Time	45		55		ns
t _{C1}	Row Enable Cycle Time, Cache Hit (Row=LRR), Read Cycle Only	16		20		ns
t _{CAE}	Column Address Latch Active Time	4		5		ns
t _{CAH}	Column Address Hold Time	0		0		ns
t _{CH}	Column Address Latch High Time (Latch Transparent)	3		5		ns
t _{CHR}	/CAL Inactive Lead Time to /RE Inactive (Write Cycles Only)	-2		-2		ns
t _{CHW}	Column Address Latch High to Write Enable Low (Multiple Writes)	0		0		ns
t _{CLV}	Column Address Latch High to Data Valid		7		7	ns
t _{CQH}	Column Address Latch Low to Data Invalid	3		3		ns
t _{ACI}	Column Address Valid to /CAL Inactive		10		12	ns
t _{CQV}	Column Address Latch High to Data Valid		10		15	ns
t _{CQX}	Column Address Latch Inactive to Data Invalid for Addresses A ₀₋₈	5		5		ns
t _{CQX1}	Column Address Latch Inactive to Data Invalid for Addresses A ₉ and A ₁₀	1		1		ns
t _{CRP}	Column Address Latch Setup Time to Row Enable	3		5		ns
t _{CWL}	/WE Low to /CAL Inactive	3		5		ns
t _{DH}	Data Input Hold Time	0		0		ns
t _{DS}	Data Input Setup Time	3		5		ns
t _{DMH}	Mask Hold Time From Row Enable (Write-Per-Bit)		0		1	ns
t _{DMS}	Mask Setup Time to Row Enable (Write-Per-Bit)	3		5		ns
t _{GQV} ⁽¹⁾	Output Enable Access Time		5		5	ns
t _{GQX} ^(2,3)	Output Enable to Output Drive Time	0	5	0	5	ns
t _{GQZ} ^(4,5)	Output Turn-Off Delay From Output Disabled (/G↑)	0	5	0	5	ns
t _{MH}	/F and W/R Mode Select Hold Time	0		0		ns
t _{MSU}	/F and W/R Mode Select Setup Time	3		5		ns
t _{NRH}	/CAL, /G, and /WE Hold Time For /RE-Only Refresh	0		0		ns
t _{NRS}	/CAL, /G, and /WE Setup Time For /RE-Only Refresh	3		5		ns
t _{PC}	Column Address Latch Cycle Time	10		12		ns
t _{RAC} ⁽¹⁾	Row Enable Access Time, On a Cache Miss		25		30	ns
t _{RAC1} ⁽¹⁾	Row Enable Access Time, On a Cache Hit (Limit Becomes t _{AC})		13		16	ns
t _{RAC2} ^(1,6)	Row Enable Access Time for a Cache Write Hit		25		30	ns
t _{RAH}	Row Address Hold Time	0		1		ns

Switching Characteristics

V_{CC} = 5V ± 5%, T_A = 0 to 70°C, C_L = 50 pF

Symbol	Description	-10		-12		Units
		Min	Max	Min	Max	
t _{RE}	Row Enable Active Time	25	100000	30	100000	ns
t _{RE1}	Row Enable Active Time, Cache Hit (Row=LRR) Read Cycle	8		8		ns
t _{REF}	Refresh Period		64		64	ms
t _{RGX}	Output Enable Don't Care From Row Enable (Write, Cache Miss), O/P Hi Z	9		9		ns
t _{RQX1}	Row Enable High to Output Turn-On After Write Miss		10		12	ns
t _{RP}	Row Precharge Time	15		20		ns
t _{RP1}	Row Precharge Time, Cache Hit (Row=LRR) Read Cycle	8		8		ns
t _{RP2}	Row Precharge Time, Self-Refresh Mode	100		100		ns
t _{RRH}	Read Hold Time From Row Enable (Write Only)	0		0		ns
t _{RSH}	Last Write Address Latch to End of Write	10		12		ns
t _{RSW}	Row Enable to Column Address Latch Low For Second Write	30		35		ns
t _{RWL}	Last Write Enable to End of Write	10		12		ns
t _{SC}	Column Address Cycle Time	10		12		ns
t _{SHR}	Select Hold From Row Enable	0		0		ns
t _{SQV}	Chip Select Access Time		10		12	ns
t _{SQX}	Output Turn-On From Select Low	0	10	0	12	ns
t _{SQZ}	Output Turn-Off From Chip Select	0	8	0	8	ns
t _{SSR}	Select Setup Time to Row Enable	3		5		ns
t _T	Transition Time (Rise and Fall)	1	10	1	10	ns
t _{WC}	Write Enable Cycle Time	10		12		ns
t _{WCH}	Column Address Latch Low to Write Enable Inactive Time	3		5		ns
t _{WHR} ⁽⁷⁾	Write Enable Hold After /RE	0		0		ns
t _{WI}	Write Enable Inactive Time	3		5		ns
t _{WP}	Write Enable Active Time	3		5		ns
t _{WQV}	Data Valid From Write Enable High		10		12	ns
t _{WQX}	Data Output Turn-On From Write Enable High	0	10	0	12	ns
t _{WQZ}	Data Turn-Off From Write Enable Low	0	10	0	12	ns
t _{WRP}	Write Enable Setup Time to Row Enable	3		5		ns
t _{WRR}	Write to Read Recovery (Cache Miss)		10		16	ns

(1) V_{OUT} Timing Reference Point at 1.5V

(2) Parameter Defines Time When Output is Enabled (Sourcing or Sinking Current) and is Not Referenced to V_{OH} or V_{OL}

(3) Minimum Specification is Referenced from V_{IH} and Maximum Specification is Referenced from V_{IL} on Input Control Signal

(4) Parameter Defines Time When Output Achieves Open-Circuit Condition and is Not Referenced to V_{OH} or V_{OL}

(5) Minimum Specification is Referenced from V_{IL} and Maximum Specification is Referenced from V_{IH} on Input Control Signal

(6) Access Parameter Applies When /CAL Has Not Been Asserted Prior to t_{RAC2}

(7) For Write-per-Bit Devices, t_{WHR} is Limited by Data Input Setup Time, t_{DS}

**10ns EDRAM (DM2200/2202/2212)
Maximum I/O Capacitance (pf)**

Description	Max	Pins
Input Capacitance	6	A ₀₋₁₀
Input Capacitance	7	/RE, /CAL, W/R, W/E, /F, /S
Input Capacitance	3	/G
I/O Capacitance	6	DQ ₀₋₃
Input Capacitance	6	D
Output Capacitance	6	Q

10ns EDRAM SIMM Operating Current (ma)

Symbol	Operating Current	DM2200	DM2202	DM2212
I _{CC1}	Random Read	180	180	180
I _{CC2}	Fast Page Mode Read	90	90	90
I _{CC3}	Static Column Read	80	80	80
I _{CC4}	Random Write	160	160	160
I _{CC5}	Fast Page Mode Write	160	160	160
I _{CC6}	Standby	1	1	1
I _{CC7}	Low Power, Self Refresh	0.2	0.2	0.2
I _{CCT}	Average Typical Operating Current	30	30	30

10ns EDRAM SIMM Maximum I/O Capacitance (pf)

Description	DM1M32	DM1M36	DM2M32	DM2M36	DM4M32	Pins
Input Capacitance	66	73	130	136	29	A ₀₋₉
Input Capacitance	90	96	180	192	39	A ₁₀ , W/R, W/E, /F
Input Capacitance	90	96	97	100	39	/S ₀ , /S ₁
Input Capacitance	45	45	72	72	39	/RE ₀
Input Capacitance	46	56	78	94	39	/RE ₂
Input Capacitance	N/A	N/A	92	92	N/A	/RE ₃
Input Capacitance	26	28	76	76	19	/G
Input Capacitance	27	27	62	62	19	/CAL ₀₋₃
Input Capacitance		16		34		/CAL _P
I/O Capacitance	8	8	16	16	18	DQ ₃₅

10ns EDRAM SIMM Operating Current (ma)

Symbol	Operating Current	DM1M32	DM1M36S	DM2M32	DM2M36	DM4M32
I _{CC1}	Random Read	1440	1620	1448	1629	6160
I _{CC2}	Fast Page Mode Read	720	810	728	819	3280
I _{CC3}	Static Column Read	640	720	648	729	2960
I _{CC4}	Random Write	1280	1440	1288	1449	5520
I _{CC5}	Fast Page Mode Write	1280	1440	1288	1449	5520
I _{CC6}	Standby	8	9	16	18	36
I _{CC7}	Low Power, Self Refresh	1.6	1.8	3.2	3.6	10.4
I _{CCT}	Average Typical Operating Current	240	270	248	279	1160

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