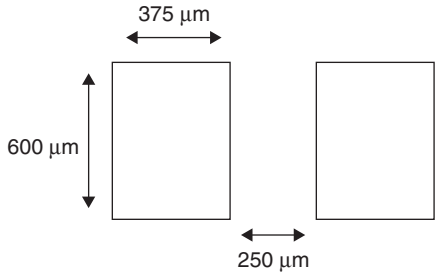
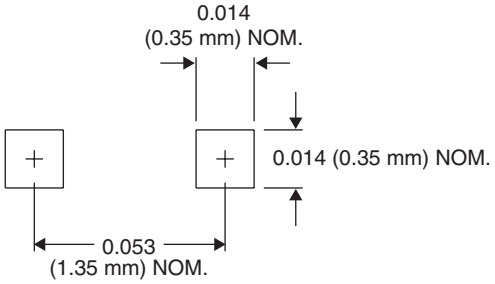
Suggested PCB Land Pattern Designs for Leaded and Leadless Packages and Detailed Surface Mount Guidelines for Leadless Packages

Below are sample printed circuit board land pattern dimensions. These are based on the IPC (Institute for Interconnecting and Packaging Electronic Circuits) surface mount design and land pattern standard: IPC-SM-782.

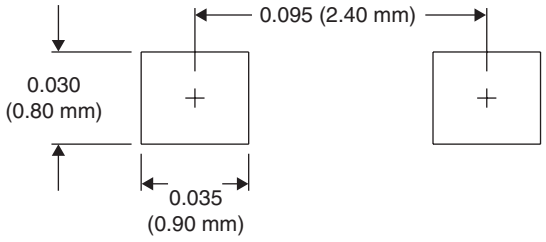
These drawings are for reference only. It is recommended that you consult with the company doing the component mounting and soldering to the printed circuit board. These companies have more information on options (various possible dimensions) of actual land patterns.



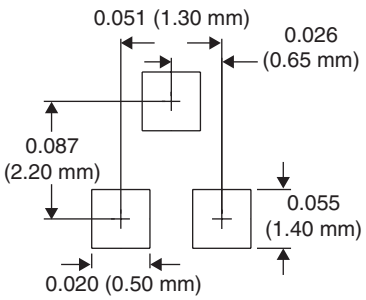
Chip Scale



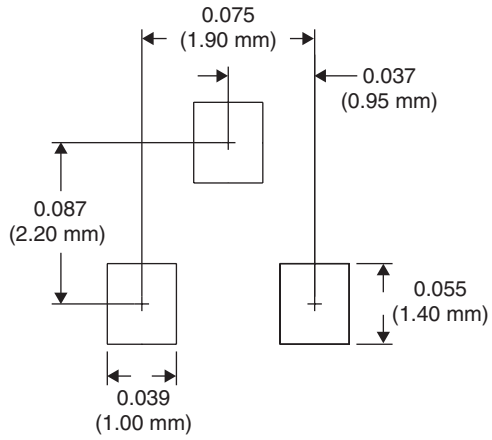
SC-79



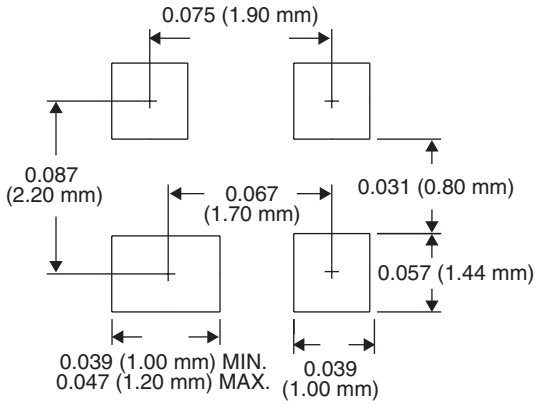
SOD-323



SC-70



SOT-23 3 Lead



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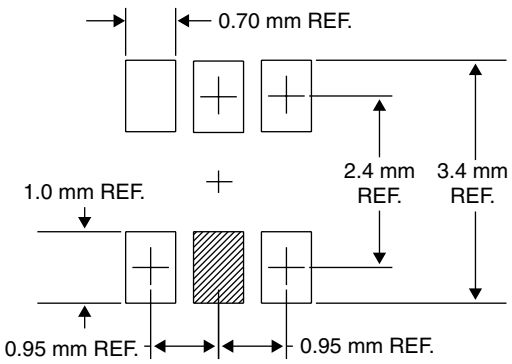
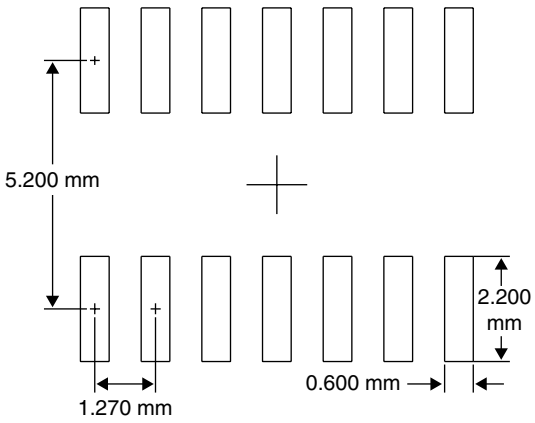
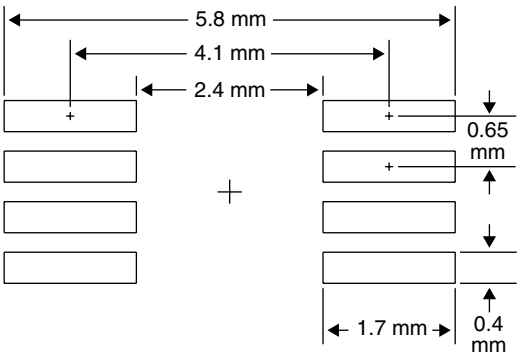


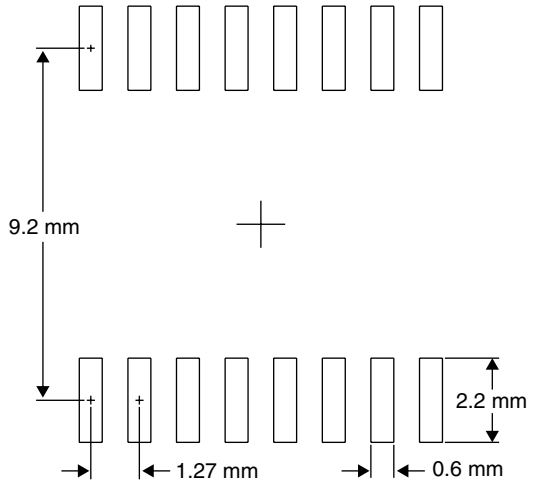
SOT-5, SOT-6



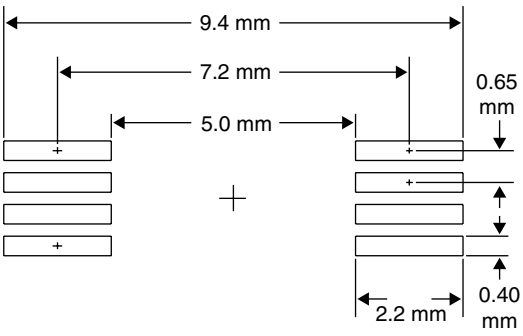
14 Lead SOIC Narrow Body



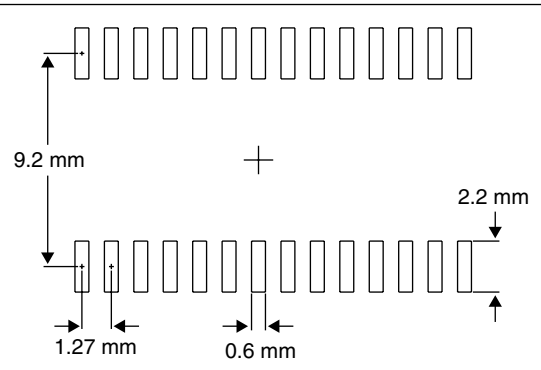
MSOP-8



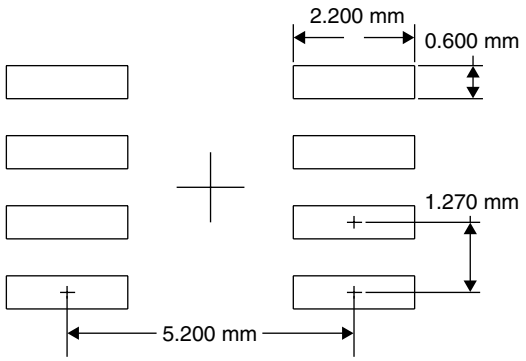
16 Lead SOIC Wide Body



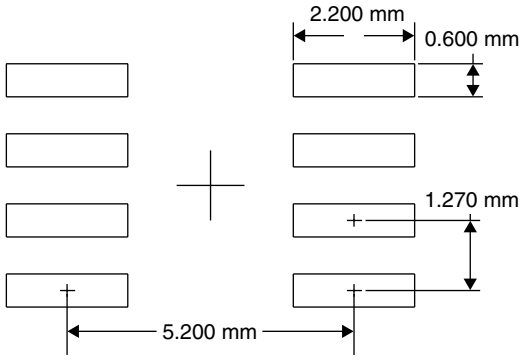
8 Lead SSOP (5.3 mm)



28 Lead SOIC Wide Body



8 Lead SOIC Narrow Body



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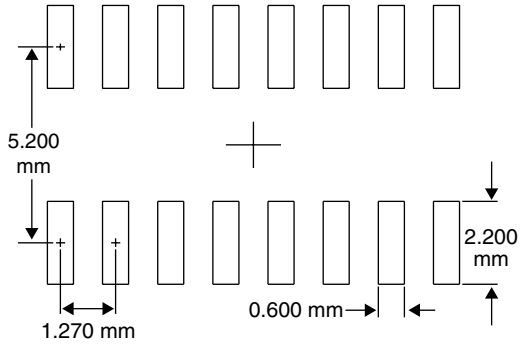
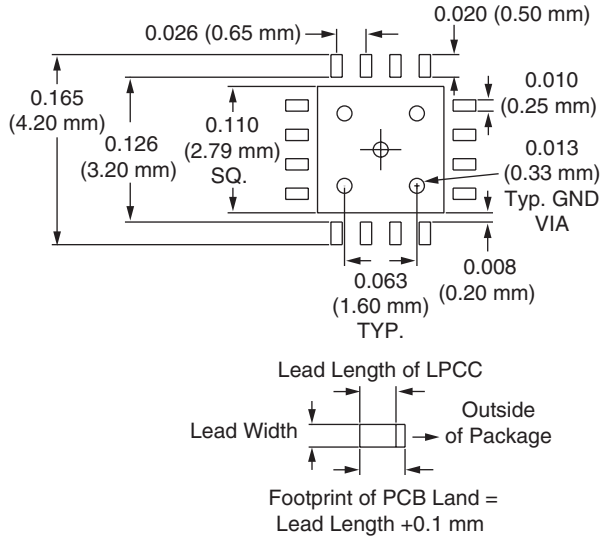
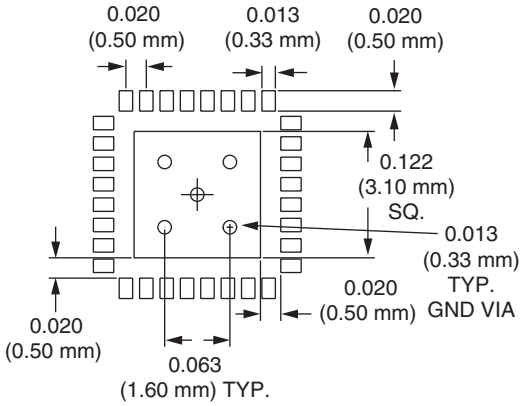


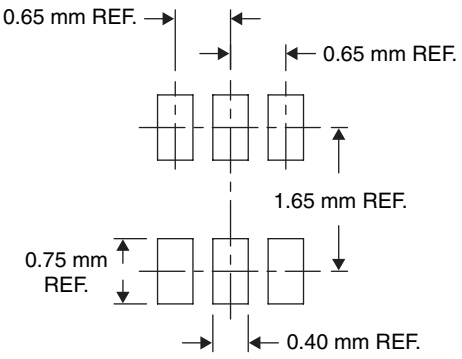
16 Lead SOIC Narrow Body



LPCC-16 Lead 4 x 4 mm (-307)
Surface Mount Land Pattern



QFN-32 Lead 5 x 5 mm (-310)
Surface Mount Land Pattern



SC-88 (6 Lead SC-70)

Detailed Surface Mount Guidelines for Leadless Packages

Skyworks' plastic encapsulated leadless style packages are being offered on several products to reduce size and weight and to improve application performance. These packages are gaining acceptance in the industry and are often referred to by such names as "QFN," "LPCC," "MLF" and others, and conform to JEDEC outline MO-220.

These packages use perimeter lands on the bottom of the package to provide contact to the PCB. These packages also have an exposed paddle on the bottom to provide a stable ground for optimum electrical performance of switches and attenuators, and an efficient heat path for thermal performance for amplifier products.

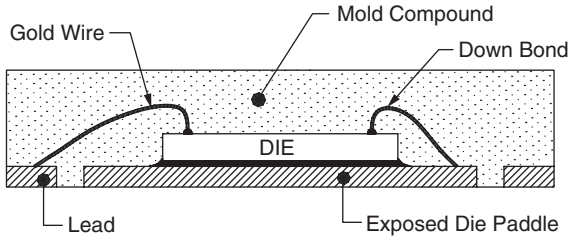


Figure 1. Package Cross Section

Within are the suggested guidelines for layout of a PCB and stencil for Skyworks' 4 x 4 mm LPCC-16.

PCB Design Guidelines

For the lead/terminal solder pad design, it is recommended to use a Non Solder Mask Defined (NSMD) approach, but a small amount of solder mask should remain between the pads to avoid solder bridging between terminals. The PCB land width should match package pad width. The PCB land length should be 0.1 mm greater than the package pad length, with the extra area on the outside of the package. See Figure 2.

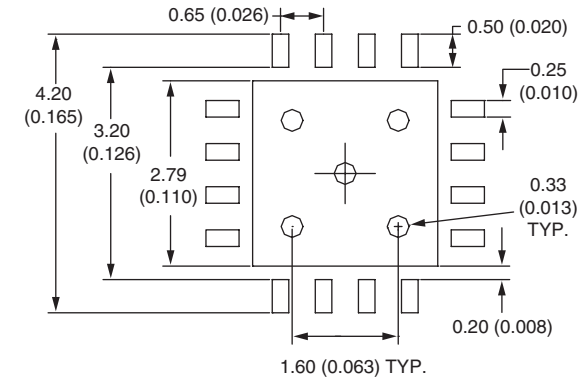


Figure 2. Surface Mount Land Pattern, 4 x 4 mm 16 Lead LPCC

The ground pad on the PCB should match the size of the exposed paddle of the package and should be Solder Mask Defined (SMD). The solder mask opening should overlap the edges of the PCB ground pad by 0.065 mm (0.0025") on all four sides. The recommended design gap between the PCB ground pad and land pad is 0.15 mm minimum to avoid solder bridging and shorting. When space is available, a gap of 0.25 mm or more is preferred.

Plated thru via holes in the PCB ground pad should be 0.33 (0.013") in diameter and plugged. If via holes cannot be plugged, it is recommended to cap the vias on the backside of the board using solder mask material. This should allow the vias to be filled with solder during reflow.

Solder Mask Design

Two types of stencil designs are used for surface mount packages:

1. Solder Mask Defined (SMD): Solder mask openings smaller than metal pads.
2. Non-Solder Mask Defined (NSMD): Solder mask openings larger than metal pads.

NSMD is recommended for the perimeter I/O lands, as this allows the solder to wrap around the sides of the metal pads on the board for a reliable solder joint.

Because the spacing between the ground pad and the land pads can be small, SMD is recommended for the ground pad to prevent solder bridging.

A stainless steel stencil, 0.125–0.150 mm (0.005–0.006") thick, is recommended for solder paste application. For better paste release, the aperture walls should be trapezoidal and the corners rounded.

For the terminal lands, the stencil opening should be 0.05 mm larger than the PCB land (0.025 mm in each direction).

For the ground pad area, it is recommended to screen the solder paste in an array of small openings rather than one large opening. The total (cumulative) area of all the openings should be approximately equal to 50% of the total ground pad area. This will ensure good solder coverage with fewer voids. See Figure 3.

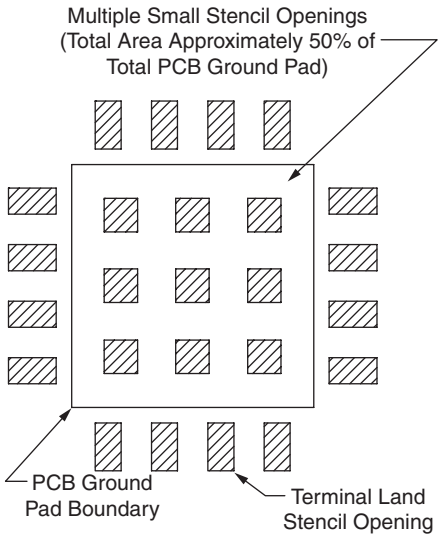


Figure 3. Recommended Stencil Design

Solder Paste and Reflow Profile

Because leadless packages have a low stand-off height and small terminal pitch, a No Clean, Type 3 solder paste, and a convection/IR reflow is recommended.

Sn63 (63% Sn, 37% Pb) solder is preferred because it is a eutectic compound with a melting point of 183°C. The reflow temperature in this case would be above 183°C for 30–60 seconds, with a peak temperature of 205–210°C.

If a lead-free alloy is used, such as tin/silver or tin/silver/copper, the melting point is 221°C and 217°C respectively. In this case, the profile would be above 221/217°C for 30–60 seconds, with a peak temperature of 230–240°C. Maximum temperature should not exceed 240°C.

A typical reflow profile is presented in Figure 4, which could be used as a starting point. The actual profile used will depend on the thermal mass of the entire populated board and the solder compound used.

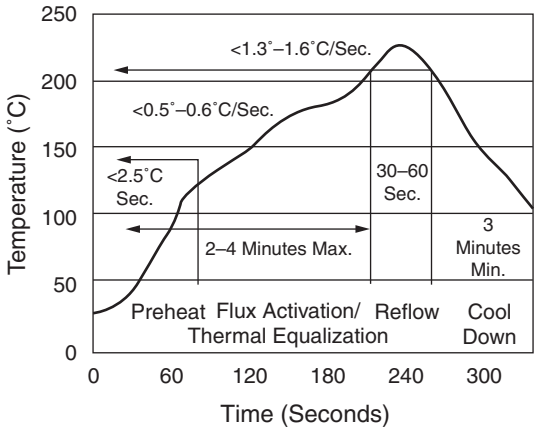


Figure 4. Typical Solder Reflow Profile