

## ADG708/ADG709

### FEATURES

- 1.8 V to 5.5 V Single Supply
- $\pm 2.5$  V Dual Supply
- 3  $\Omega$  ON Resistance
- 0.75  $\Omega$  ON Resistance Flatness
- 100 pA Leakage Currents
- 14 ns Switching Times
- Single 8-to-1 Multiplexer ADG708
- Differential 4-to-1 Multiplexer ADG709
- 16-Lead TSSOP Package
- Low Power Consumption
- TTL-/CMOS-Compatible Inputs

### APPLICATIONS

- Data Acquisition Systems
- Communication Systems
- Relay Replacement
- Audio and Video Switching
- Battery-Powered Systems

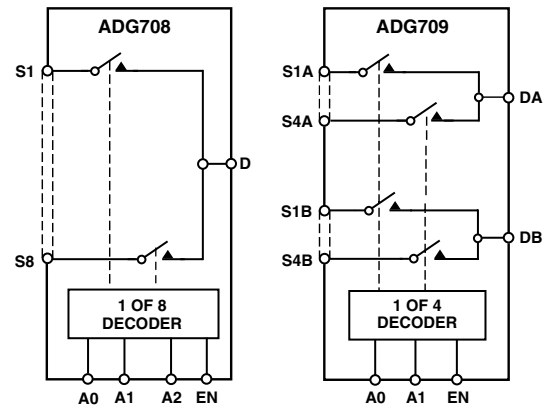
### GENERAL DESCRIPTION

The ADG708 and ADG709 are low voltage, CMOS analog multiplexers comprising eight single channels and four differential channels, respectively. The ADG708 switches one of eight inputs (S1–S8) to a common output, D, as determined by the 3-bit binary address lines A0, A1, and A2. The ADG709 switches one of four differential inputs to a common differential output as determined by the 2-bit binary address lines A0 and A1. An EN input on both devices is used to enable or disable the device. When disabled, all channels are switched OFF.

Low power consumption and an operating supply range of 1.8 V to 5.5 V make the ADG708 and ADG709 ideal for battery-powered, portable instruments. All channels exhibit break-before-make switching action preventing momentary shorting when switching channels.

These switches are designed on an enhanced submicron process that provides low power dissipation yet gives high switching

### FUNCTIONAL BLOCK DIAGRAMS



speed, very low ON resistance, and leakage currents. ON resistance is in the region of a few ohms and is closely matched between switches and very flat over the full signal range. These parts can operate equally well as either multiplexers or demultiplexers and have an input signal range that extends to the supplies.

The ADG708 and ADG709 are available in a 16-lead TSSOP package.

### PRODUCT HIGHLIGHTS

1. Single-/dual-supply operation. The ADG708 and ADG709 are fully specified and guaranteed with 3 V and 5 V single-supply and  $\pm 2.5$  V dual-supply rails.
2. Low  $R_{ON}$  (3  $\Omega$  typical).
3. Low power consumption ( $< 0.01$   $\mu$ W).
4. Guaranteed break-before-make switching action.
5. Small 16-lead TSSOP package.

### REV. A

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.

# ADG708/ADG709—SPECIFICATIONS<sup>1</sup> ( $V_{DD} = 5\text{ V} \pm 10\%$ , $V_{SS} = 0\text{ V}$ , $GND = 0\text{ V}$ , unless otherwise noted.)

Parameter	B Version		C Version		Unit	Test Conditions/Comments
	+25°C	-40°C to +85°C	+25°C	-40°C to +85°C		
<b>ANALOG SWITCH</b>						
Analogue Signal Range	0 V to $V_{DD}$		0 V to $V_{DD}$		V	$V_S = 0\text{ V to }V_{DD}$ , $I_{DS} = 10\text{ mA}$ ; Test Circuit 1
ON Resistance ( $R_{ON}$ )	3		3		$\Omega$ typ	
	4.5	5	4.5	5	$\Omega$ max	
ON Resistance Match Between Channels ( $\Delta R_{ON}$ )		0.4		0.4	$\Omega$ typ	$V_S = 0\text{ V to }V_{DD}$ , $I_{DS} = 10\text{ mA}$ $V_S = 0\text{ V to }V_{DD}$ , $I_{DS} = 10\text{ mA}$
		0.8		0.8	$\Omega$ max	
ON Resistance Flatness ( $R_{FLAT(ON)}$ )	0.75		0.75		$\Omega$ typ	
		1.2		1.2	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>						
Source OFF Leakage $I_S$ (OFF)	$\pm 0.01$		$\pm 0.01$		nA typ	$V_{DD} = 5.5\text{ V}$ $V_D = 4.5\text{ V/1 V}$ , $V_S = 1\text{ V/4.5 V}$ ; Test Circuit 2
		$\pm 20$	$\pm 0.1$	$\pm 0.3$	nA max	
Drain OFF Leakage $I_D$ (OFF)	$\pm 0.01$		$\pm 0.01$		nA typ	$V_D = 4.5\text{ V/1 V}$ , $V_S = 1\text{ V/4.5 V}$ ; Test Circuit 3
		$\pm 20$	$\pm 0.1$	$\pm 0.75$	nA max	
Channel ON Leakage $I_D$ , $I_S$ (ON)	$\pm 0.01$		$\pm 0.01$		nA typ	$V_D = V_S = 1\text{ V or }4.5\text{ V}$ ; Test Circuit 4
		$\pm 20$	$\pm 0.1$	$\pm 0.75$	nA max	
<b>DIGITAL INPUTS</b>						
Input High Voltage, $V_{INH}$	2.4		2.4		V min	$V_{IN} = V_{INL}$ or $V_{INH}$
Input Low Voltage, $V_{INL}$	0.8		0.8		V max	
Input Current $I_{INL}$ or $I_{INH}$	0.005		0.005		$\mu\text{A}$ typ	
		$\pm 0.1$		$\pm 0.1$	$\mu\text{A}$ max	
$C_{IN}$ , Digital Input Capacitance	2		2		pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>						
$t_{TRANSITION}$	14		14		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; Test Circuit 5 $V_{S1} = 3\text{ V/0 V}$ , $V_{S8} = 0\text{ V/3 V}$
		25		25	ns max	
Break-Before-Make Time Delay, $t_D$	8		8		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 3\text{ V}$ ; Test Circuit 6
		1		1	ns min	
$t_{ON(EN)}$	14		14		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 3\text{ V}$ ; Test Circuit 7
		25		25	ns max	
$t_{OFF(EN)}$	7		7		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 3\text{ V}$ ; Test Circuit 7
		12		12	ns max	
Charge Injection	$\pm 3$		$\pm 3$		pC typ	$V_S = 2.5\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; Test Circuit 8
Off Isolation	-60		-60		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$ $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Test Circuit 9
	-80		-80		dB typ	
Channel-to-Channel Crosstalk	-60		-60		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$ $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Test Circuit 10
	-80		-80		dB typ	
-3 dB Bandwidth	55		55		MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; Test Circuit 11 $f = 1\text{ MHz}$
$C_S$ (OFF)	13		13		pF typ	
$C_D$ (OFF)						
ADG708	85		85		pF typ	$f = 1\text{ MHz}$
ADG709	42		42		pF typ	$f = 1\text{ MHz}$
$C_D$ , $C_S$ (ON)						
ADG708	96		96		pF typ	$f = 1\text{ MHz}$
ADG709	48		48		pF typ	$f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>						
$I_{DD}$	0.001		0.001		$\mu\text{A}$ typ	$V_{DD} = 5.5\text{ V}$ Digital Inputs = 0 V or 5.5 V
		1.0		1.0	$\mu\text{A}$ max	

## NOTES

<sup>1</sup>Temperature range is as follows: B and C Versions: -40°C to +85°C.

<sup>2</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SPECIFICATIONS<sup>1</sup>(V<sub>DD</sub> = 3 V ± 10%, V<sub>SS</sub> = 0 V, GND = 0 V, unless otherwise noted.)

Parameter	B Version		C Version		Unit	Test Conditions/Comments
	+25°C	-40°C to +85°C	+25°C	-40°C to +85°C		
<b>ANALOG SWITCH</b>						
Analog Signal Range		0 V to V <sub>DD</sub>		0 V to V <sub>DD</sub>	V	
ON Resistance (R <sub>ON</sub> )	8		8		Ω typ	V <sub>S</sub> = 0 V to V <sub>DD</sub> , I <sub>DS</sub> = 10 mA;
	11	12	11	12	Ω max	Test Circuit 1
ON Resistance Match Between Channels (ΔR <sub>ON</sub> )		0.4		0.4	Ω typ	V <sub>S</sub> = 0 V to V <sub>DD</sub> , I <sub>DS</sub> = 10 mA
		1.2		1.2	Ω max	
<b>LEAKAGE CURRENTS</b>						
Source OFF Leakage I <sub>S</sub> (OFF)	±0.01		±0.01		nA typ	V <sub>DD</sub> = 3.3 V
		±20	±0.1	±0.3	nA max	V <sub>S</sub> = 3 V/1 V, V <sub>D</sub> = 1 V/3 V;
Drain OFF Leakage I <sub>D</sub> (OFF)	±0.01		±0.01		nA typ	Test Circuit 2
		±20	±0.1	±0.75	nA max	V <sub>S</sub> = 3 V/1 V, V <sub>D</sub> = 1 V/3 V;
Channel ON Leakage I <sub>D</sub> , I <sub>S</sub> (ON)	±0.01		±0.01		nA typ	Test Circuit 3
		±20	±0.1	±0.75	nA max	V <sub>S</sub> = V <sub>D</sub> = 1 V or 3 V; Test Circuit 4
<b>DIGITAL INPUTS</b>						
Input High Voltage, V <sub>INH</sub>		2.0		2.0	V min	
Input Low Voltage, V <sub>INL</sub>		0.8		0.8	V max	
Input Current						
I <sub>INL</sub> or I <sub>INH</sub>	0.005		0.005		μA typ	V <sub>IN</sub> = V <sub>INL</sub> or V <sub>INH</sub>
		±0.1		±0.1	μA max	
C <sub>IN</sub> , Digital Input Capacitance	2		2		pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>						
t <sub>TRANSITION</sub>	18		18		ns typ	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF; Test Circuit 5
		30		30	ns max	V <sub>S1</sub> = 2 V/0 V, V <sub>S2</sub> = 0 V/2 V
Break-Before-Make Time Delay, t <sub>D</sub>	8		8		ns typ	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF
		1		1	ns min	V <sub>S</sub> = 2 V; Test Circuit 6
t <sub>ON</sub> (EN)	18		18		ns typ	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF
		30		30	ns max	V <sub>S</sub> = 2 V; Test Circuit 7
t <sub>OFF</sub> (EN)	8		8		ns typ	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF
		15		15	ns max	V <sub>S</sub> = 2 V; Test Circuit 7
Charge Injection	±3		±3		pC typ	V <sub>S</sub> = 1.5 V, R <sub>S</sub> = 0 Ω, C <sub>L</sub> = 1 nF;
						Test Circuit 8
Off Isolation	-60		-60		dB typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 10 MHz
	-80		-80		dB typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz;
						Test Circuit 9
Channel-to-Channel Crosstalk	-60		-60		dB typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 10 MHz
	-80		-80		dB typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz;
						Test Circuit 10
-3 dB Bandwidth	55		55		MHz typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF; Test Circuit 11
C <sub>S</sub> (OFF)	13		13		pF typ	f = 1 MHz
C <sub>D</sub> (OFF)						
ADG708	85		85		pF typ	f = 1 MHz
ADG709	42		42		pF typ	f = 1 MHz
C <sub>D</sub> , C <sub>S</sub> (ON)						
ADG708	96		96		pF typ	f = 1 MHz
ADG709	48		48		pF typ	f = 1 MHz
<b>POWER REQUIREMENTS</b>						
I <sub>DD</sub>	0.001		0.001		μA typ	V <sub>DD</sub> = 3.3 V
		1.0		1.0	μA max	Digital Inputs = 0 V or 3.3 V

## NOTES

<sup>1</sup>Temperature ranges are as follows: B and C Versions: -40°C to +85°C.<sup>2</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

# ADG708/ADG709—SPECIFICATIONS<sup>1</sup>

**DUAL SUPPLY** ( $V_{DD} = +2.5\text{ V} \pm 10\%$ ,  $V_{SS} = -2.5\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ , unless otherwise noted.)

Parameter	B Version -40°C +25°C to +85°C		C Version -40°C +25°C to +85°C		Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>						
Analog Signal Range	$V_{SS}$ to $V_{DD}$		$V_{SS}$ to $V_{DD}$		V	
ON Resistance ( $R_{ON}$ )	2.5		2.5		$\Omega$ typ	$V_S = V_{SS}$ to $V_{DD}$ , $I_{DS} = 10\text{ mA}$ ; Test Circuit 1
	4.5	5	4.5	5	$\Omega$ max	
ON Resistance Match Between Channels ( $\Delta R_{ON}$ )		0.4		0.4	$\Omega$ typ	
		0.8		0.8	$\Omega$ max	$V_S = V_{SS}$ to $V_{DD}$ , $I_{DS} = 10\text{ mA}$
ON Resistance Flatness ( $R_{FLAT(ON)}$ )	0.6		0.6		$\Omega$ typ	$V_S = V_{SS}$ to $V_{DD}$ , $I_{DS} = 10\text{ mA}$
		1.0		1.0	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>						
Source OFF Leakage $I_S$ (OFF)	$\pm 0.01$		$\pm 0.01$		nA typ	$V_{DD} = +2.75\text{ V}$ , $V_{SS} = -2.75\text{ V}$ $V_S = +2.25\text{ V}/-1.25\text{ V}$ , $V_D = -1.25\text{ V}/+2.25\text{ V}$ ; Test Circuit 2
		$\pm 20$	$\pm 0.1$	$\pm 0.3$	nA max	
Drain OFF Leakage $I_D$ (OFF)	$\pm 0.01$		$\pm 0.01$		nA typ	$V_S = +2.25\text{ V}/-1.25\text{ V}$ , $V_D = -1.25\text{ V}/+2.25\text{ V}$ ; Test Circuit 3
		$\pm 20$	$\pm 0.1$	$\pm 0.75$	nA max	
Channel ON Leakage $I_D$ , $I_S$ (ON)	$\pm 0.01$		$\pm 0.01$		nA typ	$V_S = V_D = +2.25\text{ V}/-1.25\text{ V}$ ; Test Circuit 4
		$\pm 20$	$\pm 0.1$	$\pm 0.75$	nA max	
<b>DIGITAL INPUTS</b>						
Input High Voltage, $V_{INH}$		1.7		1.7	V min	
Input Low Voltage, $V_{INL}$		0.7		0.7	V max	
Input Current $I_{INL}$ or $I_{INH}$	0.005		0.005		$\mu\text{A}$ typ	$V_{IN} = V_{INL}$ or $V_{INH}$
		$\pm 0.1$		$\pm 0.1$	$\mu\text{A}$ max	
$C_{IN}$ , Digital Input Capacitance	2		2		pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>						
$t_{TRANSITION}$	14		14		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; Test Circuit 5
		25		25	ns max	$V_S = 1.5\text{ V}/0\text{ V}$ ; Test Circuit 5
Break-Before-Make Time Delay, $t_D$	8		8		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
		1		1	ns min	$V_S = 1.5\text{ V}$ ; Test Circuit 6
$t_{ON(EN)}$	14		14		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
		25		25	ns max	$V_S = 1.5\text{ V}$ ; Test Circuit 7
$t_{OFF(EN)}$	8		8		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
		15		15	ns max	$V_S = 1.5\text{ V}$ ; Test Circuit 7
Charge Injection	$\pm 3$		$\pm 3$		pC typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; Test Circuit 8
Off Isolation	-60		-60		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$
	-80		-80		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Test Circuit 9
Channel-to-Channel Crosstalk	-60		-60		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$
	-80		-80		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Test Circuit 10
-3 dB Bandwidth	55		55		MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; Test Circuit 11
$C_S$ (OFF)	13		13		pF typ	$f = 1\text{ MHz}$
$C_D$ (OFF)						
ADG708	85		85		pF typ	$f = 1\text{ MHz}$
ADG709	42		42		pF typ	$f = 1\text{ MHz}$
$C_D$ , $C_S$ (ON)						
ADG708	96		96		pF typ	$f = 1\text{ MHz}$
ADG709	48		48		pF typ	$f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>						
$I_{DD}$	0.001		0.001		$\mu\text{A}$ typ	$V_{DD} = 2.75\text{ V}$ Digital Inputs = 0 V or 2.75 V
		1.0		1.0	$\mu\text{A}$ max	
$I_{SS}$	0.001		0.001		$\mu\text{A}$ typ	$V_{SS} = -2.75\text{ V}$ Digital Inputs = 0 V or 2.75 V
		1.0		1.0	$\mu\text{A}$ max	

## NOTES

<sup>1</sup>Temperature range is as follows: B and C Versions:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

<sup>2</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

(T<sub>A</sub> = 25°C, unless otherwise noted.)

V <sub>DD</sub> to V <sub>SS</sub> .....	7 V
V <sub>DD</sub> to GND .....	-0.3 V to +7 V
V <sub>SS</sub> to GND .....	+0.3 V to -3.5 V
Analog Inputs <sup>2</sup> .....	V <sub>SS</sub> - 0.3 V to V <sub>DD</sub> + 0.3 V or 30 mA, Whichever Occurs First
Digital Inputs <sup>2</sup> .....	-0.3 V to V <sub>DD</sub> + 0.3 V or 30 mA, Whichever Occurs First
Peak Current, S or D .....	100 mA (Pulsed at 1 ms, 10% Duty Cycle Max)
Continuous Current, S or D .....	30 mA
Operating Temperature Range	
Industrial (B and C Versions) .....	-40°C to +85°C
Storage Temperature Range .....	-65°C to +150°C
Junction Temperature .....	150°C

TSSOP Package, Power Dissipation .....	432 mW
θ <sub>JA</sub> Thermal Impedance .....	150.4°C/W
θ <sub>JC</sub> Thermal Impedance .....	27.6°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec) .....	215°C
Infrared (15 sec) .....	220°C

## NOTES

<sup>1</sup>Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

<sup>2</sup>Overtolerages at A, EN, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

**Table I. ADG708 Truth Table**

A2	A1	A0	EN	Switch Condition
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

X = Don't Care

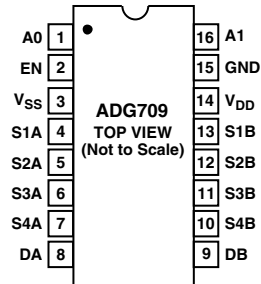
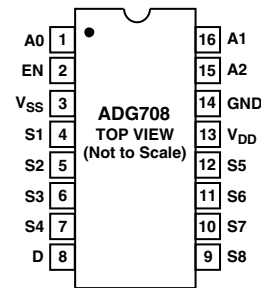
**Table II. ADG709 Truth Table**

A1	A0	EN	ON Switch Pair
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

X = Don't Care

## PIN CONFIGURATIONS

### TSSOP



## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG708BRU	-40°C to +85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG709BRU	-40°C to +85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG708CRU	-40°C to +85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG709CRU	-40°C to +85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16

## CAUTION

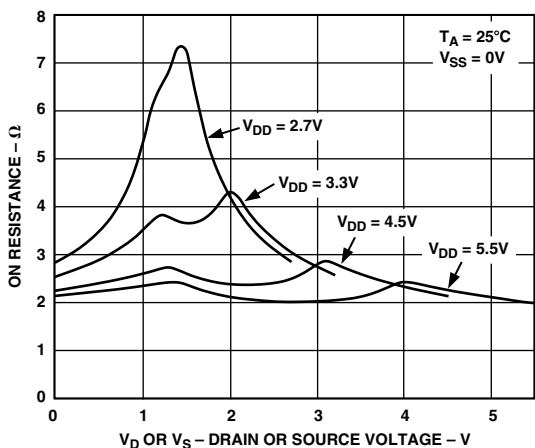
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG708/ADG709 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



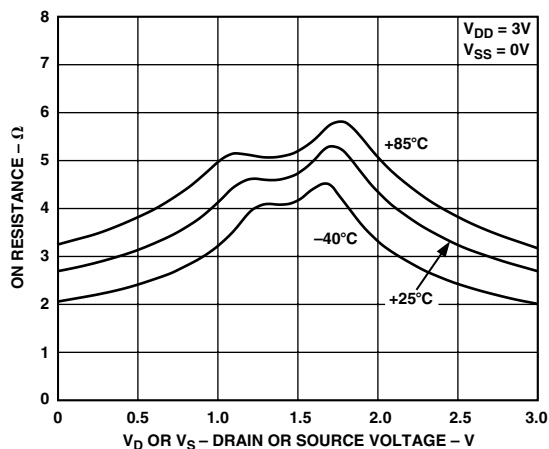
## TERMINOLOGY

$V_{DD}$	Most Positive Power Supply Potential
$V_{SS}$	Most Negative Power Supply in a Dual-Supply Application. In single-supply applications, this should be tied to ground at the device.
GND	Ground (0 V) Reference
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
Ax	Logic Control Input
EN	Active High Enable
$R_{ON}$	Ohmic Resistance between D and S
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of ON resistance as measured over the specified analog signal range.
$I_S$ (OFF)	Source Leakage Current with the Switch OFF
$I_D$ (OFF)	Drain Leakage Current with the Switch OFF
$I_D, I_S$ (ON)	Channel Leakage Current with the Switch ON
$V_D$ ( $V_S$ )	Analog Voltage on Terminals D and S
$C_S$ (OFF)	OFF Switch Source Capacitance. Measured with reference to ground.
$C_D$ (OFF)	OFF Switch Drain Capacitance. Measured with reference to ground.
$C_D, C_S$ (ON)	ON Switch Capacitance. Measured with reference to ground.
$C_{IN}$	Digital Input Capacitance
$t_{TRANSITION}$	Delay time measured between the 50% and 90% points of the digital inputs and the switch ON condition when switching from one address state to another.
$t_{ON}$ (EN)	Delay time between the 50% and 90% points of the EN digital input and the switch ON condition.
$t_{OFF}$ (EN)	Delay time between the 50% and 90% points of the EN digital input and the switch OFF condition.
$t_{OPEN}$	OFF time measured between the 80% points of both switches when switching from one address state to another.
Off Isolation	A measure of unwanted signal coupling through an OFF switch.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
Charge	A measure of the glitch impulse transferred from injection of the digital input to the analog output during switching.
Bandwidth	The frequency at which the output is attenuated by 3 dBs
On Response	The Frequency Response of the ON Switch
On Loss	The Loss Due to the ON Resistance of the Switch
$V_{INL}$	Maximum Input Voltage for Logic "0"
$V_{INH}$	Minimum Input Voltage for Logic "1"
$I_{INL}$ ( $I_{INH}$ )	Input Current of the Digital Input
$I_{DD}$	Positive Supply Current
$I_{SS}$	Negative Supply Current

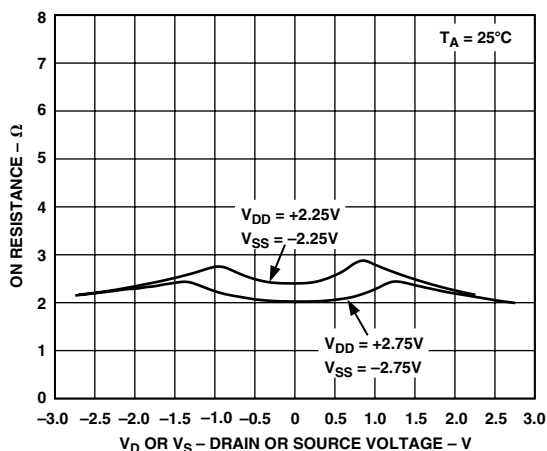
# Typical Performance Characteristics—ADG708/ADG709



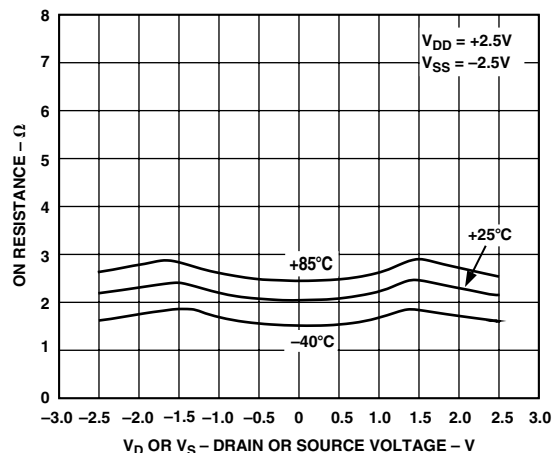
TPC 1. ON Resistance as a Function of  $V_D$  ( $V_S$ ) for Single Supply



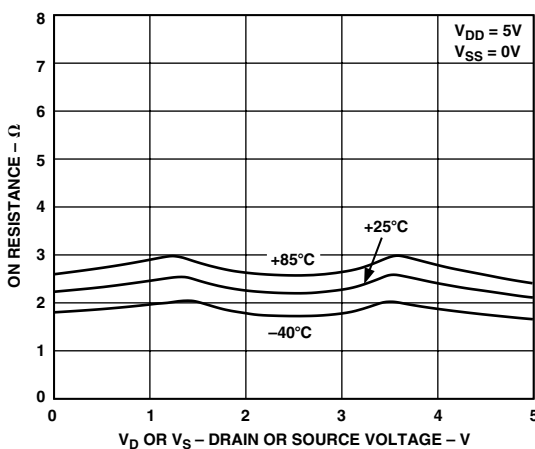
TPC 4. ON Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures, Single Supply



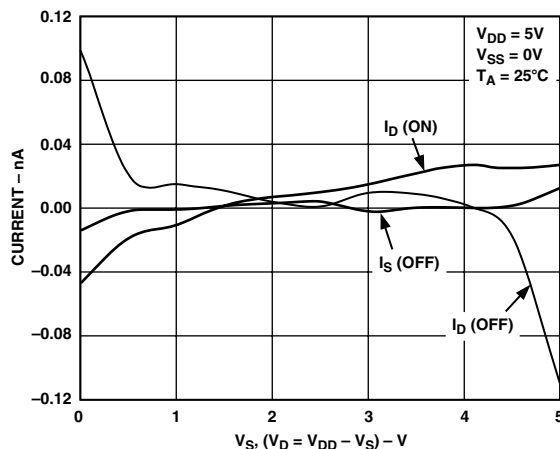
TPC 2. ON Resistance as a Function of  $V_D$  ( $V_S$ ) for Dual Supply



TPC 5. ON Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures, Dual Supply

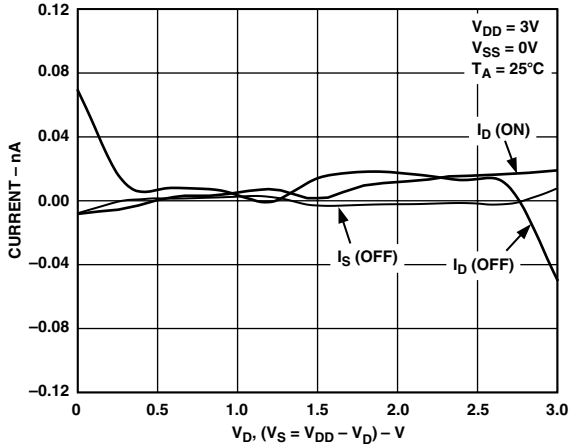


TPC 3. ON Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures, Single Supply

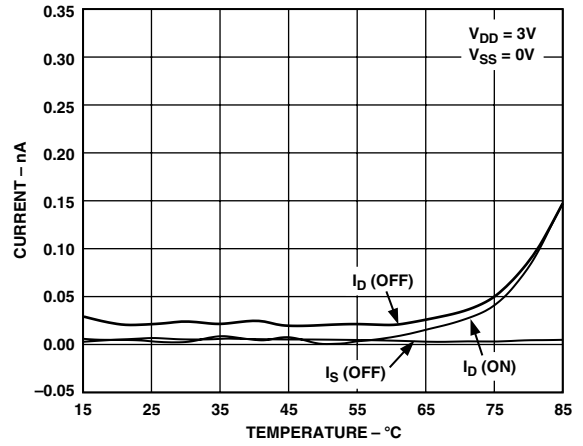


TPC 6. Leakage Currents as a Function of  $V_D$  ( $V_S$ )

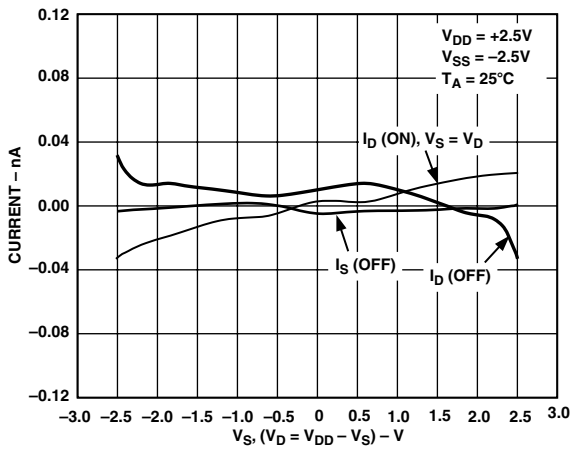
# ADG708/ADG709



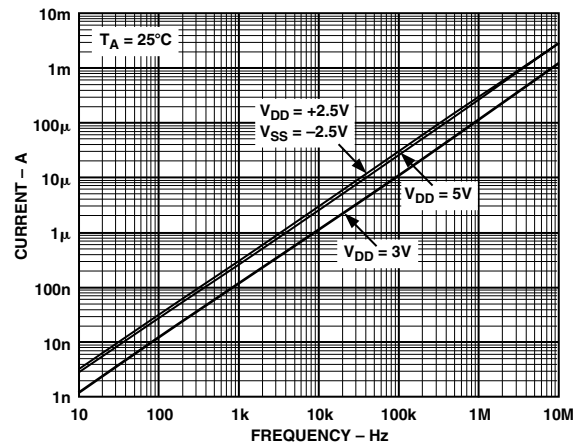
TPC 7. Leakage Currents as a Function of  $V_D$  ( $V_S$ )



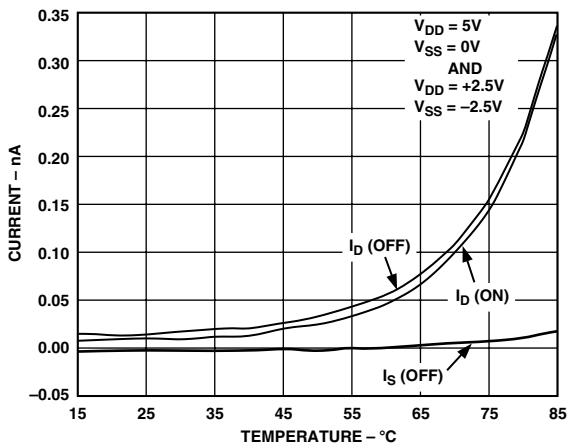
TPC 10. Leakage Currents as a Function of Temperature



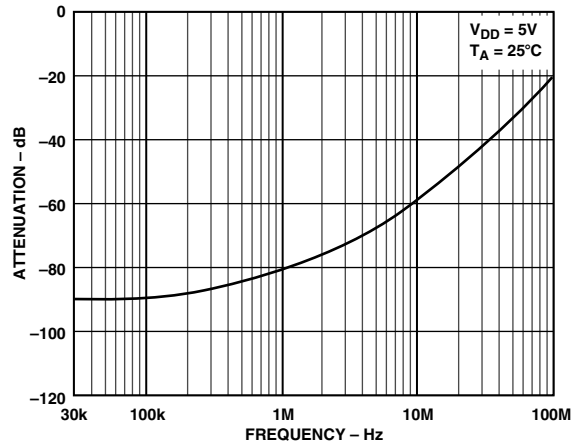
TPC 8. Leakage Currents as a Function of  $V_D$  ( $V_S$ )



TPC 11. Supply Current vs. Input Switching Frequency

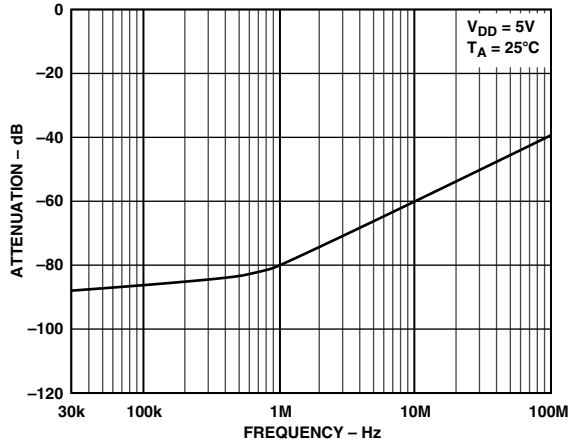


TPC 9. Leakage Currents as a Function of Temperature

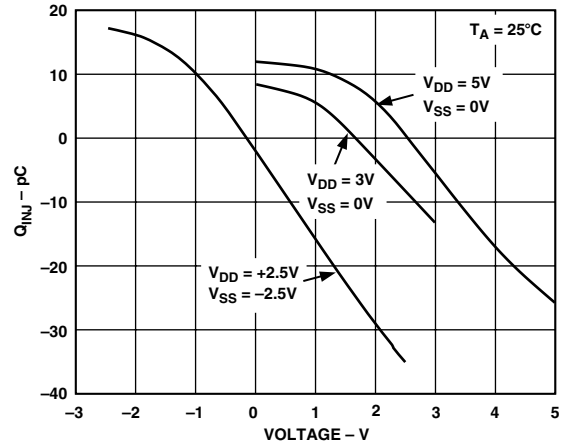


TPC 12. OFF Isolation vs. Frequency

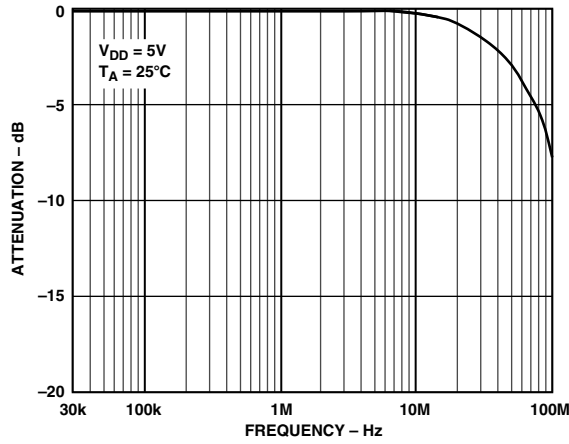




TPC 13. Crosstalk vs. Frequency



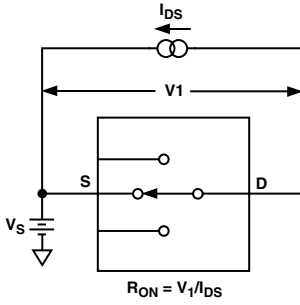
TPC 15. Charge Injection vs. Source Voltage



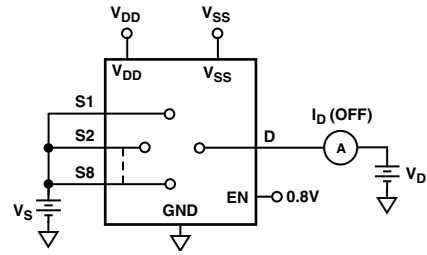
TPC 14. ON Response vs. Frequency

# ADG708/ADG709

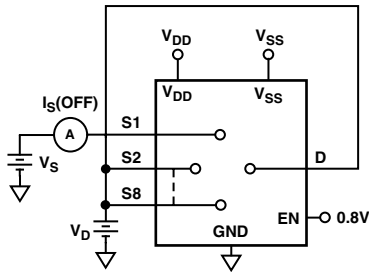
## Test Circuits



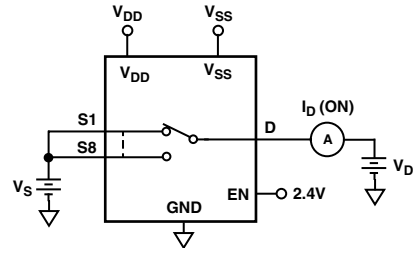
Test Circuit 1. ON Resistance



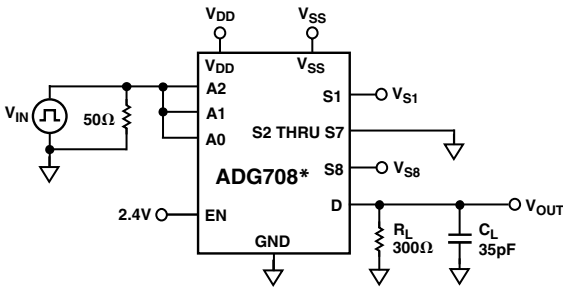
Test Circuit 3.  $I_D$  (OFF)



Test Circuit 2.  $I_S$  (OFF)

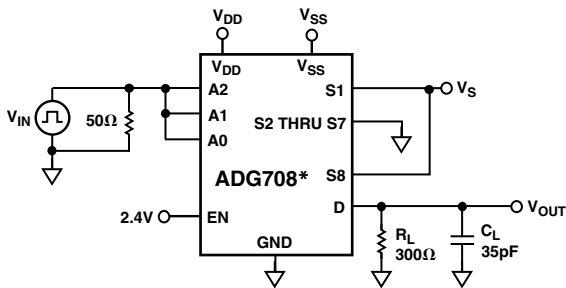
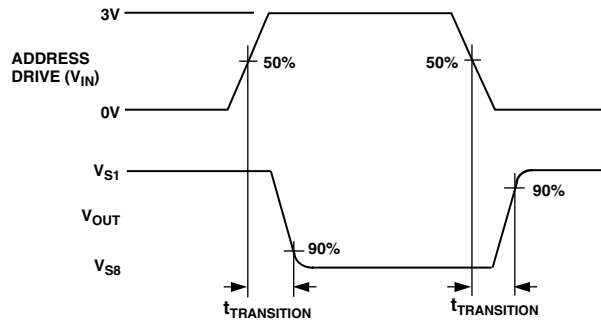


Test Circuit 4.  $I_D$  (ON)



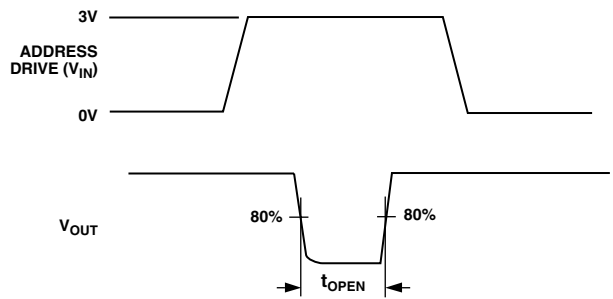
\*SIMILAR CONNECTION FOR ADG709

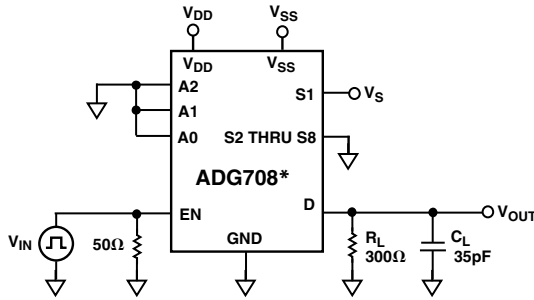
Test Circuit 5. Switching Time of Multiplexer,  $t_{TRANSITION}$



\*SIMILAR CONNECTION FOR ADG709

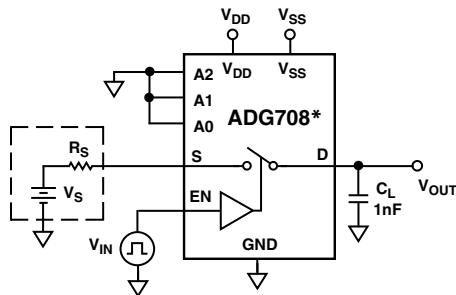
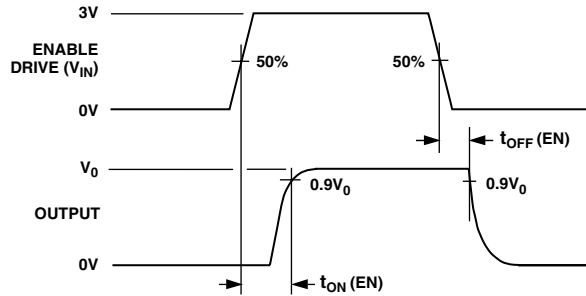
Test Circuit 6. Break-Before-Make Delay,  $t_{OPEN}$





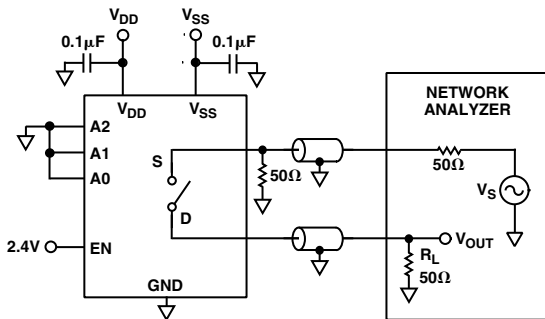
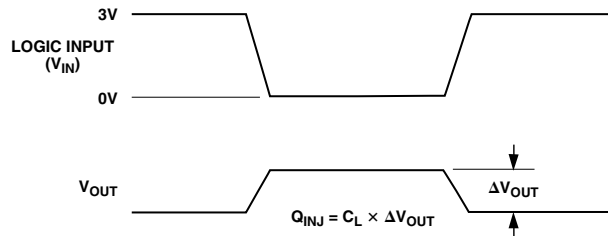
\*SIMILAR CONNECTION FOR ADG709

Test Circuit 7. Enable Delay,  $t_{ON}(EN)$ ,  $t_{OFF}(EN)$



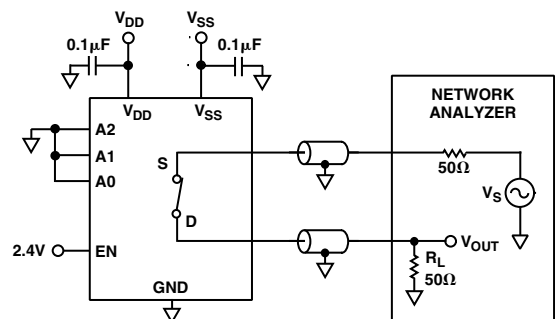
\*SIMILAR CONNECTION FOR ADG709

Test Circuit 8. Charge Injection



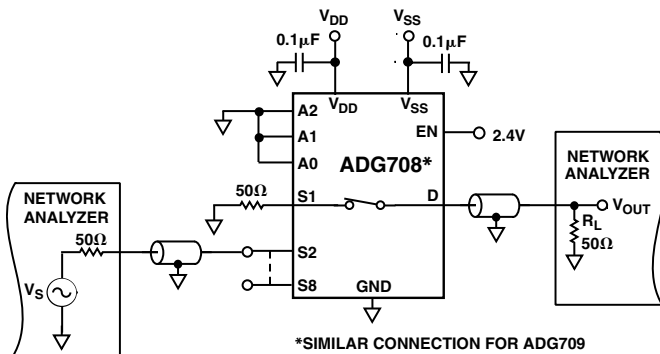
$$\text{OFF ISOLATION} = 20 \text{ LOG } \frac{V_{OUT}}{V_S}$$

Test Circuit 9. OFF Isolation



$$\text{INSERTION LOSS} = 20 \text{ LOG } \frac{V_{OUT \text{ WITH SWITCH}}}{V_{OUT \text{ WITHOUT SWITCH}}}$$

Test Circuit 11. Bandwidth



\*SIMILAR CONNECTION FOR ADG709  
CHANNEL-TO-CHANNEL  
CROSSTALK = 20 LOG  $\frac{V_{OUT}}{V_S}$

Test Circuit 10. Channel-to-Channel Crosstalk

### Power-Supply Sequencing

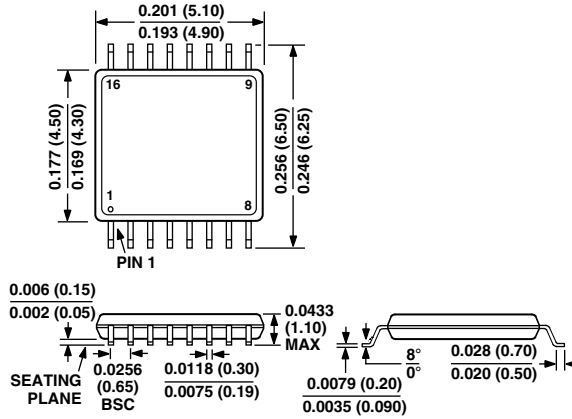
When using CMOS devices, care must be taken to ensure correct power supply sequencing. Incorrect power supply sequencing can result in the device being subjected to stresses beyond the maximum ratings listed in the data sheet. Digital and analog inputs should always be applied after power supplies and ground. For single-supply operation,  $V_{SS}$  should be tied to GND as close to the device as possible.

# ADG708/ADG709

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

### 16-Lead TSSOP (RU-16)



## Revision History

Location	Page
4/02—Data Sheet changed from REV. 0 to REV. A.	
Edits to FEATURES and PRODUCT HIGHLIGHTS	1
Change to SPECIFICATIONS	2-4
Edits to ABSOLUTE MAXIMUM RATINGS Notes	5
Edits to TPCs 2, 5, 6-9, 11, and 15	7-9
Edits to Test Circuits 9 and 10	11
Addition of Test Circuit 11	11

C00041-0-5/02(A)

PRINTED IN U.S.A.