

FULLY DECODED 4096 STATIC CMOS RAM

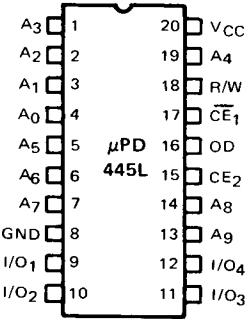
DESCRIPTION The μPD445L is a very low power 4,096 bit (1024 words by 4 bits) static RAM fabricated with NEC's complementary MOS (CMOS) process. It has two chip enable inputs ($\overline{CE}_1$, CE_2). Minimum standby current is drawn when $\overline{CE}_1$ is at a high level, while inhibiting all address and control line transitions or, unconditionally when CE_2 is at a low level. This device ideally meets the low power requirements of battery operated systems and battery back-up systems for non-volatility of data.

The μPD445L uses fully static circuitry requiring no clocking. Output data is read out non-destructively by placing a high on the R/W pin and has the same polarity as input data. All inputs and outputs are directly TTL compatible. The device has common input/output data busses and an OD (Output Disable) pin for use in common I/O bus systems.

The μPD445L is guaranteed to retain data with the power supply voltage as low as 2.0 volts.

- FEATURES**
- Single +5V Power Supply
 - Ideal for Battery Operation
 - Low Standby Power for Data Retention
 - Simple Memory Expansion — Chip Enable Inputs
 - Access Time — 650 ns Max. (μPD445L)
450 ns Max. (μPD445L-1)
 - Directly TTL Compatible — All Inputs and Outputs
 - Common Data Input and Output
 - Static CMOS — No Clock or Refreshing Required
 - 20 Pin Dual-In-Line Plastic Package

PIN CONFIGURATION

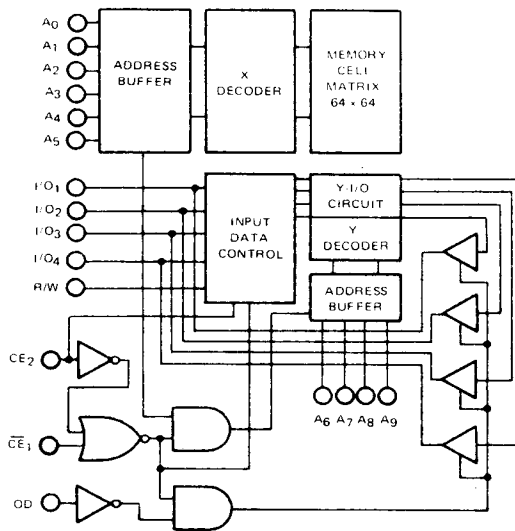


PIN NAMES

A ₀ -A ₉	Address Input
OD	Output Disable
R/W	Read/Write
$\overline{CE}_1$	Chip Enable 1
CE ₂	Chip Enable 2
I/O ₁ -I/O ₄	Data Input/Output
V _{CC}	Power Supply
GND	Ground

OPERATION MODES

$\overline{CE}_1$	CE ₂	OD	Chip	Output Mode
0	1	0	Selected	Data Out
0	1	1		High Impedance
Others			Non-Selected	



Operating Temperature 0°C to +70°C
 Storage Temperature -40°C to +125°C
 All Output Voltages -0.3 to $V_{CC} + 0.3$ Volts
 All Input Voltages -0.3 to $V_{CC} + 0.3$ Volts
 Supply Voltage V_{CC} -0.3 to +7 Volts

ABSOLUTE MAXIMUM RATINGS*

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* $T_a = 25^\circ\text{C}$

$T_a = 0^\circ\text{C}$ to $+70^\circ\text{C}$; +5V ± 10%

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input High Voltage	V_{IH}	+2.2		V_{CC}	V	
Input Low Voltage	V_{IL}	-0.3		+ 0.65	V	
Output High Voltage	V_{OH1}	+2.4			V	$I_{OH} = -1.0 \text{ mA}$
	V_{OH2}	+3.5			V	$I_{OH} = -100 \mu\text{A}$
Output Low Voltage	V_{OL}			+ 0.4	V	$I_{OL} = +2.0 \text{ mA}$
Input Leakage Current High	I_{LIH}			+ 1.0	μA	$V_I = V_{CC}$
Input Leakage Current Low	I_{LIL}			- 1.0	μA	$V_I = 0\text{V}$
Output Leakage Current High	I_{LOH}			+ 1.0	μA	$V_O = V_{CC}$ $CE_1 = 2.2\text{V}$
Output Leakage Current Low	I_{LOL}			1.0	μA	$V_O = 0\text{V}$ $CE_1 = 2.2\text{V}$
Supply Current	I_{CC1}		12	25	mA	Outputs Open $V_I = V_{CC}$ except $CE_1 < 0.65\text{V}$
Supply Current	I_{CC2}		16	30	mA	Outputs Open $V_I = 2.2\text{V}$ except $CE_1 < 0.65\text{V}$

DC CHARACTERISTICS

CAPACITANCE $T_a = 25^\circ\text{C}; f = 1\text{ MHz}$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C_I		5	8	pF	$V_I = 0\text{V}$
Output Capacitance	C_O		8	12	pF	$V_O = 0\text{V}$

AC CHARACTERISTICS

READ CYCLE

$T_a = 0^\circ\text{C to } +70^\circ\text{C}; V_{CC} = +5\text{V} \pm 10\%$

PARAMETER	SYMBOL	LIMITS				UNIT	TEST CONDITIONS
		445L		445L-1			
		MIN	MAX	MIN	MAX		
Read Cycle Time	t _{RC}	650		450		ns	Input Voltage Levels V = +0.65 to +2.2V
Access Time	t _A		650		450	ns	
Chip Enable (CE ₁) to Output	t _{CO1}		600		400	ns	
Chip Enable (CE ₂) to Output	t _{CO2}		700		500	ns	Input Rise Time 20 ns
Output Enable to Output	t _{OD}		350		250	ns	Input Fall Time 20 ns
Output Disable (OD) to Floating	t _{DF}	0	150	0	130	ns	Timing Measurement Reference Level = +1.5V
Data Output Hold Time	t _{OH1}	0		0		ns	Output Load
Chip Disable to Floating	t _{OH2}	0		0		ns	1 TTL + 100 pF
Address Rise and Fall Time	t _r t _f		300		300	ns	For Address change during Chip Enabled

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WRITE CYCLE

$T_a = 0^\circ\text{C to } +70^\circ\text{C}; V_{CC} = +5\text{V} \pm 10\%$

PARAMETER	SYMBOL	LIMITS				UNIT	TEST CONDITIONS
		445L		445L-1			
		MIN	MAX	MIN	MAX		
Write Cycle Time	tWC	650		450		ns	Input Voltage Levels V _I = +0.65 to +2.2V
Address Setup Time	tAW	150		130		ns	
Chip Enable (CE ₁) to Write End	tCW1	550		350		ns	
Chip Enable (CE ₂) to Write End	tCW2	550		350		ns	Input Rise Time 20 ns
Data Setup Time	tDW	400		250		ns	Input Fall Time 20 ns
Data Hold Time	tDH	100		50		ns	Timing Measurement Reference Level = +1.5V
Write Pulse Width	tWP	400		250		ns	
Address Hold Time	tWR	50		50		ns	
Output Disable Setup Time	tDS	150		130		ns	For Address change during Chip Enabled
Address Rise and Fall Time	t _r t _f		300		300	ns	

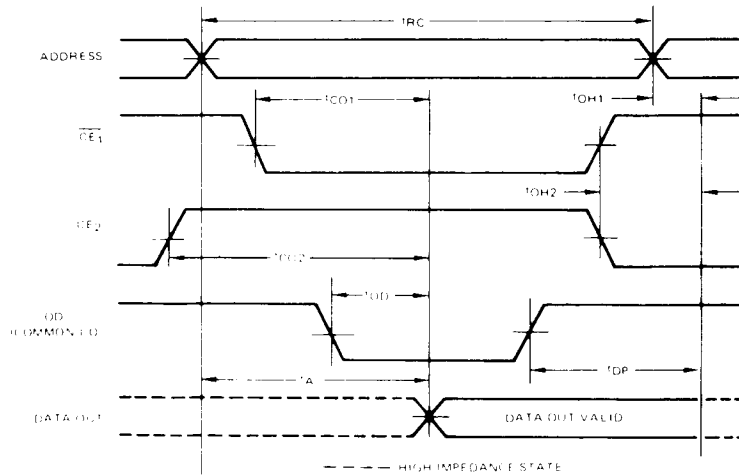
LOW V_{CC} DATA RETENTION

$T_a = 0^\circ\text{C to } +70^\circ\text{C}$

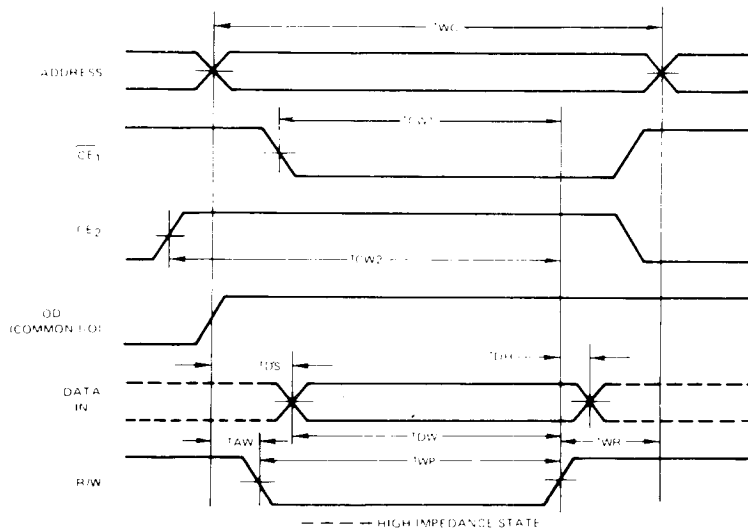
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
V_{CC} for Data Retention	V_{CCDR}	+2.0			V	$CE_2 \leq +0.2\text{V}$
Data Retention Current	I_{CCDR}			40	μA	$V_{CCDR} = +2.0\text{V}$ $CE_2 \leq +0.2\text{V}$
Chip Deselect Setup Time	t_{CDR}	0			ns	
Chip Deselect Hold Time	t_{RH}	$t_{RC} \text{ (1)}$			ns	

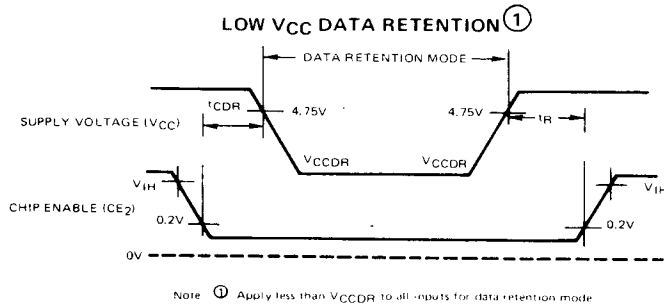
Note: (1) t_{RC} = Read Cycle Time

READ CYCLE

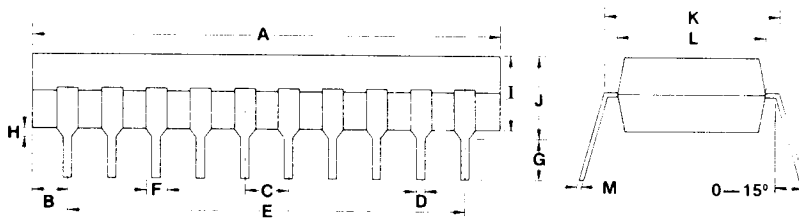


WRITE CYCLE





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PACKAGE OUTLINE
μPD445LC

(PLASTIC)

ITEM	MILLIMETERS	INCHES
A	27.00	1.07
B	2.07	0.08
C	2.54	0.10
D	0.50	0.02
E	22.86	0.90
F	1.20	0.05
G	2.54 MIN	0.10 MIN
H	0.50 MIN	0.02 MIN
I	4.58 MAX	0.18
J	5.08 MAX	0.20
K	10.16	0.40
L	8.60	0.39
M	+0.10 -0.05	+0.004 -0.002