

### SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

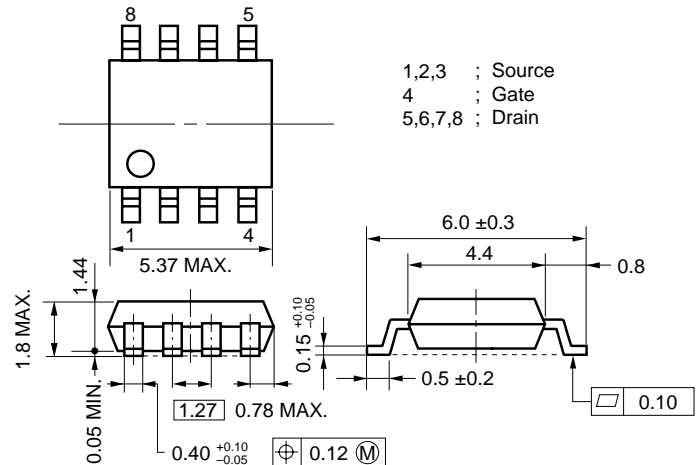
#### DESCRIPTION

The μPA1721 is N-Channel MOS Field Effect Transistor designed for DC/DC converters and power management applications of notebook computers.

#### FEATURES

- Low on-resistance  
 $R_{DS(on)1} = 10.5 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 5.0 \text{ A)}$   
 $R_{DS(on)2} = 14.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 5.0 \text{ A)}$   
 $R_{DS(on)3} = 17.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.0 \text{ V, } I_D = 5.0 \text{ A)}$
- Low  $C_{iss}$ :  $C_{iss} = 2200 \text{ pF TYP.}$
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

#### PACKAGE DRAWING (Unit : mm)



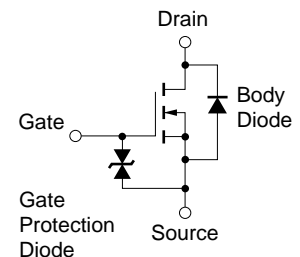
#### ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA1721G	Power SOP8

#### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C, All terminals are connected.)

Drain to Source Voltage (V <sub>GS</sub> = 0 V)	V <sub>DSS</sub>	30	V
Gate to Source Voltage (V <sub>DS</sub> = 0 V)	V <sub>GSS</sub>	±20	V
Drain Current (DC)	I <sub>D(DC)</sub>	±10	A
Drain Current (pulse) <sup>Note1</sup>	I <sub>D(pulse)</sub>	±40	A
Total Power Dissipation (T <sub>A</sub> = 25°C) <sup>Note2</sup>	P <sub>T</sub>	2.0	W
Channel Temperature	T <sub>ch</sub>	150	°C
Storage Temperature	T <sub>stg</sub>	-55 to +150	°C

#### EQUIVALENT CIRCUIT



- Notes 1.**  $PW \leq 10 \mu s$ , Duty Cycle  $\leq 1 \%$   
**2.** Mounted on ceramic substrate of  $1200 \text{ mm}^2 \times 2.2 \text{ mm}$

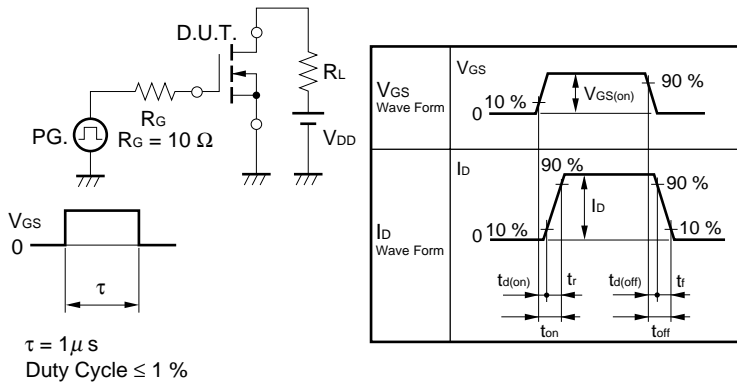
**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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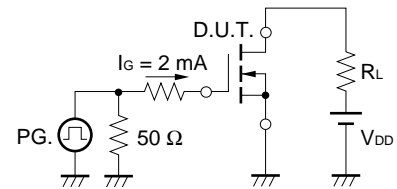
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, All terminals are connected.)**

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R <sub>DS(on)1</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 5.0 A		8.0	10.5	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 5.0 A		10.0	14.0	mΩ
	R <sub>DS(on)3</sub>	V <sub>GS</sub> = 4.0 V, I <sub>D</sub> = 5.0 A		12.0	17.0	mΩ
Gate to Source Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 5.0 A	7.0	14.0		S
Drain Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V			10	μA
Gate to Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±10	μA
Input Capacitance	C <sub>iSS</sub>	V <sub>DS</sub> = 10 V		2200		pF
Output Capacitance	C <sub>oSS</sub>	V <sub>GS</sub> = 0 V		710		pF
Reverse Transfer Capacitance	C <sub>rSS</sub>	f = 1 MHz		270		pF
Turn-on Delay Time	t <sub>d(on)</sub>	I <sub>D</sub> = 5.0 A		30		ns
Rise Time	t <sub>r</sub>	V <sub>GS(on)</sub> = 10 V		90		ns
Turn-off Delay Time	t <sub>d(off)</sub>	V <sub>DD</sub> = 15 V		90		ns
Fall Time	t <sub>f</sub>	R <sub>G</sub> = 10 Ω		50		ns
Total Gate Charge	Q <sub>G</sub>	I <sub>D</sub> = 10 A		39		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>DD</sub> = 24 V		6.3		nC
Gate to Drain Charge	Q <sub>GD</sub>	V <sub>GS</sub> = 10 V		10.0		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	I <sub>F</sub> = 10 A, V <sub>GS</sub> = 0 V		0.8		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 10 A, V <sub>GS</sub> = 0 V		40		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100 A/μs		50		nC

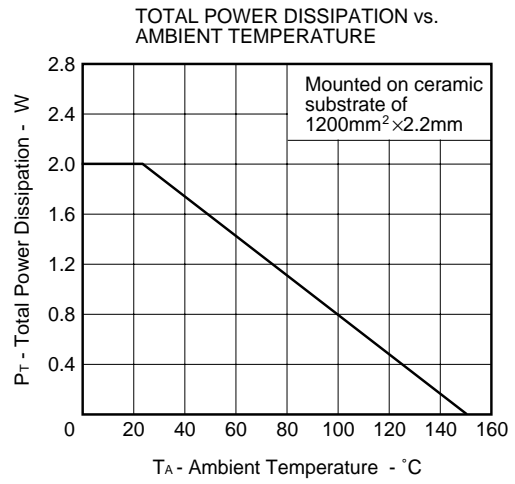
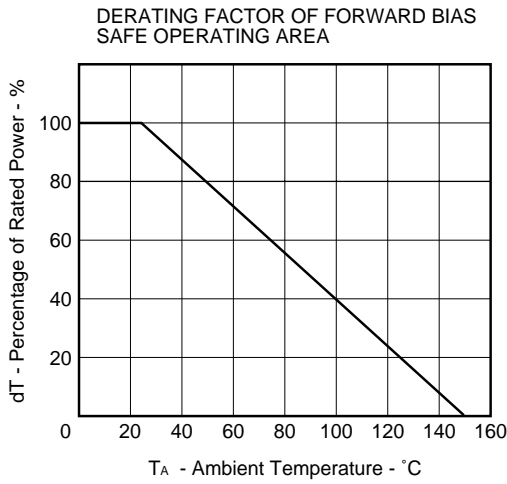
**TEST CIRCUIT 1 SWITCHING TIME**



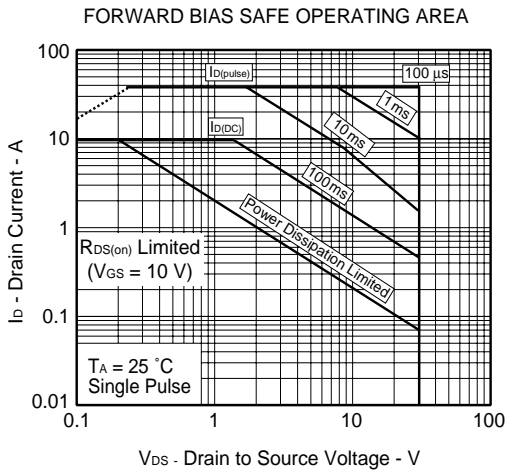
**TEST CIRCUIT 2 GATE CHARGE**



TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C)



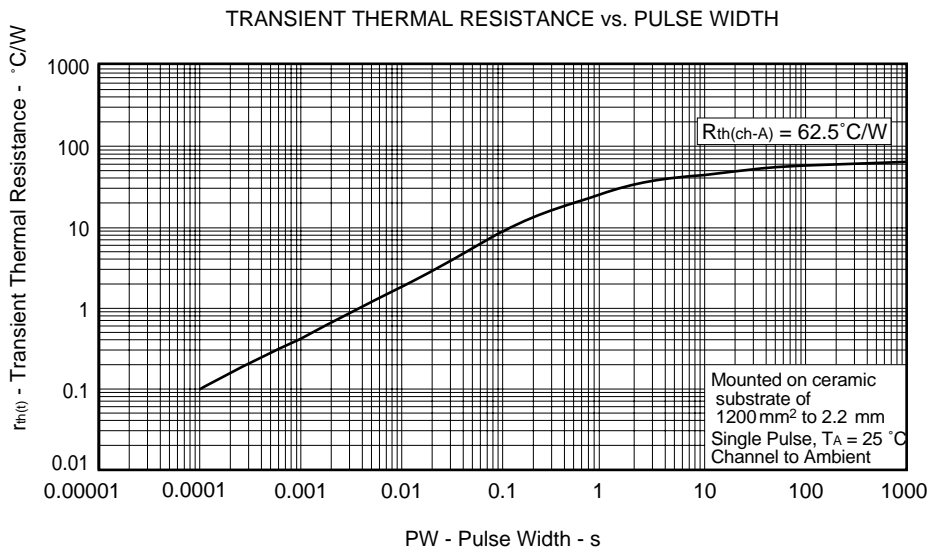
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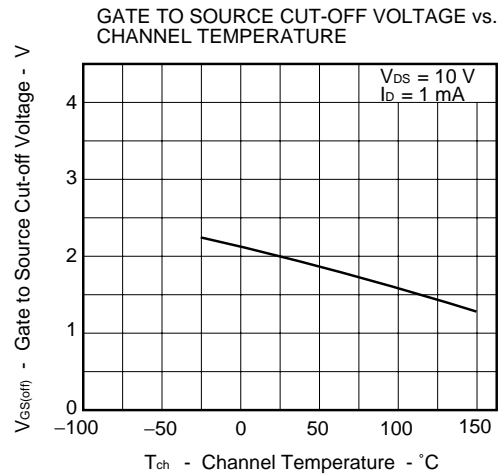
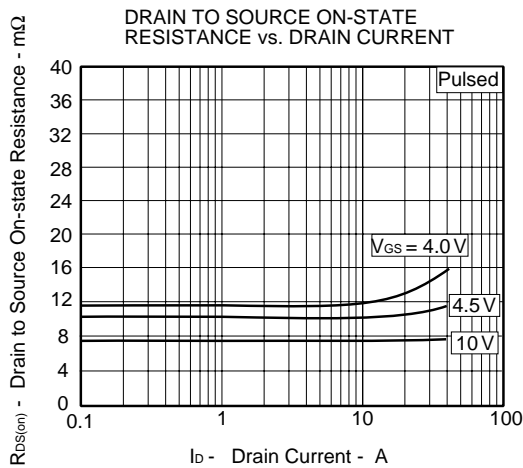
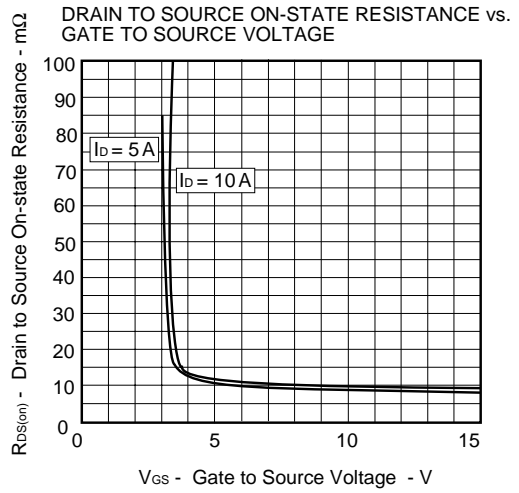
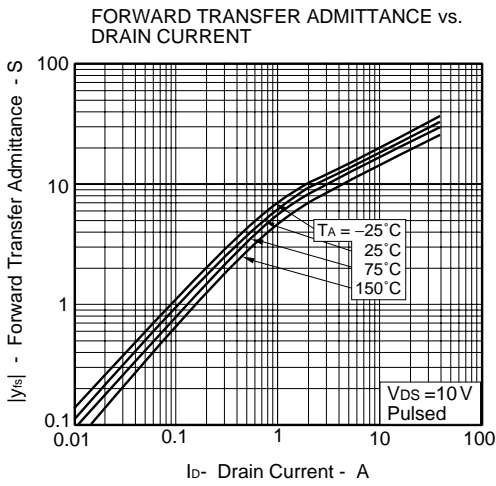
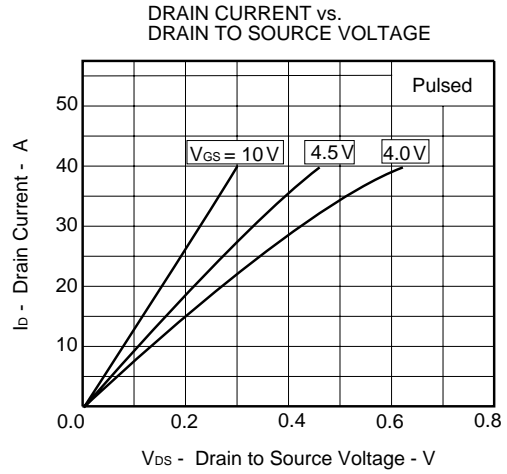
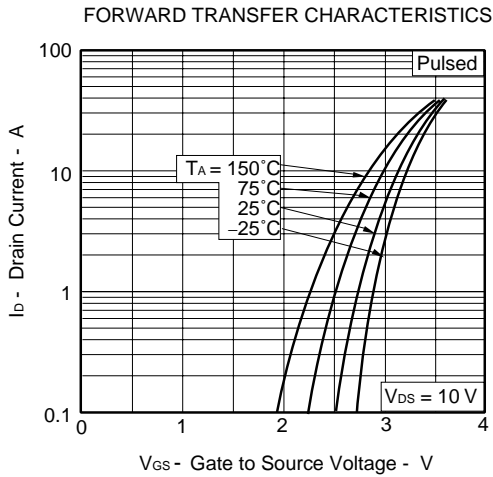


Note

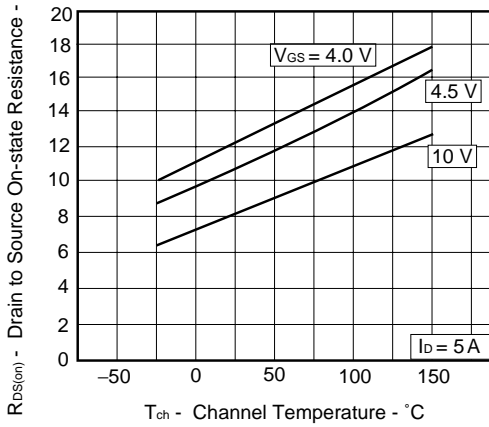
Mounted on ceramic substrate of 1200 mm<sup>2</sup> × 2.2 mm

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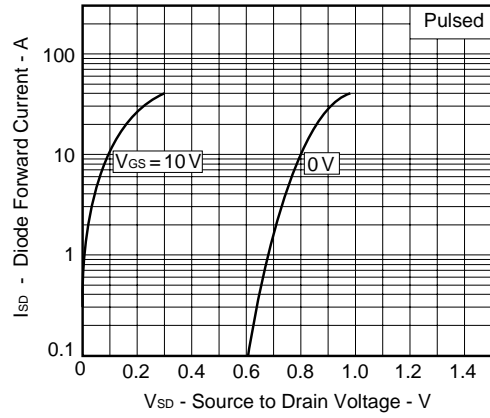




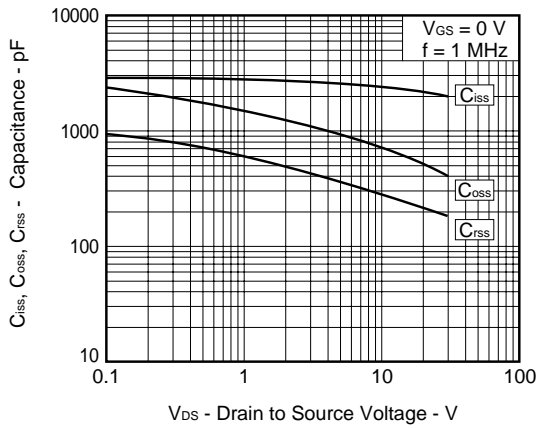
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



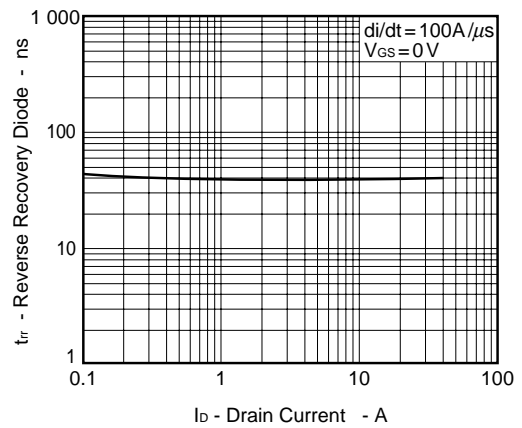
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



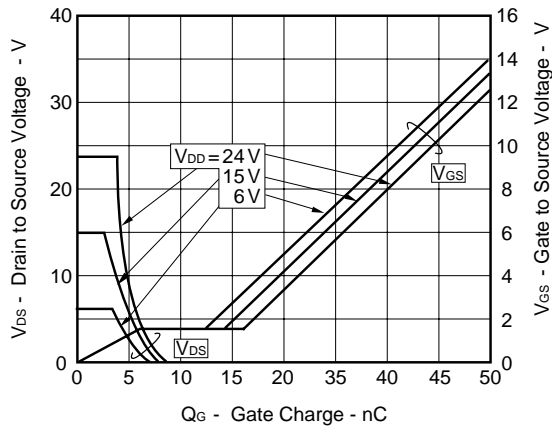
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



REVERSE RECOVERY TIME vs. DRAIN CURRENT



DYNAMIC INPUT/OUTPUT CHARACTERISTICS



[MEMO]

[MEMO]

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