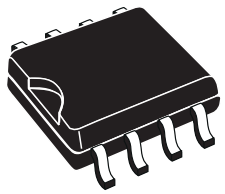
STS11NF3LL

N-CHANNEL 30V - 0.008Ω - 11A SO-8
LOW GATE CHARGE STripFET™ II POWER MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STS11NF3LL	30 V	< 0.011 Ω	11 A

- TYPICAL $R_{DS}(on)$ = 0.011Ω @ 4.5V
- OPTIMAL $R_{DS(on)}$ Q_g TRADE-OFF @4.5V
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED

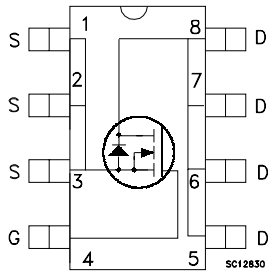


SO-8

DESCRIPTION

This application specific Power MOSFET is the third genaration of STMicroelectronics unique " Single Feature Size" strip-based process. The resulting transistor shows the best trade-off between on-resistance and gate charge. When used as high and low side in buck regulators, it gives the best performance in terms of both conduction and switching losses. This is extremely important for motherboards where fast switching and high efficiency are of paramount importance.

INTERNAL SCHEMATIC DIAGRAM



APPLICATIONS

- SPECIFICALLY DESIGNED AND OPTIMISED FOR HIGH EFFICIENCY CPU CORE DC/DC CONVERTERS FOR MOBILE PCs

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	30	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	30	V
V_{GS}	Gate- source Voltage	± 16	V
I_D	Drain Current (continuos) at T_C = 25°C (*) Drain Current (continuos) at T_C = 100°C	11 7	A A
I_{DM} (●)	Drain Current (pulsed)	44	A
P_{TOT}	Total Dissipation at T_C = 25°C	2.5	W

(●) Pulse width limited by safe operating area (*)Value limited by wires bonding

THERMAL DATA

Rthj-amb	Thermal Resistance Junction-ambient Max (#)	50	°C/W
T_j	Max. Operating Junction Temperature	150	°C
T_{stg}	Storage Temperature	–65 to 150	°C

(#) When Mounted on a 1inch^2 pad

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	30			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating			1	µA
		V_{DS} = Max Rating, T_C = 125 °C			10	µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 16V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	1			V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10 V, I_D = 5.5 A		0.008	0.011	Ω
		V_{GS} = 4.5 V, I_D = 5.5 A		0.011	0.013	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$, I_D = 5.5 A		15		S
C_{iss}	Input Capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0		1700		pF
C_{oss}	Output Capacitance			505		pF
C_{rss}	Reverse Transfer Capacitance			115		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	V_{DD} = 15 V, I_D = 5.5 A		20		ns
t_r	Rise Time	R_G = 4.7Ω V_{GS} = 4.5 V (Resistive Load, see Fig. 3)		70		ns
Q_g	Total Gate Charge	V_{DD} = 15 V, I_D = 11 A,		21	28	nC
Q_{gs}	Gate-Source Charge	V_{GS} = 4.5 V		9.5		nC
Q_{gd}	Gate-Drain Charge			10		nC

SWITCHING OFF

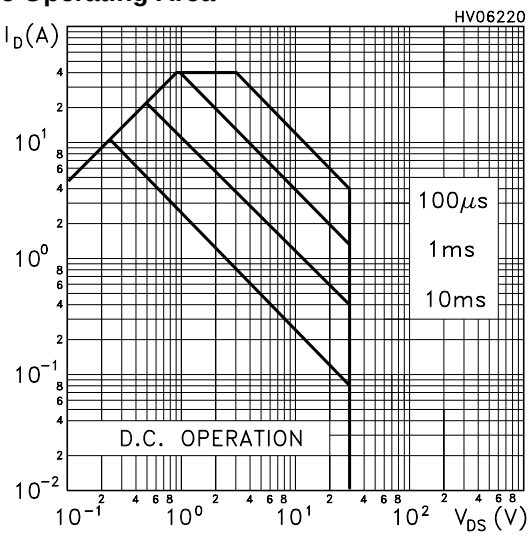
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off-Delay Time	V_{DD} = 15 V, I_D = 5.5 A,		40		ns
t_f	Fall Time	R_G = 4.7Ω, V_{GS} = 4.5 V (Resistive Load see, Fig. 3)		20		ns

SOURCE DRAIN DIODE

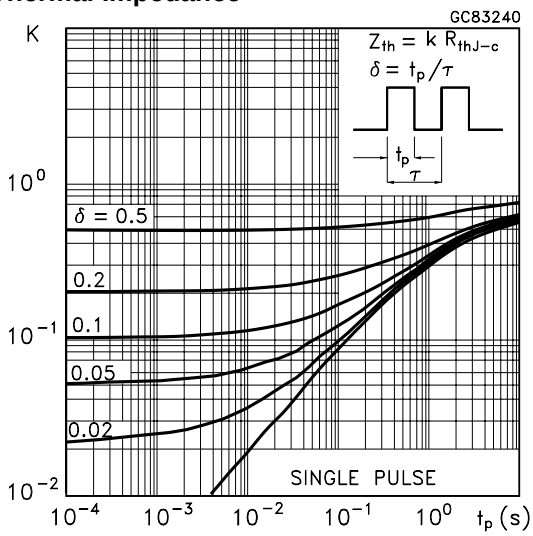
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				11	A
I_{SDM} (1)	Source-drain Current (pulsed)				44	A
V_{SD} (2)	Forward On Voltage	I_{SD} = 11 A, V_{GS} = 0			1.2	V
t_{rr}	Reverse Recovery Time	I_{SD} = 11 A, di/dt = 100A/µs,		45		ns
Q_{rr}	Reverse Recovery	V_{DD} = 20 V, T_j = 150°C		52		nC
I_{RRM}	ChargeReverse Recovery Current	(see test circuit, Figure 5)		2.3		A

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

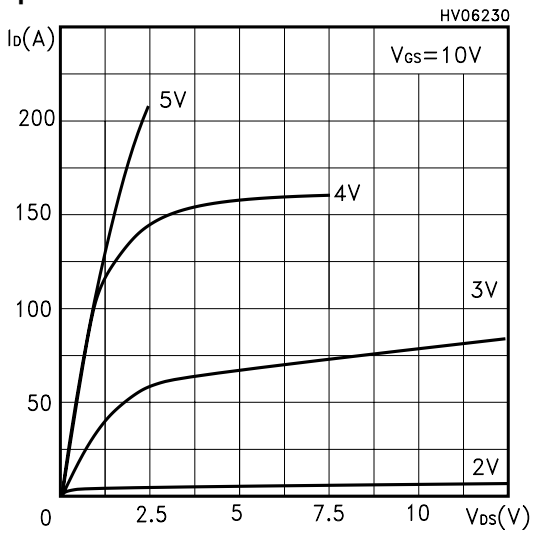
Safe Operating Area



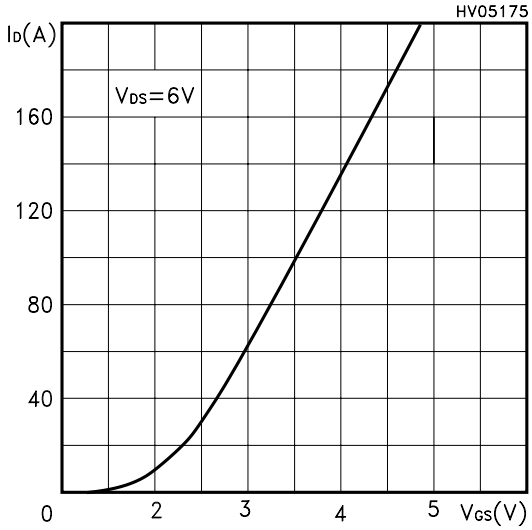
Thermal Impedance



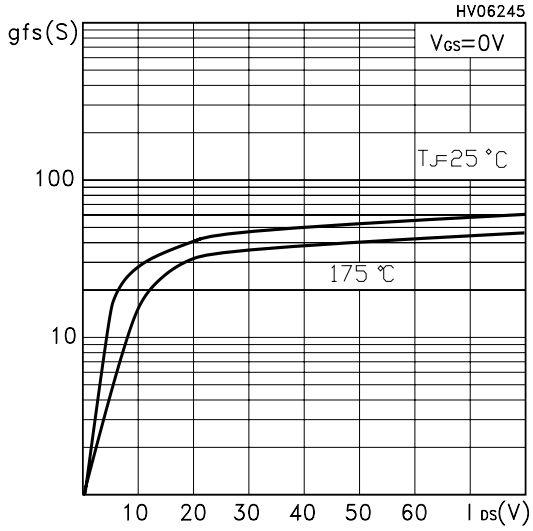
Output Characteristics



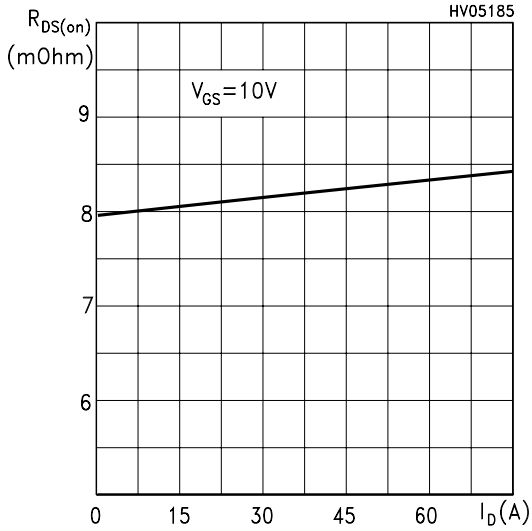
Transfer Characteristics



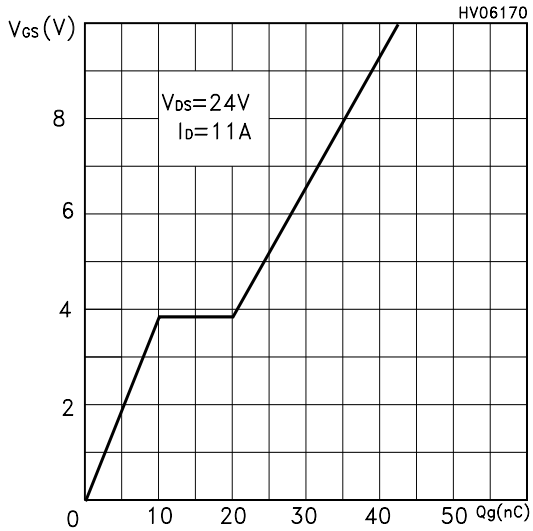
Transconductance



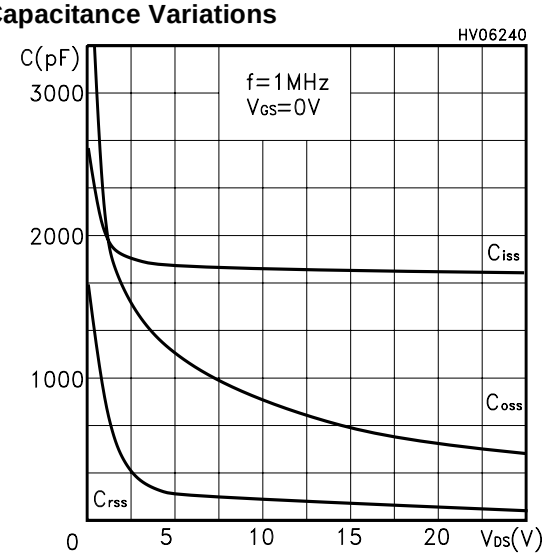
Static Drain-source On Resistance



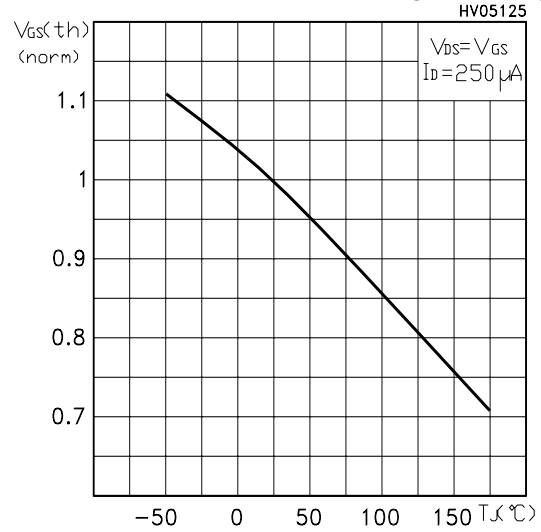
Gate Charge vs Gate-source Voltage



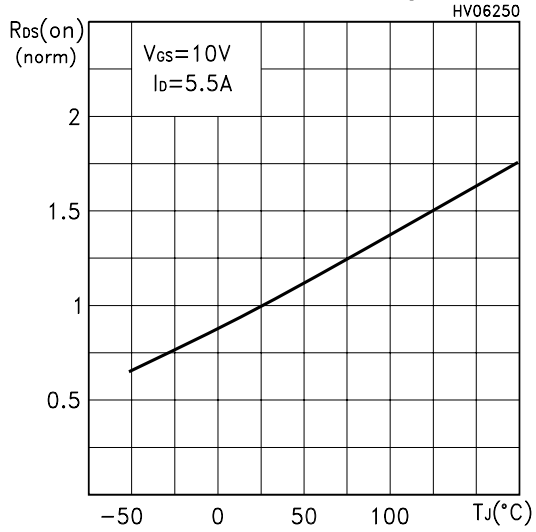
Capacitance Variations



Normalized Gate Thereshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

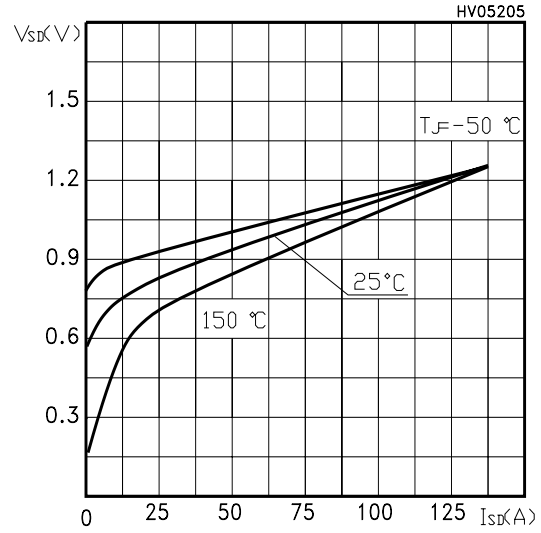


Fig. 1: Unclamped Inductive Load Test Circuit

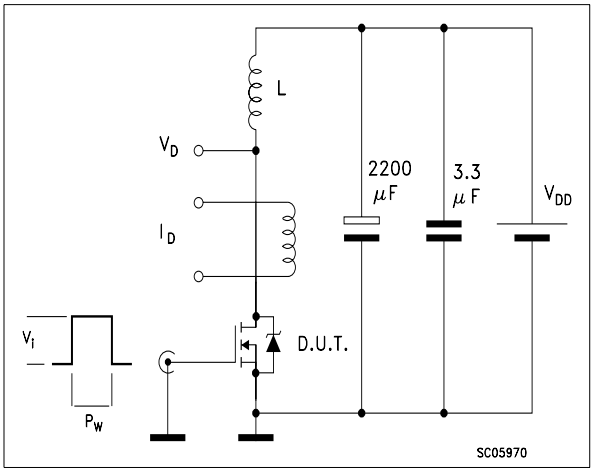


Fig. 2: Unclamped Inductive Waveform

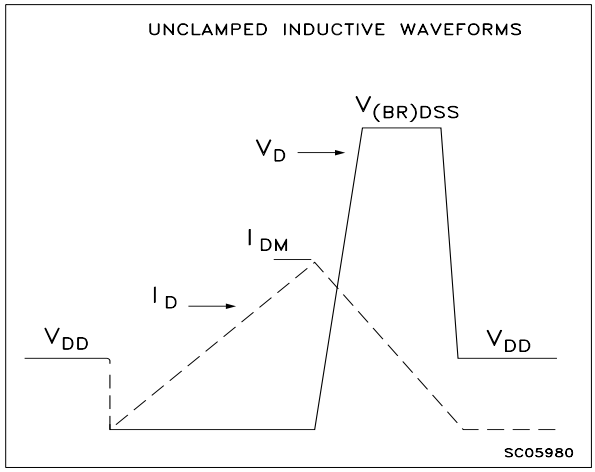


Fig. 3: Switching Times Test Circuit For Resistive Load

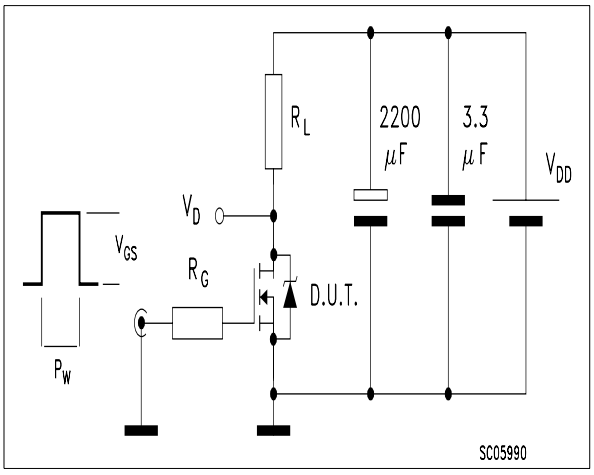


Fig. 4: Gate Charge test Circuit

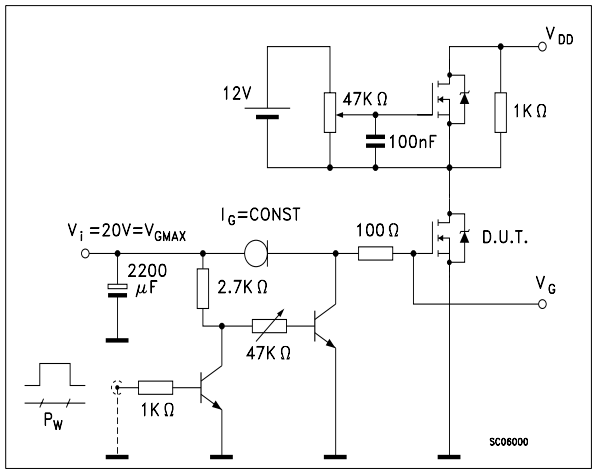
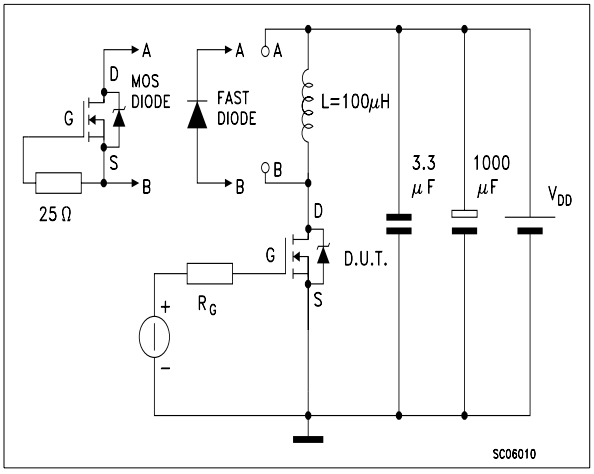
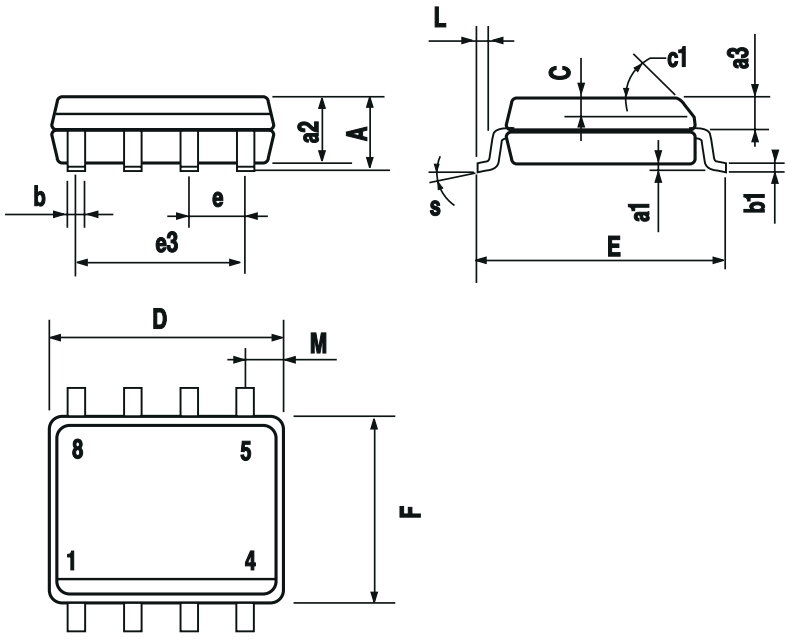


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



SO-8 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



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