



# STS11NF3LL

## N-CHANNEL 30V - 0.008Ω - 11A SO-8 LOW GATE CHARGE STripFET™ II POWER MOSFET

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STS11NF3LL	30 V	< 0.011 Ω	11 A

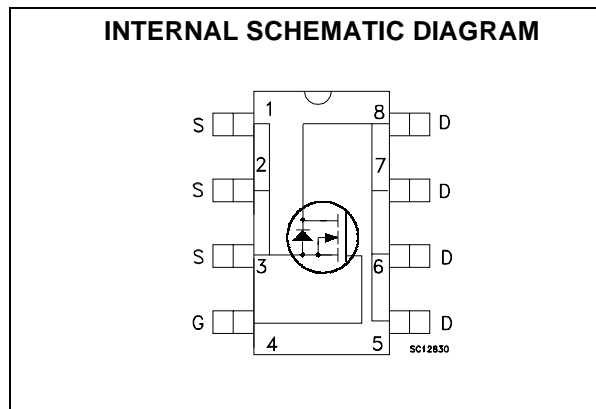
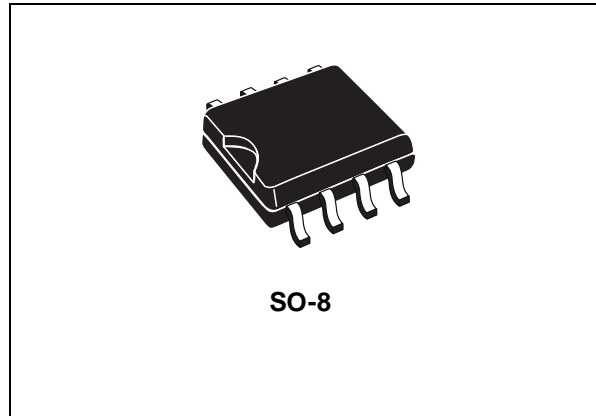
- TYPICAL R<sub>DS(on)</sub> = 0.011Ω @ 4.5V
- OPTIMAL R<sub>DS(on)</sub> Q<sub>g</sub> TRADE-OFF @4.5V
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED

### DESCRIPTION

This application specific Power MOSFET is the third generation of STMicroelectronics unique "Single Feature Size" strip-based process. The resulting transistor shows the best trade-off between on-resistance and gate charge. When used as high and low side in buck regulators, it gives the best performance in terms of both conduction and switching losses. This is extremely important for motherboards where fast switching and high efficiency are of paramount importance.

### APPLICATIONS

- SPECIFICALLY DESIGNED AND OPTIMISED FOR HIGH EFFICIENCY CPU CORE DC/DC CONVERTERS FOR MOBILE PCs



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	30	V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	30	V
V <sub>GS</sub>	Gate- source Voltage	± 16	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C (*)	11	A
	Drain Current (continuous) at T <sub>C</sub> = 100°C	7	A
I <sub>DM</sub> (●)	Drain Current (pulsed)	44	A
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C	2.5	W

(●) Pulse width limited by safe operating area

(\*)Value limited by wires bonding

## STS11NF3LL

### THERMAL DATA

Rthj-amb	Thermal Resistance Junction-ambient Max (#)	50	°C/W
T <sub>j</sub>	Max. Operating Junction Temperature	150	°C
T <sub>stg</sub>	Storage Temperature	-65 to 150	°C

(#) When Mounted on a 1inch<sup>2</sup> pad

### ELECTRICAL CHARACTERISTICS (T<sub>CASE</sub> = 25 °C UNLESS OTHERWISE SPECIFIED) OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating, T <sub>C</sub> = 125 °C			1 10	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 16V			±100	nA

### ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	1			V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 5.5 A V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 5.5 A		0.008 0.011	0.011 0.013	Ω Ω

### DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (1)	Forward Transconductance	V <sub>DS</sub> > I <sub>D(on)</sub> × R <sub>DS(on)max</sub> , I <sub>D</sub> = 5.5 A		15		S
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, f = 1 MHz, V <sub>GS</sub> = 0		1700		pF
C <sub>oss</sub>	Output Capacitance			505		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			115		pF

**ELECTRICAL CHARACTERISTICS (CONTINUED)**

**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 15\text{ V}, I_D = 5.5\text{ A}$		20		ns
$t_r$	Rise Time	$R_G = 4.7\Omega, V_{GS} = 4.5\text{ V}$ (Resistive Load, see Fig. 3)		70		ns
$Q_g$	Total Gate Charge	$V_{DD} = 15\text{ V}, I_D = 11\text{ A},$		21	28	nC
$Q_{gs}$	Gate-Source Charge	$V_{GS} = 4.5\text{ V}$		9.5		nC
$Q_{gd}$	Gate-Drain Charge			10		nC

**SWITCHING OFF**

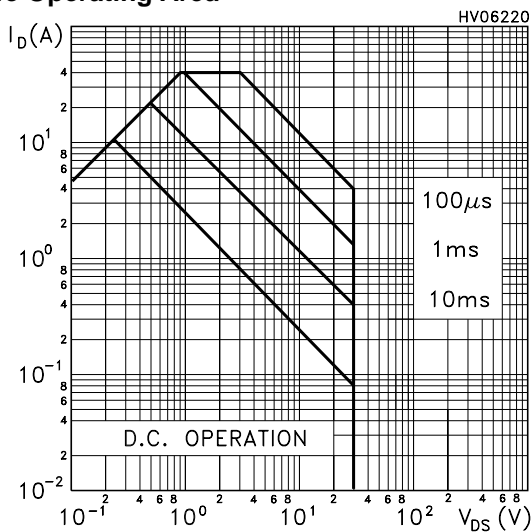
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off-Delay Time	$V_{DD} = 15\text{ V}, I_D = 5.5\text{ A},$		40		ns
$t_f$	Fall Time	$R_G = 4.7\Omega, V_{GS} = 4.5\text{ V}$ (Resistive Load see, Fig. 3)		20		ns

**SOURCE DRAIN DIODE**

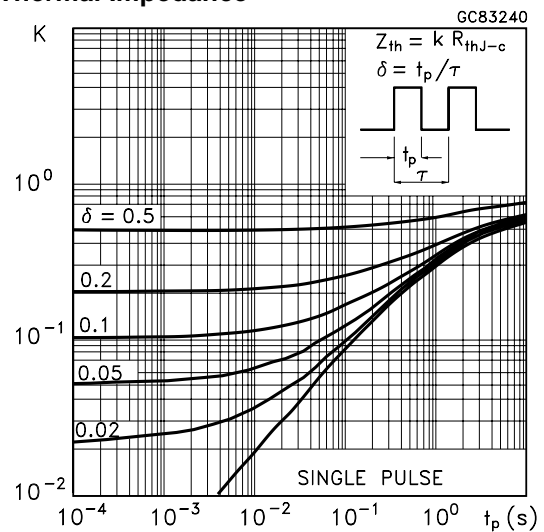
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				11	A
$I_{SDM(1)}$	Source-drain Current (pulsed)				44	A
$V_{SD(2)}$	Forward On Voltage	$I_{SD} = 11\text{ A}, V_{GS} = 0$			1.2	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 11\text{ A}, di/dt = 100\text{ A}/\mu\text{s},$		45		ns
$Q_{rr}$	Reverse Recovery Charge	$V_{DD} = 20\text{ V}, T_j = 150^\circ\text{C}$		52		nC
$I_{RRM}$	Reverse Recovery Current	(see test circuit, Figure 5)		2.3		A

Note: 1. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.  
2. Pulse width limited by safe operating area.

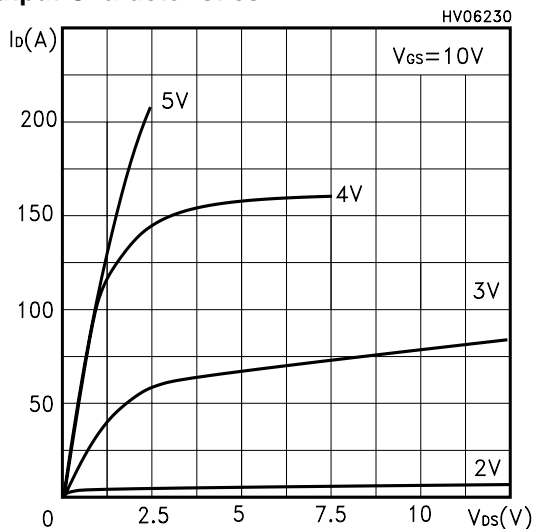
**Safe Operating Area**



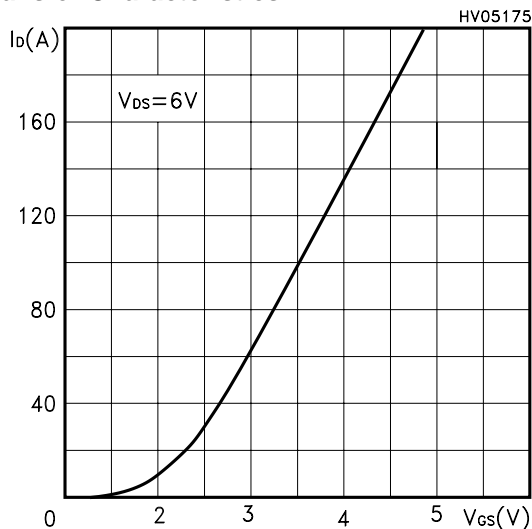
**Thermal Impedance**



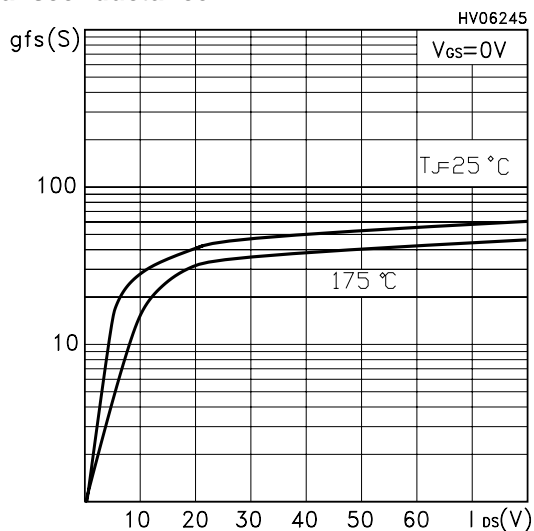
Output Characteristics



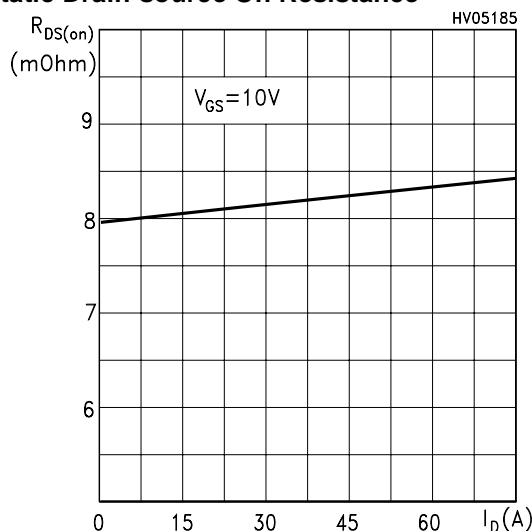
Transfer Characteristics



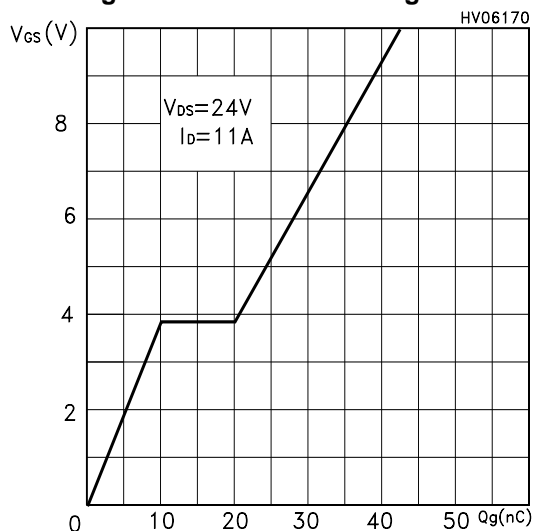
Transconductance



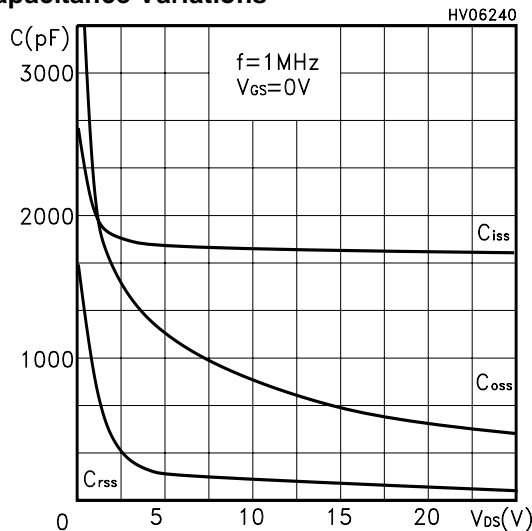
Static Drain-source On Resistance



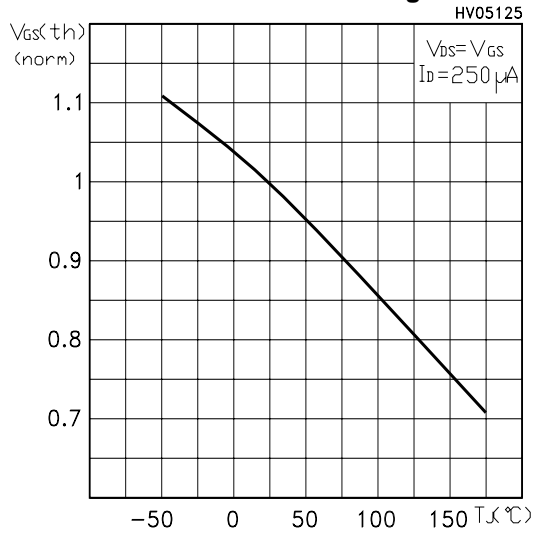
Gate Charge vs Gate-source Voltage



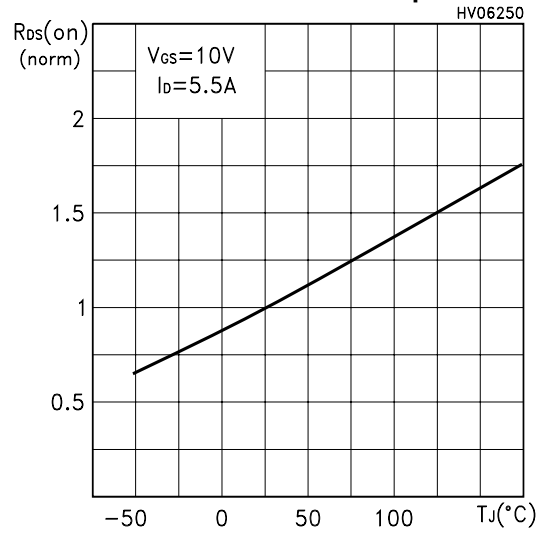
Capacitance Variations



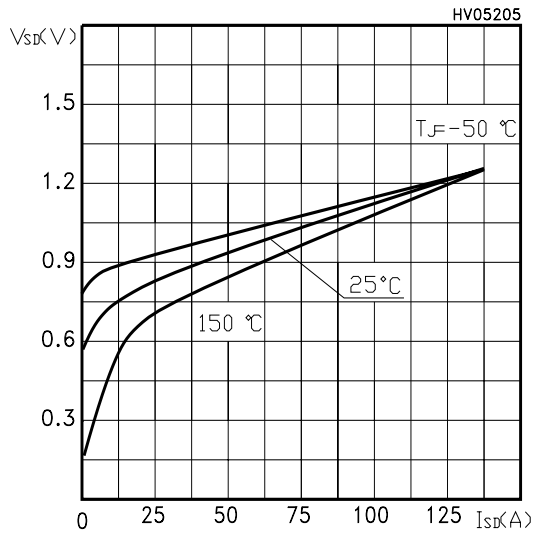
**Normalized Gate Threshold Voltage vs Temp.**



**Normalized On Resistance vs Temperature**



**Source-drain Diode Forward Characteristics**



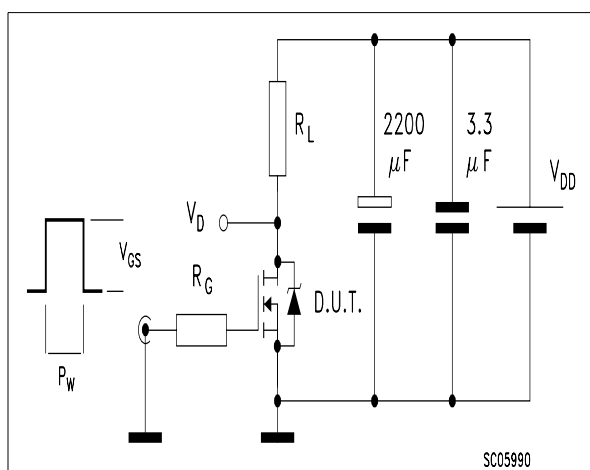
**Fig. 1: Unclamped Inductive Load Test Circuit**



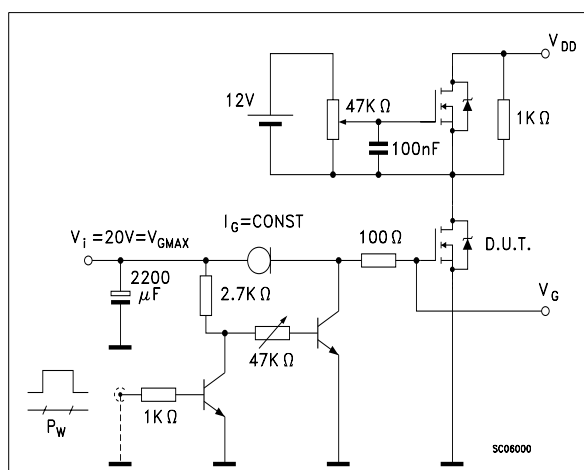
**Fig. 2: Unclamped Inductive Waveform**



**Fig. 3: Switching Times Test Circuit For Resistive Load**



**Fig. 4: Gate Charge test Circuit**

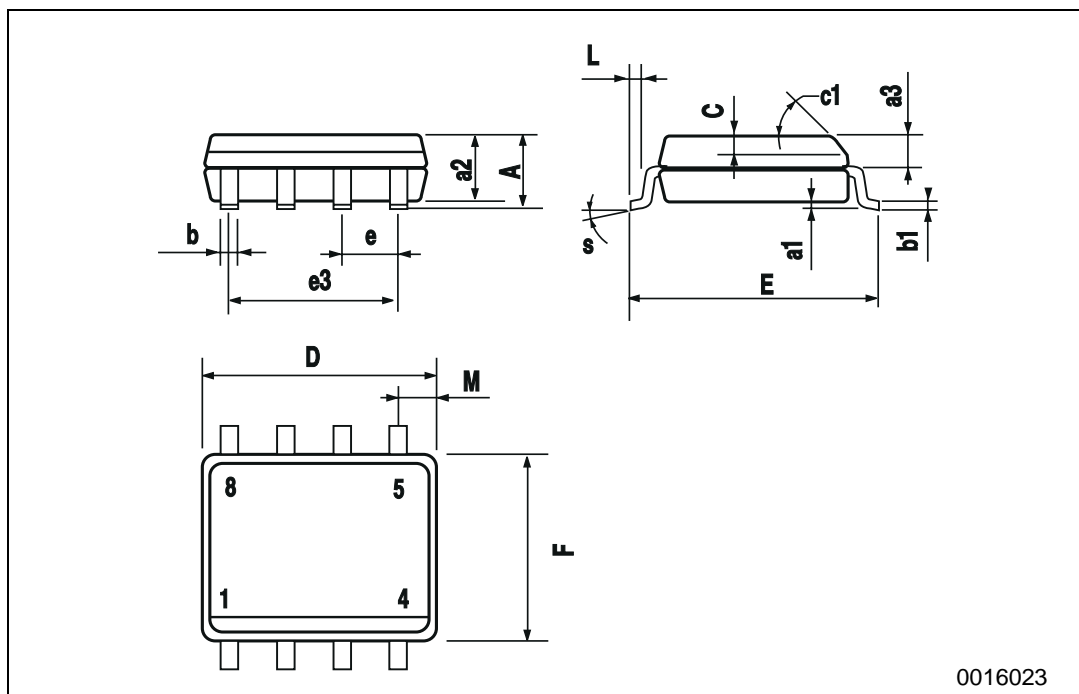


**Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times**



**SO-8 MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



0016023

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a trademark of STMicroelectronics

© 2001 STMicroelectronics – Printed in Italy – All Rights Reserved

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco -  
Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.

<http://www.st.com>