FAIRCHILD
SEMICONDUCTOR™

July 2000
PRELIMINARY

ML4833*

Electronic Dimming Ballast Controller

GENERAL DESCRIPTION

The ML4833 is a complete solution for a dimmable or a non-dimmable, high power factor, high efficiency electronic ballast. The BiCMOS ML4833 contains controllers for "boost" type power factor correction as well as for a dimming ballast. The ML4833 was designed to minimize the number of external components required to build an electronic ballast.

The PFC circuit uses a new, simple PFC topology which requires only one loop for compensation. This system produces a power factor of better than 0.99 with low input current THD. An overvoltage protection comparator inhibits the PFC section in the event of a lamp out or lamp failure condition.

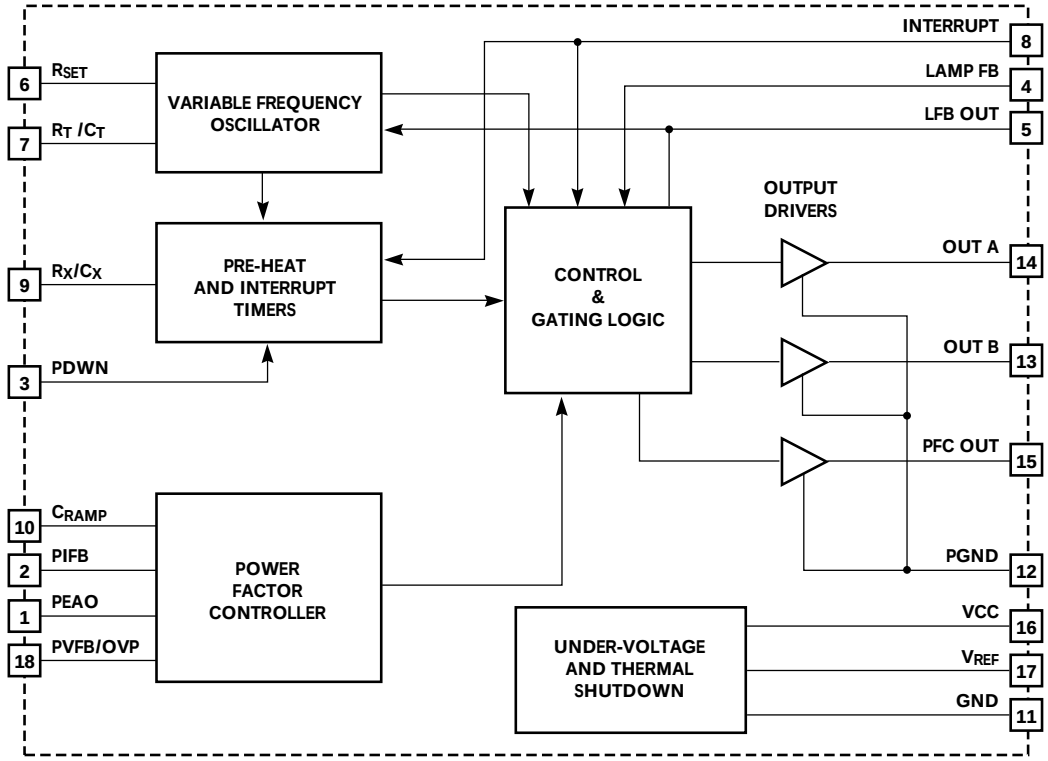
The ballast controller section provides for programmable starting sequence with individually adjustable preheat and lamp out-of-socket interrupt times. The IC controls lamp output power through feedback. The ML4833 provides a power down input which reduces power to the lamp, for GFI, end of life, etc.

FEATURES

- Complete power factor correction and dimming ballast control in one IC
- Low distortion, high efficiency continuous boost, peak current sensing PFC section
- Programmable start scenario for rapid or instant start lamps
- Lamp current feedback for dimming control
- Variable frequency dimming and starting
- Programmable restart for lamp out condition to reduce ballast heating
- Internal over-temperature shutdown replaces external heat sensor
- PFC overvoltage comparator eliminates output "runaway" due to load removal
- Low start-up current <0.5mA
- Power reduction pin for end of life and GFI detectors

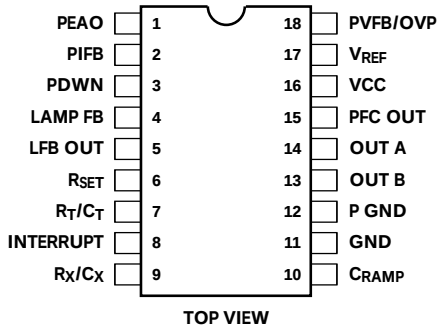
(* Indicates part is End Of Life as of July 1, 2000)

BLOCK DIAGRAM

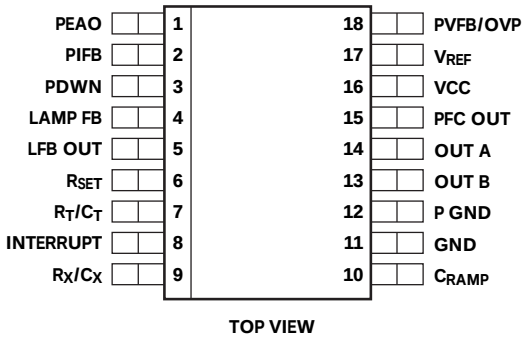


PIN CONFIGURATION

ML4833
18-Pin DIP (P18)



ML4833
18-Pin SOIC (S18)



PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	PEAO	PFC error amplifier output and compensation node.
2	PIFB	Sensing of the inductor current and peak current sense point of the PFC cycle by cycle current limit comparator.
3	PDWN	A one volt comparator threshold that switches the operating frequency to the preheat frequency when exceeded.
4	LAMP FB	Inverting input of an error amplifier used to sense (and regulate) lamp arc current. Also the input node for dimming control.
5	LFB OUT	Output of the lamp current error transconductance amplifier used for lamp current loop compensation.
6	R_{SET}	External resistor which sets oscillator F_{MAX}, and R(X)/C(X) charging current.
7	R_T/C_T	Oscillator timing components.
8	INTERRUPT	Input used for lamp-out detection and restart. A voltage less than 1.25 volts resets the chip and causes a restart after a programmable interval.
9	R_X/C_X	Sets the timing for the preheat, dimming lockout, and interrupt.
10	C_{RAMP}	Integrated voltage of the error amp out.
11	GND	Ground.
12	P GND	Power ground for the IC.
13	OUT B	Ballast MOSFET drive output.
14	OUT A	Ballast MOSFET drive output.
15	PFC OUT	Power Factor MOSFET drive output.
16	VCC	Positive supply for the IC.
17	V_{REF}	Buffered output for the 7.5V voltage reference.
18	PVFB/OVP	Inverting input to PFC error amplifier and OVP comparator input.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Current (I_{CC}) 60mA
Output Current, Source or Sink
(OUT A, OUT B, PFC OUT) DC 250mA
Output Energy (capacitive load per cycle)..... 1.5 mJ
Analog Inputs
(LAMP FB, INTERRUPT, VCC) .....–0.3V to V_{CC} –2V
PIFB input voltage .....–1.5V to 2V
Maximum Forced Voltage
(PEAO, LFB OUT) .....–0.3V to 7.7V
Maximum Forced Current (PEAO, LFB OUT) ..... ±20mA
Junction Temperature ..... 150°C
Storage Temperature Range .....–65°C to 150°C
Lead Temperature (Soldering 10 sec.) ..... 260°C
Thermal Resistance (θ_{JA})
ML4833CP .....70°C/W
ML4833CS .....100°C/W

OPERATING CONDITIONS

Temperature Range .....0°C to 85°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, R_{SET} = 22.1ký, R_T = 15.8kΩ, C_T = 1.5nF, C_{VCC} = 1µF, V_{CC} = 12.5V. (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Lamp Current Amplifier (LAMP FB, LFB OUT)					
Input Bias Current			–0.3	–1.0	µA
Small Signal Transconductance		35	65	105	µ℧
Input Voltage Range		–0.3		5.0	V
Output Low	Voltage at LAMP FB = 3V, R_L =		0.2	0.4	V
Output High	Voltage at LAMP FB = 2V, R_L =	7.1	7.5	7.8	V
Source Current	Voltage at LAMP FB = 0V, LFB OUT = 7V, T_A = 25°C	–0.05	–0.15	–0.25	mA
Sink Current	Voltage at LAMP FB = 5V, LFB OUT = 0.3V, T_A = 25°C	0.05	0.12	0.22	mA
PFC Voltage Feedback Amplifier (PEAO, PVFB/OVP)					
Input Bias Current			–0.3	–1.0	µA
Small Signal Transconductance		35	65	105	µ℧
Input Voltage Range		–0.3		5.0	V
Output Low	Voltage at PVFB = 3V, R_L =		0.2	0.4	V
Output High	Voltage at PVFB = 2V, R_L =	6.5	6.8	7.1	V
Source Current	Voltage at PVFB/OVP = 0V, PEAO = 6V, T_A = 25°C	–0.05	–0.15	–0.25	mA
Sink Current	Voltage at PVFB/OVP = 3V, PEAO = 0.3V, T_A = 25°C	0.03	0.07	0.16	mA
PFC Current — Limit Comparator (PIFB)					
Current-Limit Threshold		–0.90	–1.05	–1.15	V
Propagation Delay	100mV step and 100mV overdrive		100		ns
Oscillator					
Initial Accuracy	T_A = 25°C	72	76	80	kHz
Voltage Stability	V_{CCZ} – 4.5V < V_{CC} <V_{CCZ} – 0.5V		1		%
Temperature Stability			2		%
Total Variation	Line, temperature	69		83	kHz
Ramp Valley to Peak			2.5		V

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator (Continued)					
C_T Charging Current	Voltage at LAMP FB = 3V, R_T/C_T = 2.5V, R_X/C_X = 0.9V (Preheat)	–90	–110	–130	µA
	LAMP FB = 3V, R_T/C_T = 2.5V, R_X/C_X = Open	–180	–220	–260	µA
C_T Discharge Current	Voltage at R_T/C_T = 2.5V	4.0	5.5	7.0	mA
Output Drive Deadtime		0.65	1	1.35	µs
Reference Section					
Output Voltage	T_A = 25°C, I_O = 1mA	7.4	7.5	7.6	V
Line regulation	V_{CCZ} – 4.5V < V_{CC} < V_{CCZ} – 0.5V		2	35	mV
Load regulation	1mA < I_O < 5mA		2	15	mV
Temperature stability			0.4		%
Total Variation	Line, load, temp	7.35		7.65	V
Output Noise Voltage	10Hz to 10kHz		50		µV
Long Term Stability	T_J = 125°C, 1000 hrs		5		mV
Preheat and Interrupt Timer (R_X/C_X where R_X = 680ký, C_X = 4.7µF)					
Initial Preheat Period			0.8		s
Subsequent Preheat Period			0.7		s
Start Period			1.2		s
Interrupt Period			5.7		s
R_X/C_X Charging Current		–24	–28	–33	µA
R_X/C_X Open Circuit Voltage	V_{CC} < Start-up threshold	0.4	0.7	1.0	V
R_X/C_X Maximum Voltage		7.0	7.3	7.7	V
Input Bias Current	Voltage at C_{RAMP} = 1.2V			0.1	µA
Preheat Lower Threshold		1.05	1.22	1.36	V
Preheat Upper Threshold		4.2	4.7	5.1	V
Interrupt Recovery Threshold		1.05	1.22	1.36	V
Start Period End Threshold		6.05	6.6	7.35	V
Interrupt Input (INTERRUPT)					
Interrupt Threshold		1.1	1.22	1.4	V
Input Bias Current				0.1	µA
R_{SET} Voltage		2.4	2.5	2.6	V
OVP Comparator (PVFB/OVP)					
OVP Threshold		2.63	2.73	2.83	V
Hysteresis		0.18	0.23	0.27	V
Propagation Delay			1.4		µs

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Outputs (OUT A, OUT B, PFC OUT)					
Output Voltage Low	I_{OUT} = 20mA		0.1	0.2	V
	I_{OUT} = 200mA		1.0	2.0	V
Output Voltage High	I_{OUT} = –20mA	V_{CC} – 0.2	V_{CC} – 0.1		V
	I_{OUT} = –200mA	V_{CC} – 2.0	V_{CC} – 1.0		V
Output Voltage Low in UVLO	I_{OUT} = 10mA, V_{CC} < Start-up threshold			0.2	V
Output Rise/Fall Time	C_L = 1000pF		20		ns
Under-Voltage Lockout and Bias Circuits					
IC Shunt Protection Voltage (V_{CCZ})	I_{CC} = 15mA	14.2	15.0	15.8	V
Start-up Current	V_{CC} - Start-up threshold		0.34	0.48	mA
Operating Current	V_{CC} = 12.5V, Voltage at LAMP FB = 0V, LFB OUT = 2.3, PVFB/OVP = 2.3V PIFB = Open		5.5	8.0	mA
Start-up Threshold		V_{CC} – 1.2	V_{CCZ} – 1.0	V_{CC} – 0.8	V
Shutdown Threshold		V_{CC} – 5.3	V_{CCZ} – 4.8	V_{CC} – 4.3	V
Shutdown Temperature (T_{DWN})	(Note 2)		130		°C
Hysteresis (T_{DWN})			30		°C
PDWN					
PDWN Threshold		0.9	1.0	1.1	V

Note 1: Limits are guaranteed by 100% testing, sampling or correlation with worst case test conditions.
Note 2: Junction temperature.

FUNCTIONAL DESCRIPTION

OVERVIEW

The ML4833 consists of peak current controlled continuous boost power factor front end section with a flexible ballast control section. Start-up and lamp-out retry timing are controlled by the selection of external timing components, allowing for control of a wide variety of different lamp types. The ballast section controls the lamp power using frequency modulation (FM) with additional programmability provided to adjust the VCO frequency range. This allows for the IC to be used with a variety of different output networks. Figure 1 depicts a detailed block diagram of ML4833.

POWER FACTOR SECTION

The ML4833 power factor section is a peak current sensing boost mode PFC control circuit in which only voltage loop compensation is needed. It is simpler than a conventional average current control method. It consists of a voltage error amplifier, a current sense amplifier (no compensation is needed), an integrator, a comparator, and a logic control block. In the boost topology, power factor correction is achieved by sensing the output voltage and the current flowing through the current sense resistor. Duty cycle control is achieved by comparing the integrated voltage signal of the error amplifier and the voltage across R_{SENSE}. The duty cycle control timing is shown in Figure 2. Setting minimum input voltage for output regulation can be achieved by selecting C_{RAMP} according to equation 1.

$$C_{RAMP} = \frac{PEAO_{MAX}}{22K}\left\{(1-D)Ts - 1.1\mu s\right\}\frac{1}{\left[\frac{\sqrt{2}P_{OUT}}{V_{IN}} - \left(\frac{V_{OUT} - \sqrt{2}V_{IN}}{2L}\right)(1-D)Ts\right]8R_{SENSE}} \quad (1)$$

OVERVOLTAGE PROTECTION AND INHIBIT

The OVP pin serves to protect the power circuit from being subjected to excessive voltages if the load should change suddenly (lamp removal). A divider from the high voltage DC bus sets the OVP trip level. When the voltage on PVFB/OVP exceeds 2.75V, the PFC transistor are inhibited. The ballast section will continue to operate.

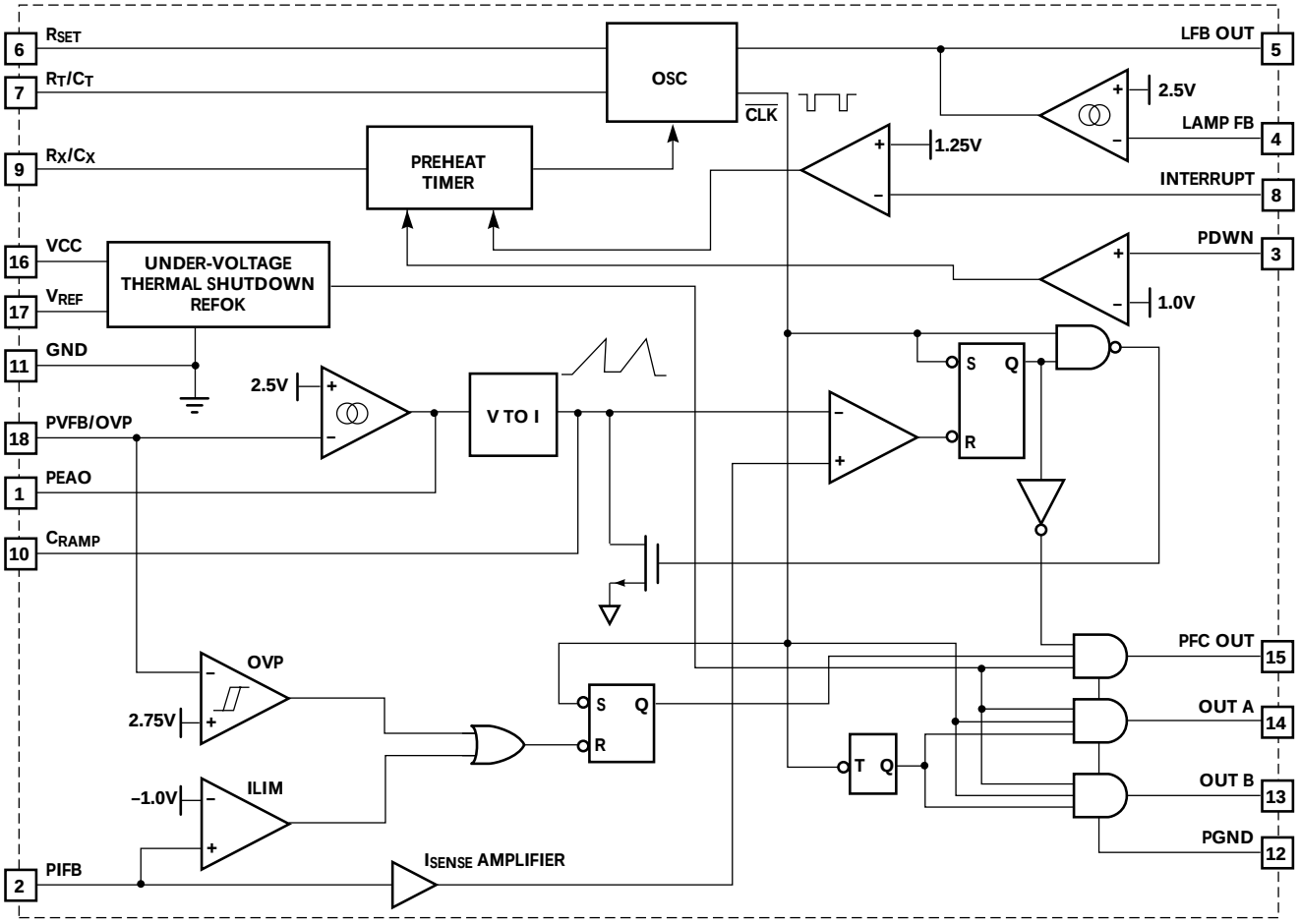


Figure 1. ML4833 Detailed Block Diagram

TRANSCONDUCTANCE AMPLIFIERS

The PFC voltage feedback amplifier is implemented as an operational transconductance amplifier. It is designed to have low small signal forward transconductance such that a large value of load resistor (R1) and a low value ceramic capacitor (<1µF) can be used for AC coupling (C1) in the frequency compensation network. The compensation network shown in Figure 3 will introduce a zero and a pole at:

$$f_Z = \frac{1}{2\pi R_1 C_1} \qquad f_P = \frac{1}{2\pi R_1 C_2} \qquad (2)$$

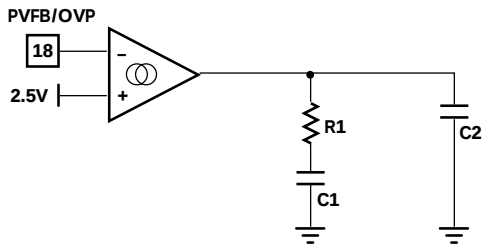


Figure 3. Compensation Network

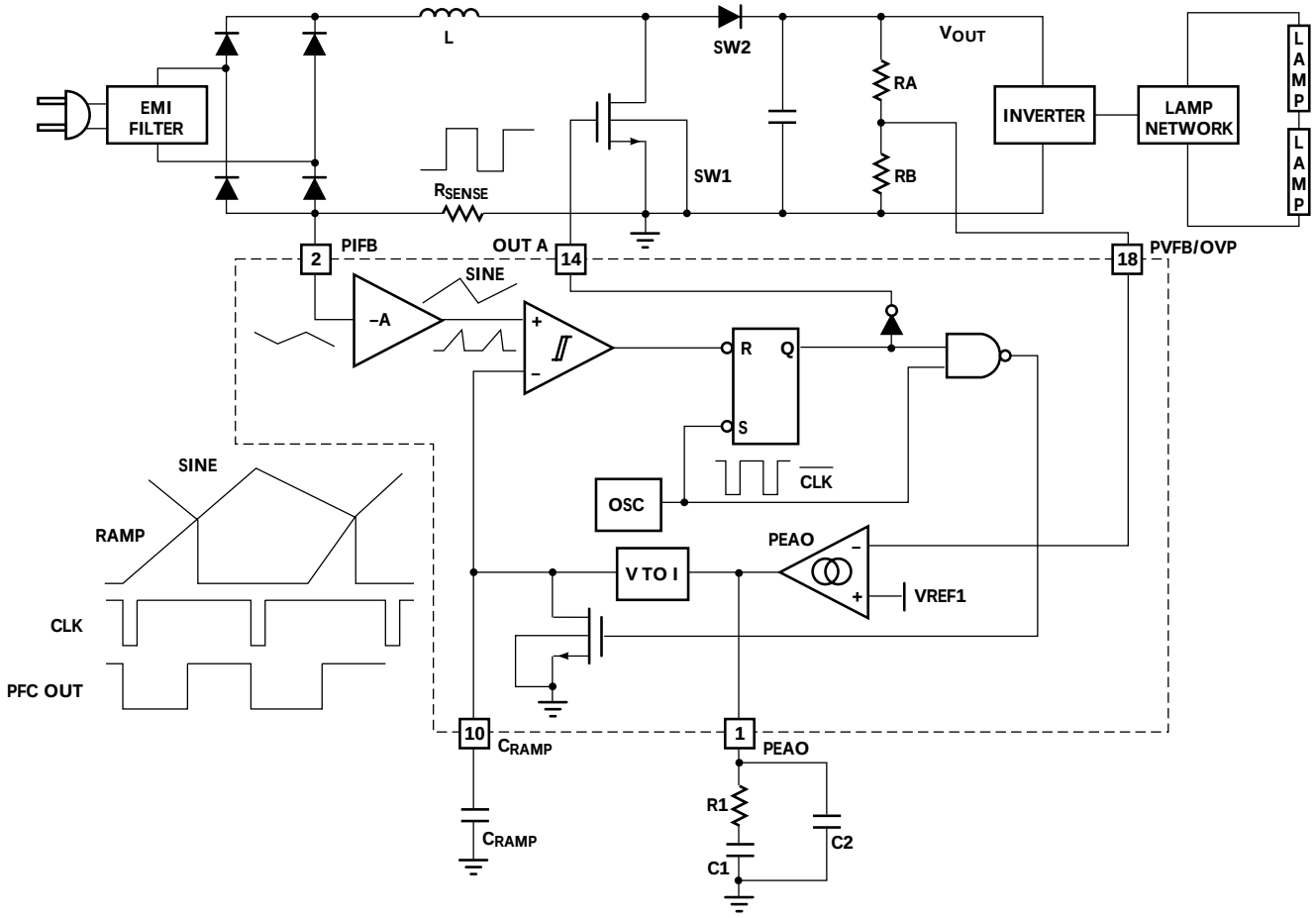


Figure 2. ML4833 PFC Controller Section

Figure 4 shows the output configuration for the operational transconductance amplifiers.

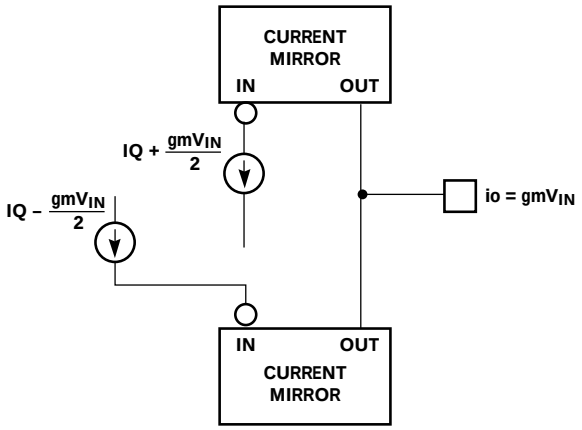


Figure 4. Output Configuration

A DC path to ground or V_{CC} at the output of the transconductance amplifiers will introduce an offset error. The magnitude of the offset voltage that will appear at the input is given by V_{OS} = io/gm. For an io of 1µA and a gm of 0.05 µ℧ the input referred offset will be 20mV. Capacitor C1 as shown in Figure 3 is used to block the DC current to minimize the adverse effect of offsets.

Slew rate enhancement is incorporated into all of the operational transconductance amplifiers in the ML4833. This improves the recovery of the circuit in response to power up and transient conditions. The response to large signals will be somewhat non-linear as the transconductance amplifiers change from their low to high transconductance mode. This is illustrated in Figure 5.

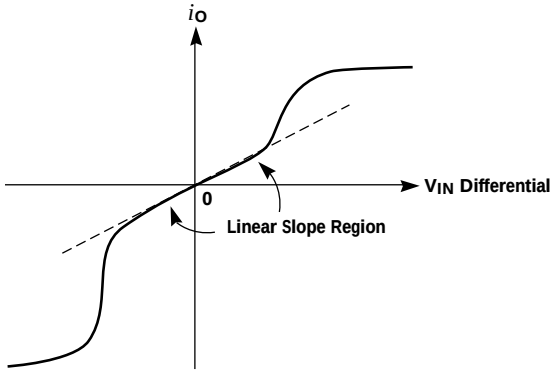


Figure 5. Transconductance Amplifier Characteristics

BALLAST OUTPUT SECTION

The IC controls output power to the lamps via frequency modulation with non-overlapping conduction. This means that both ballast output drivers will be low during the discharging time t_{DIS} of the oscillator capacitor C_T.

OSCILLATOR

The VCO frequency ranges are controlled by the output of the LFB amplifier (R_{SET}). As lamp current increases, LFB OUT falls in voltage, causing the C_T charging current to increase, thereby causing the oscillator frequency to increase. Since the ballast output network attenuates high frequencies, the power to the lamp will be decreased.

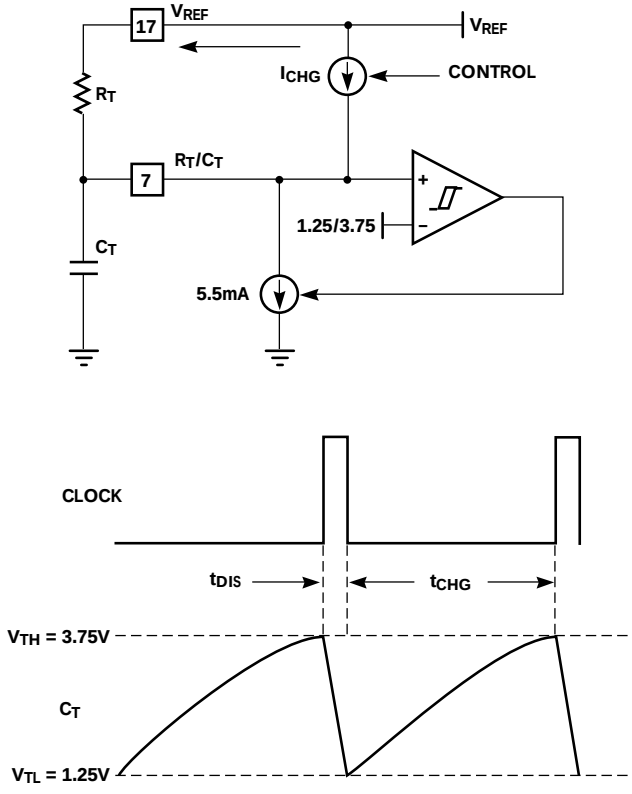


Figure 6. Oscillator Block Diagram and Timing

The oscillator frequency is determined by the following equations:

$$F_{OSC} = \frac{1}{t_{CHG} + t_{DIS}} \quad (3)$$

and

$$t_{CHG} = R_T C_T \ln\left(\frac{V_{REF} + I_{CH} R_T - V_{TL}}{V_{REF} + I_{CH} R_T - V_{TH}}\right) \quad (4)$$

The oscillator's minimum frequency is set when I_{CH} = 0 where:

$$F_{OSC} \cong \frac{1}{0.51 \times R_T C_T} \quad (5)$$

This assumes that $t_{CHG} >> t_{DIS}$.

When LFB OUT is high, $I_{CH} = 0$ and the minimum frequency occurs. The charging current varies according to two control inputs to the oscillator:

1. The output of the preheat timer
2. The voltage at LFB OUT (lamp feedback amplifier output)

In preheat condition, charging current is fixed at

$$I_{CHG(PREHEAT)} = \frac{2.5}{R_{SET}} \quad (6)$$

In running mode, charging current decreases as the voltage rises from 0V to V_{OH} at the LAMP FB amplifier. The highest frequency will be attained when I_{CHG} is highest, which is attained when voltage at LFB OUT is at 0V:

$$I_{CHG(0)} = \frac{5}{R_{SET}} \quad (7)$$

Highest lamp power, and lowest output frequency are attained when voltage at LFB OUT is at its maximum output voltage (V_{OH}).

In this condition, the minimum operating frequency of the ballast is set per equation 5 above.

For the IC to be used effectively in dimming ballasts with higher Q output networks a larger C_T value and lower R_T value can be used, to yield a smaller frequency excursion over the control range (voltage at LFB OUT). The discharge current is set to 5mA. Assuming that $I_{DIS} >> I_{RT}$:

$$t_{DIS(VCO)} \cong 600 \times C_T \quad (8)$$

IC BIAS, UNDER-VOLTAGE LOCKOUT AND THERMAL SHUTDOWN

The IC includes a shunt clamp which will limit the voltage at V_{CC} to 15V (V_{CCZ}). The IC should be fed with a current limited source, typically derived from the ballast transformer auxiliary winding. When V_{CC} is below V_{CCZ} – 1.1V, the IC draws less than 0.48mA of quiescent current and the outputs are off. This allows the IC to start using a "bleed resistor" from the rectified AC line.

To help reduce ballast cost, the ML4833 includes a temperature sensor which will inhibit ballast operation if the IC's junction temperature exceeds 120°C. In order to use this sensor in lieu of an external sensor, care should be taken when placing the IC to ensure that it is sensing temperature at the physically appropriate point in the ballast. The ML4833's die temperature can be estimated with the following equation:

$$T_J \cong T_A + (P_D + 65°C/W) \quad (9)$$

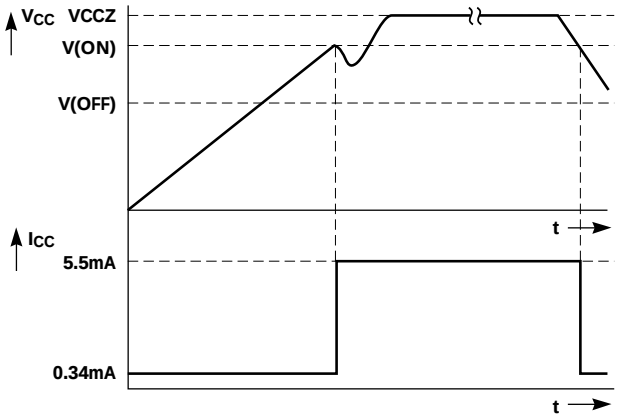


Figure 7. Typical V_{CC} and I_{CC} Waveforms when the ML4833 is Started with a Bleed Resistor from the Rectified AC Line and Bootstrapped from an Auxiliary Winding.

STARTING, RE-START, PREHEAT AND INTERRUPT

The lamp starting scenario implemented in the ML4833 is designed to maximize lamp life and minimize ballast heating during lamp out conditions.

The circuit in Figure 8 controls the lamp starting scenarios: Filament preheat and lamp out interrupt. C_X is charged with a current of $I_{R(SET)}/4$ and discharged through R_X. The voltage at C_X is initialized to 0.7V (V_{BE}) at power up. The time for C_X to rise to 4.8V is the filament preheat time. During that time, the oscillator charging current (I_{CHG}) is $2.5/R_{SET}$. This will produce a high frequency for filament preheat, but will not produce sufficient voltage to ignite the lamp or cause significant glow current.

After cathode heating, the inverter frequency drops to F_{MIN} causing a high voltage to appear to ignite the lamp. If lamp current is not detected when the lamp is supposed to have ignited, the lamp voltage feedback coming into pin 8 remains below 1.25V, the C_X charging current is shut off and the inverter is inhibited until C_X is discharged by R_X to the 1.2V threshold. Shutting off the inverter in this manner prevents the inverter from generating excessive heat when the lamp fails to strike or is out of socket. Typically this time is set to be fairly long by choosing a large value of R_X.

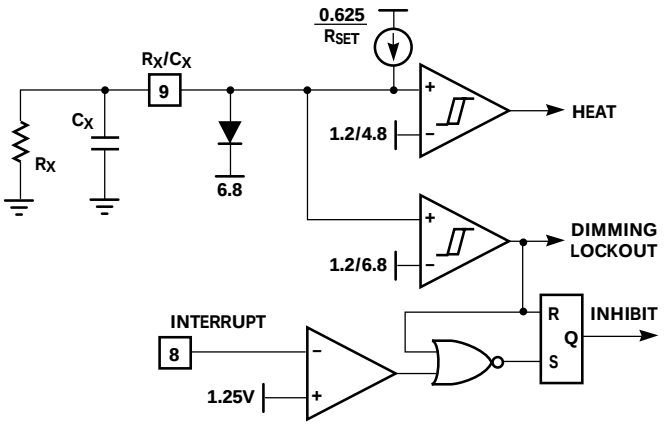


Figure 8. Lamp Preheat and Interrupt Timers

LFB OUT is ignored by the oscillator until C_X reaches 6.8V threshold. The lamps are therefore driven to full power and then dimmed. The C_X pin is clamped to about 7.5V.

A summary of the operating frequencies in the various operating modes is shown below.

Operating Mode	Operating Frequency
Preheat	$\frac{[F(MAX) \text{ to } F(MIN)]}{2}$
Dimming Lock-out	F(MIN)
Dimming Control	F(MIN) to F(MAX)

TYPICAL APPLICATIONS

Figure 10 shows a schematic for a dimming power-factor corrected 60W ballast, designed to operate two F32T8 fluorescent lamps connected in series.

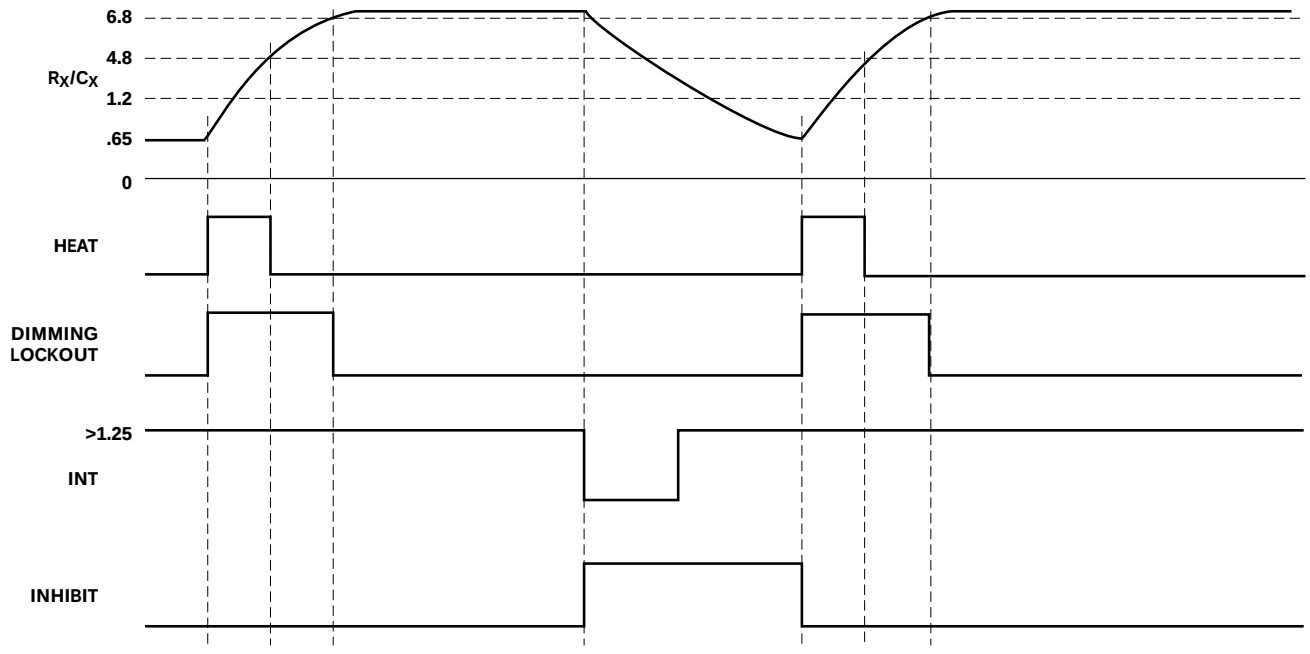


Figure 9. Lamp Starting and Restart Timing

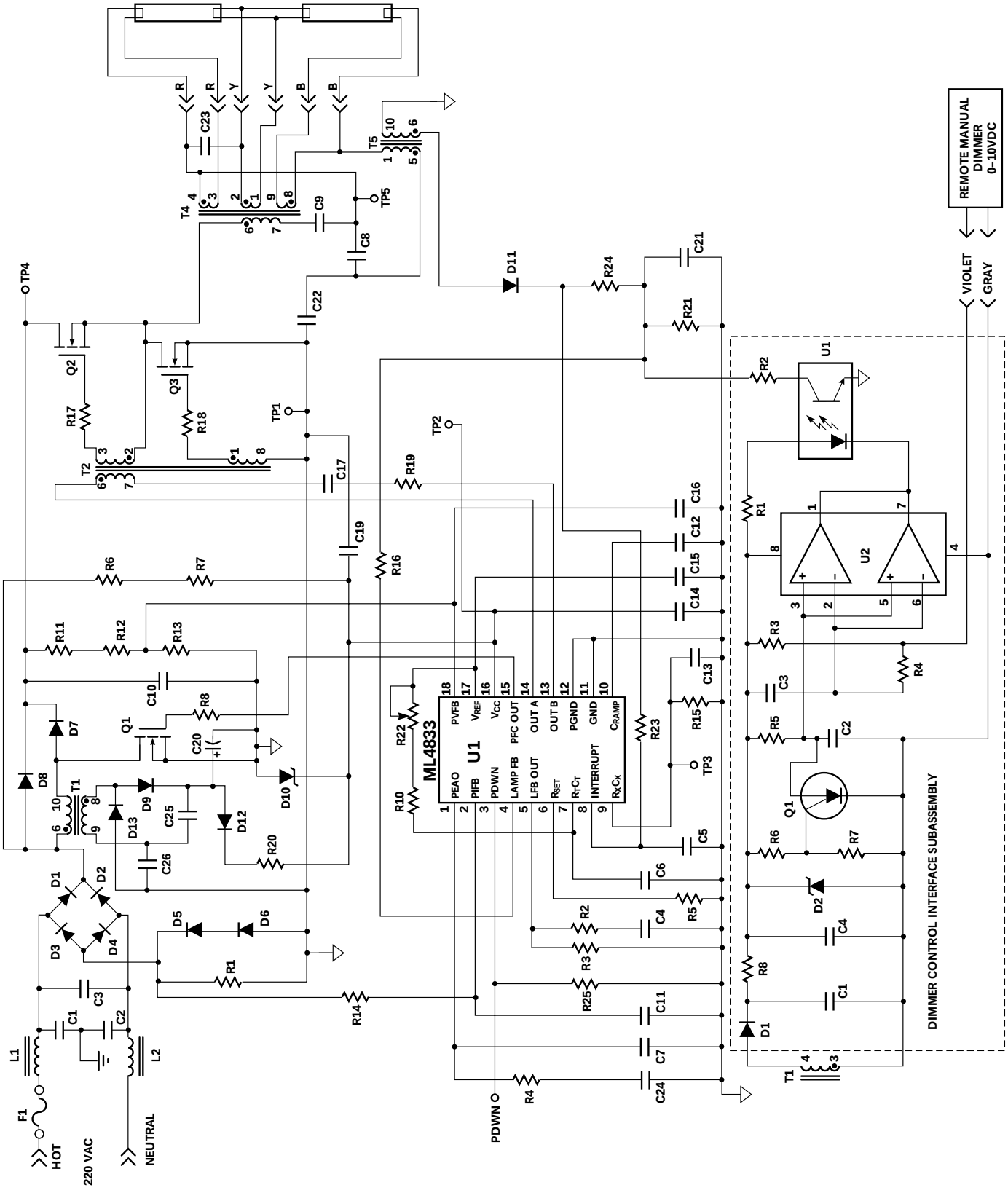
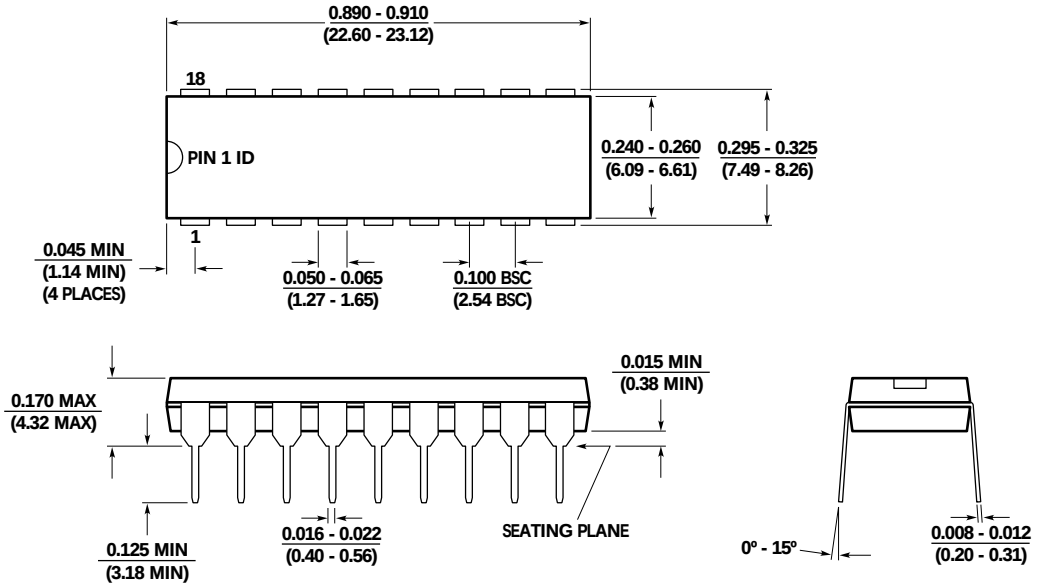


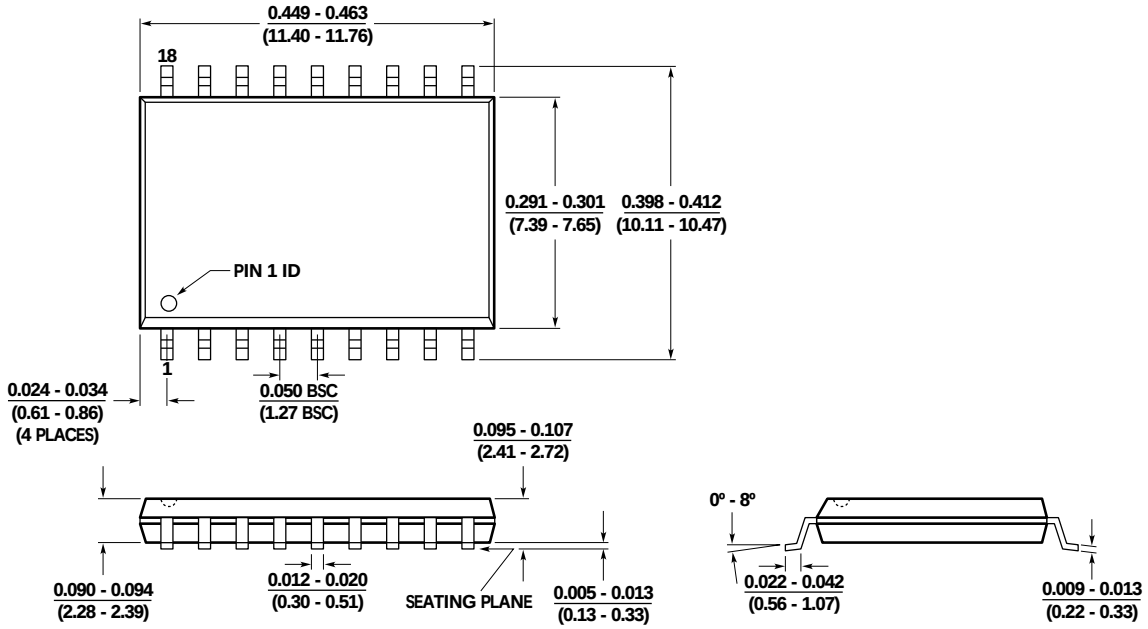
Figure 10. 220V Dimming Ballast

PHYSICAL DIMENSIONS inches (millimeters)

Package: P18
18-Pin PDIP



Package: S18
18-Pin SOIC



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4833CP (End of Life)	0°C to 85°C	Molded DIP (P18)
ML4833CS (Obsolete)	0°C to 85°C	SOIC (S18)