



Am486 Microprocessor PCI Customer Development Platform

Am486 Microprocessor Development System With PCI Expansion and On-Board Am79C972 100MB/s Ethernet Controller

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Rev 1.0: Original design

Rev 1.1: Minor modifications after Design Review

Rev 1.2: Added External 8042 Style Keyboard Controller (SH24)
Removed Support for M1487 Internal KBC (SH15)
Removed Keyboard Interface From Clock Page (SH17)
Changed design name to Am486PCI C.D.P.

Rev 1.3: Added Extra Bypass Capacitors (SH5 & SH14 & SH15 & SH17)
Swapped Around Some Signals Within Resistor Networks (SH6 & SH20)
Renamed MCLK1 net to M_CLK1 (SH24)
Added 0-ohm resistor to make pin 10 & 11 pullup work (SH17)
Added Pin to HSL for NetLister (SH3)
Fixed Error in 3.3V Regulator Circuit (SH12)

Rev 1.4: Rearranged Clock Nets to Facilitate Routing (SH17)
Changed Some Components to Standard Values
(50ohm to 49.9ohm, 1% on SH 13 and 40pF to 39pF,
5% on SH19)

Rev 2.0: Changed SIP resistor packs to 10-pin (SH2, SH3, SH11, SH15, SH16, SH17, SH19, SH20 & SH21)
Changed 330ohm SIP Resistor Pack to 8-pin (SH19)
SH3: Added diagram to correct Power Connector Footprint

SH4 & 5: Broke CPU Logic Analyzer Headers into 2 pages
Added PAL to generate CPU A0 and A1 and also generate a Logic Analyzer Qualify signal
Buffered BE[0..3], RDY#, BRDY#, and ADS# through the new PAL

SH9: Added better explanation of EIP Flash memory operation

SH11: Added configuration information for PCI slots
Removed circuit to generate PCI PERR# to cause
M1487 to assert NMI to Am486 microprocessor

SH13: Added a 4K serial EEPROM for user parameters and mux. circuit to daisy chain it off the 1K device.
'972 E/net device loads its configuration from 1K EEPROM.
CLKCNTL signal from M1487 used to select 1K or 4K EEPROM.

SH14: Swapped R107 and R109; R109 is 49.9ohm, 1%
Fixed wiring error on crystal

SH15: Added 5 more 0.1uF bypass capacitors for new chips ('F14, 'ABT125, 22V10, 'F08, 'C66)

SH16: Fixed wiring error on crystal
Fixed wiring error in generation of low-active reset signal RSTDRV#
Removed unused inverter (used on SH24)
Changed net on NMI pin to 1487NMI for use in new circuit
Changed R58 to be a populated component

Rev 2.0 (continued): SH17: Added jumpers to allow multiple BIOS images in a single Flash ROM device
Removed 1 diode from VBAT generation circuit
Added new NMI generation circuit and spare 'F14 gates
Added jumper for external RESET# pushbutton

SH18: Fixed wiring error on crystal
Removed MCLK1 net (16MHz) and rewired MCLK2 to drive all 33MHz clock nets
Removed CLKCNTL signal from DOZE# pin of U17

SH20: Removed unneeded 0-ohm resistors from Super I/O chip
Fixed wiring error on crystal
Added 'ABT125 buffer to drive serial port LEDs

SH22: MACH device outputs changed for new ISA Flash support

SH23: Changed ISA Flash to 1MByte (512Kx16)

SH24: Removed unneeded logic from RTC interface
Added inverter to generate proper CS# for RTC chip
Fixed wiring error on crystal
Grounded U22-pin 22
Removed 1 unused OR gate for use on SH17

SH25: Switched mouse connector to verticle type
Changed 'F06 symbol to show o/c

Rev 2.1: Updated revision level and prototype warning on all sheets

SH17: Modified ROM jumpers to allow multiple BIOS images in a single Flash ROM device and support 256K or 512K BIOS for non-PC applications

SH22: Added XBUSCSJ signal to Mach device so it does not respond when Am486 fetches the reset vector at FFFF FFFF

SH14 & 15 & 20: Connected pins 1 and 2 on all LEDs for greater purchasing/manufacturing flexibility

Rev 2.1A: SH1: New Rev. of cover sheet text: no design changes made!

SH7: Changed Cache Tag SRAM Speed to 10ns

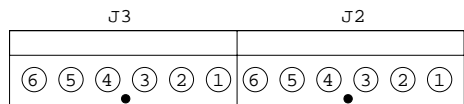
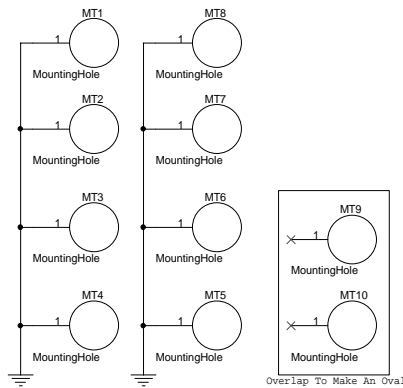
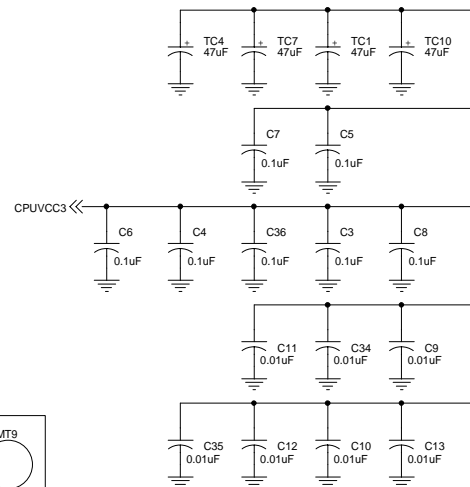
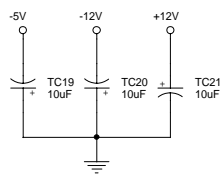
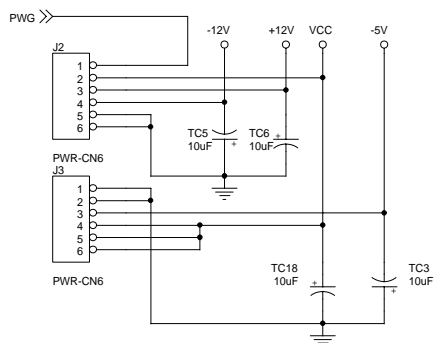
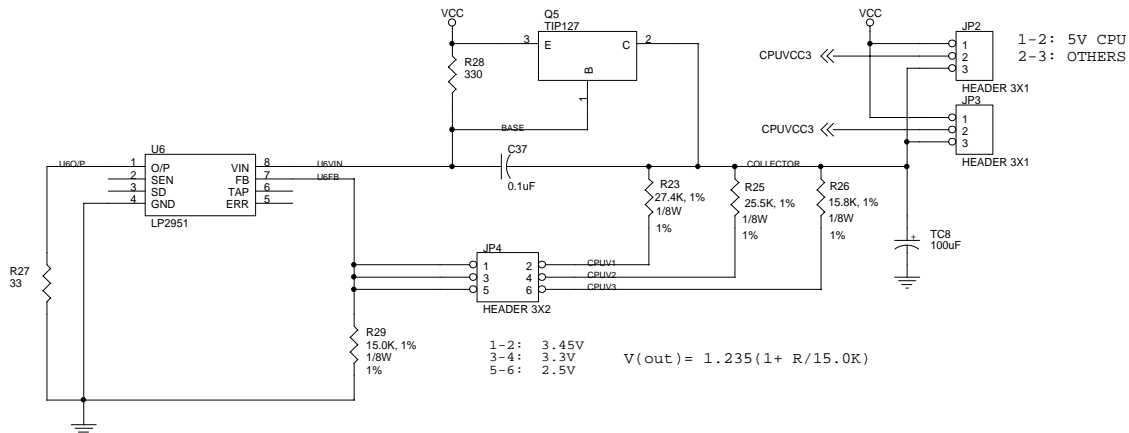
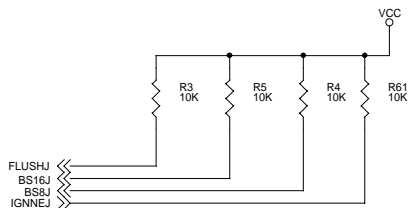
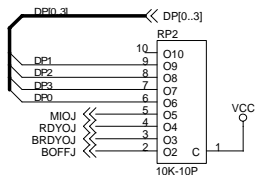
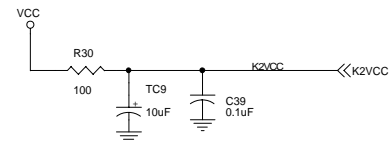
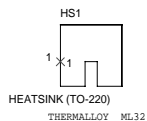
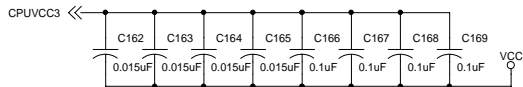
Note: Unless otherwise noted all logic operates off a 5V power supply

Note: Unless otherwise stated the resistors are a 0805 package and 5% Tol.

Note: Unless otherwise stated the capacitors are a 0805 package and 10% Tol.

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Title		Am486 MICROPROCESSOR	
		PCI CUSTOMER DEVELOPMENT PLATFORM	
Size	Document Number	COVER.SCH	Rev 2.1A
Date: Friday, December 18, 1998		Sheet	1 of 26

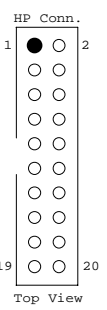
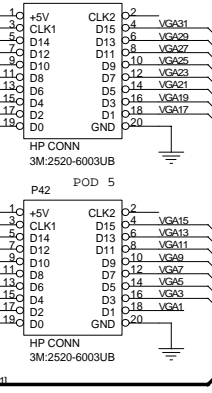
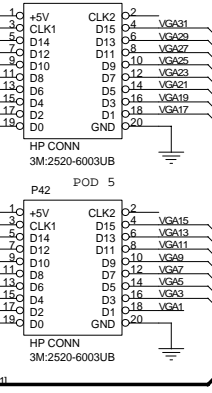
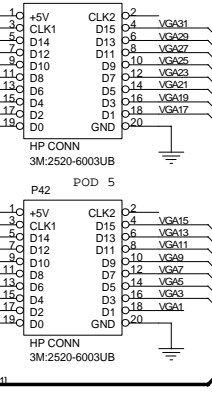
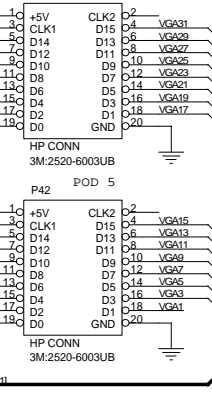
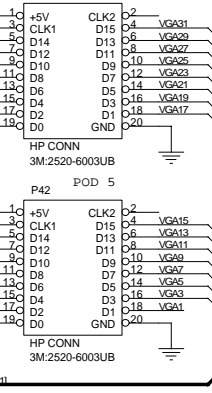
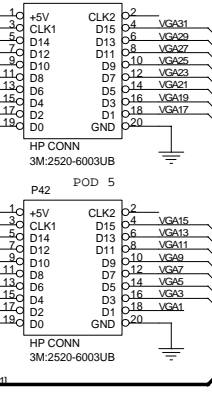
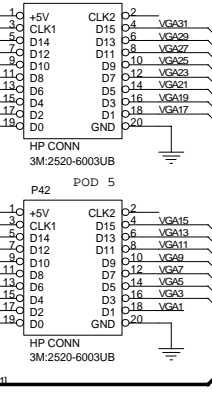
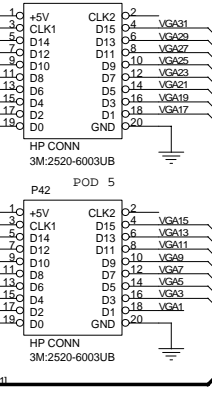
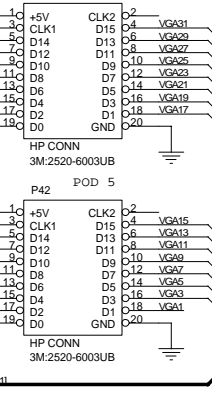
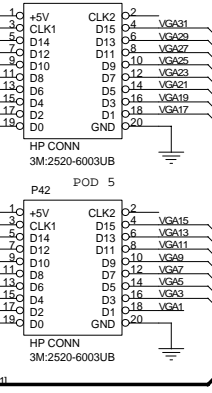
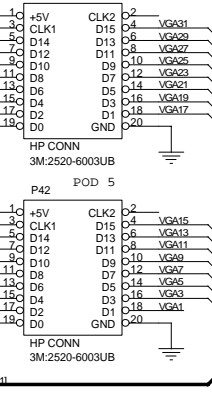
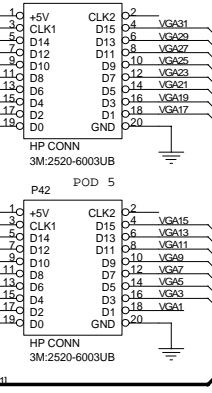
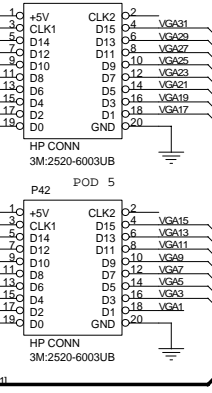
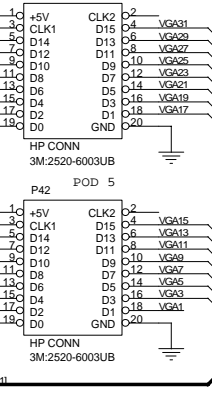
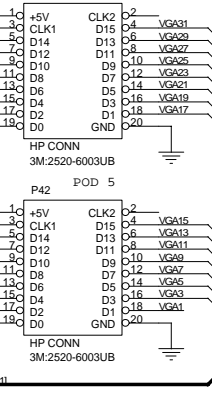
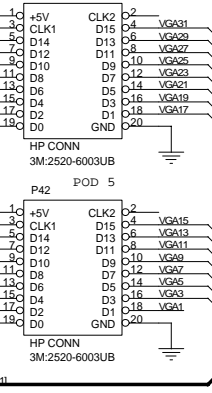
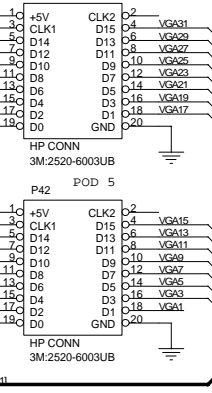
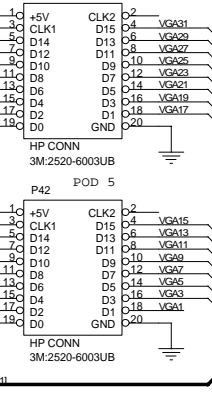
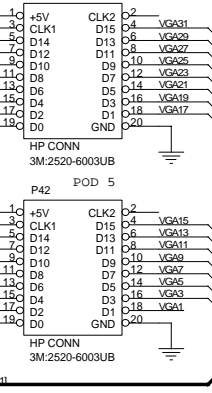
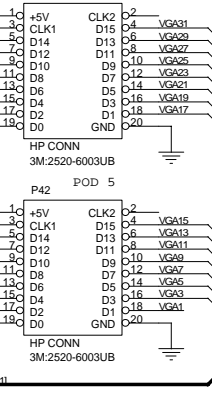
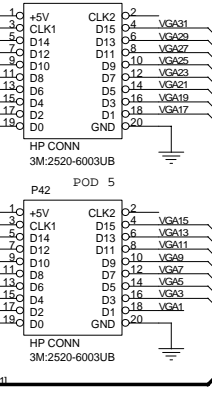
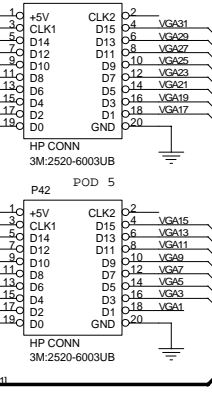
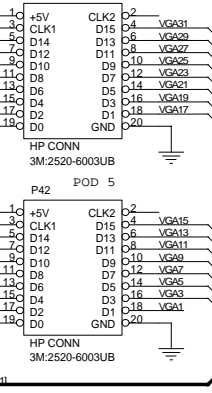
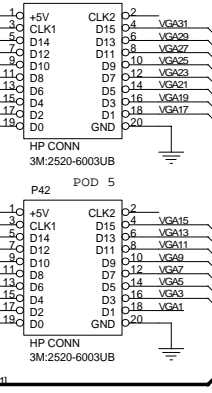
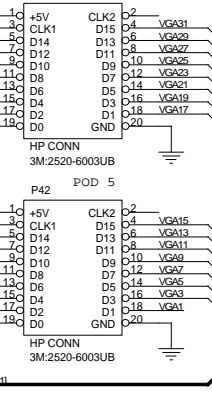
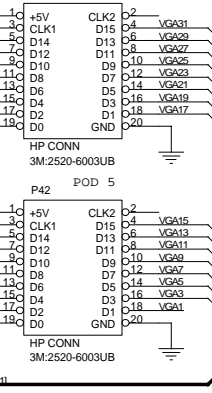
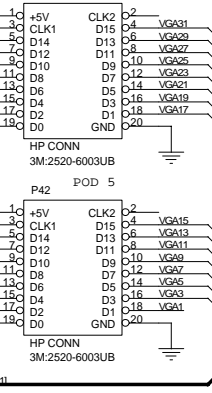
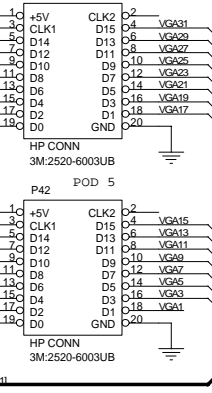
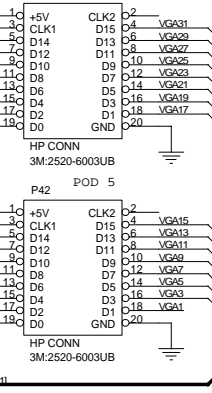
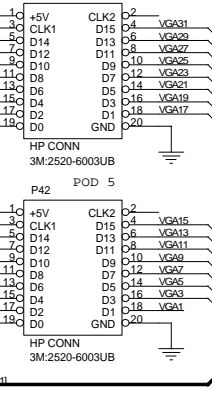
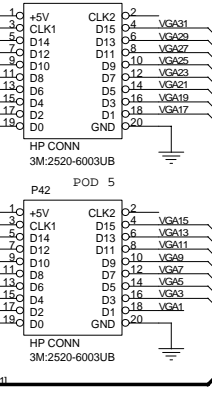
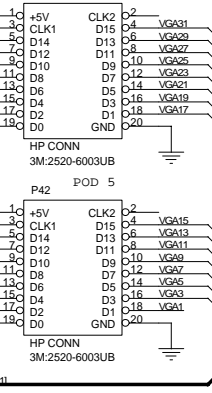
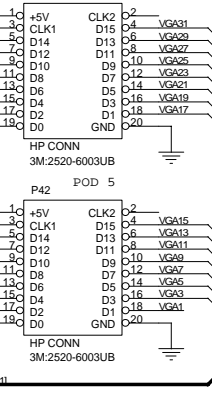
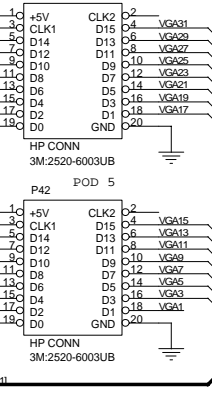
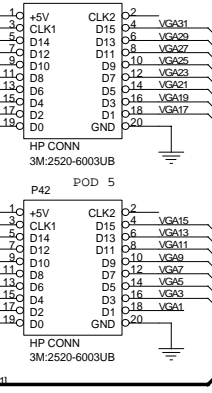
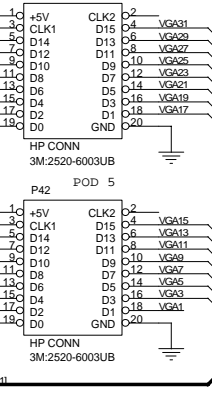
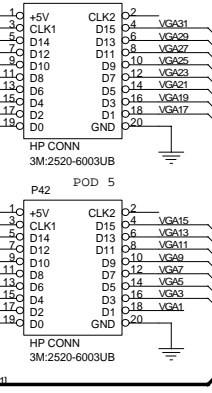
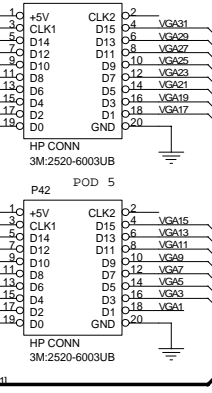
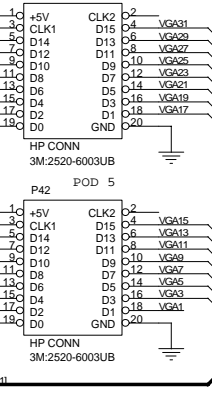
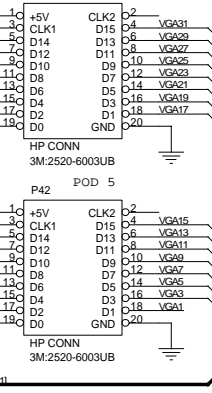
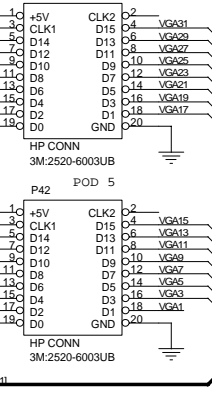
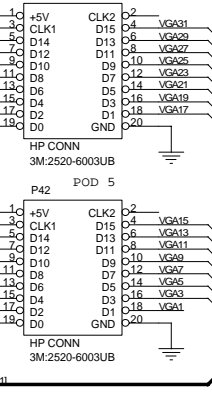
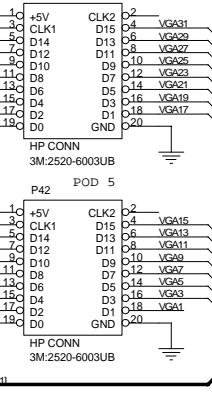
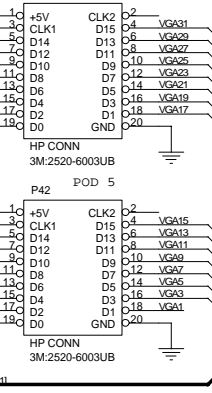
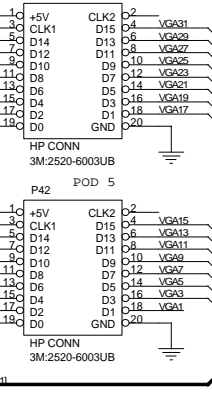
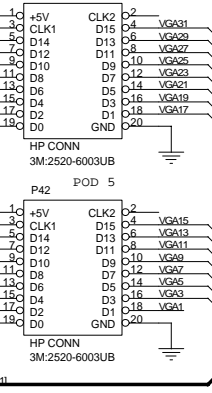
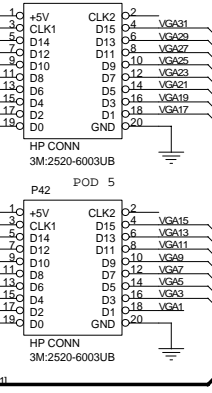
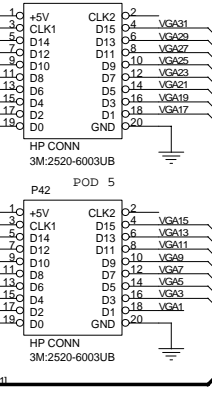
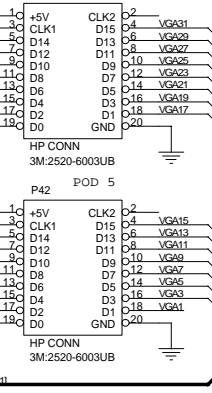
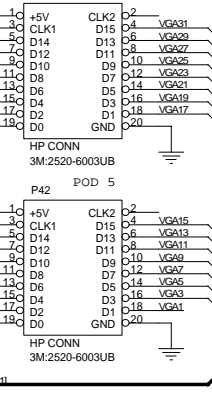
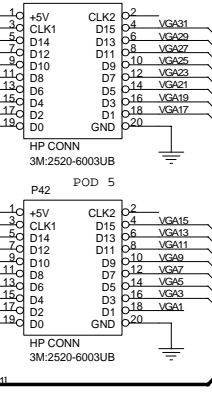
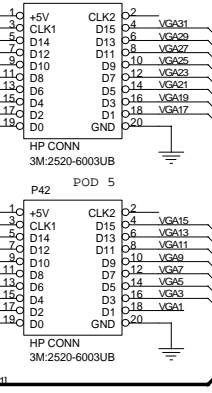
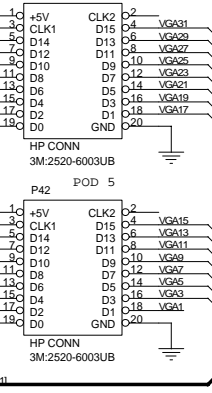
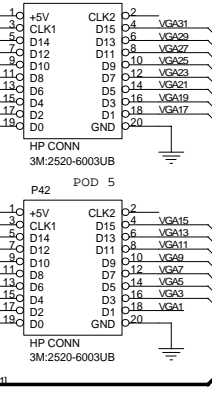
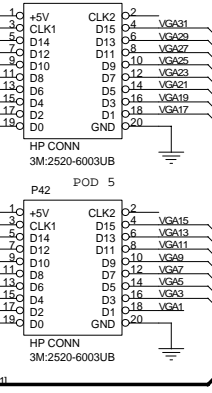
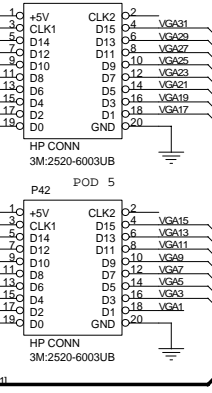
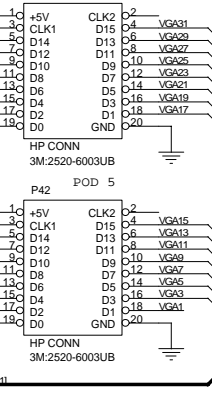
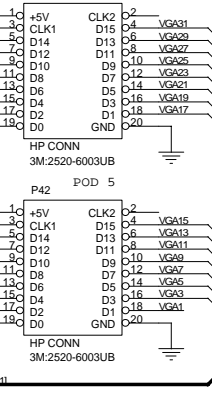
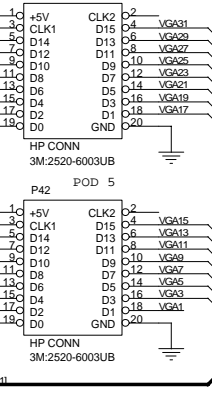
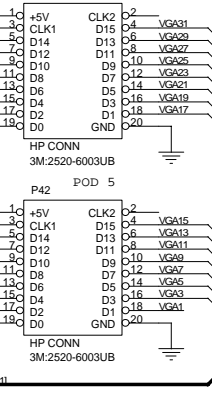
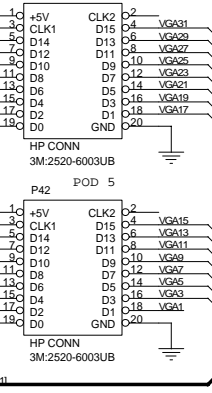
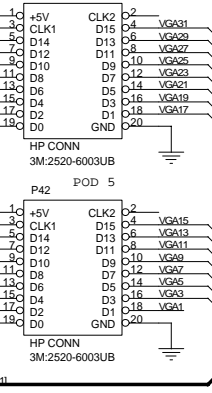
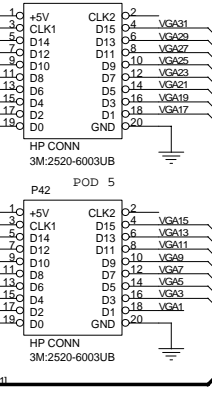
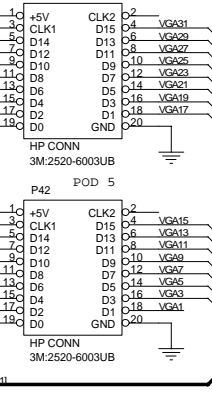
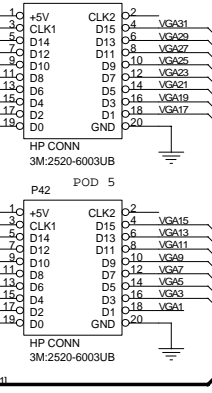
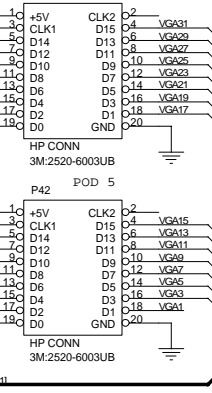
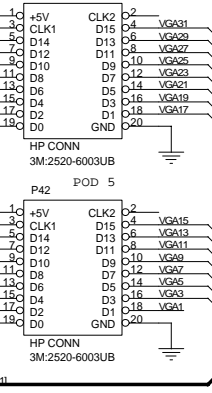
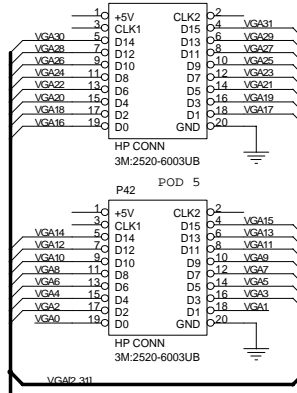
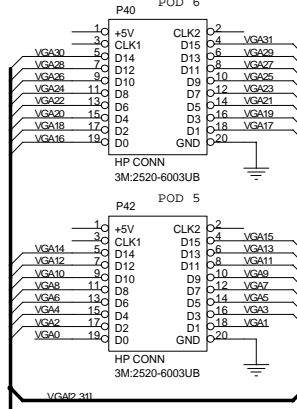
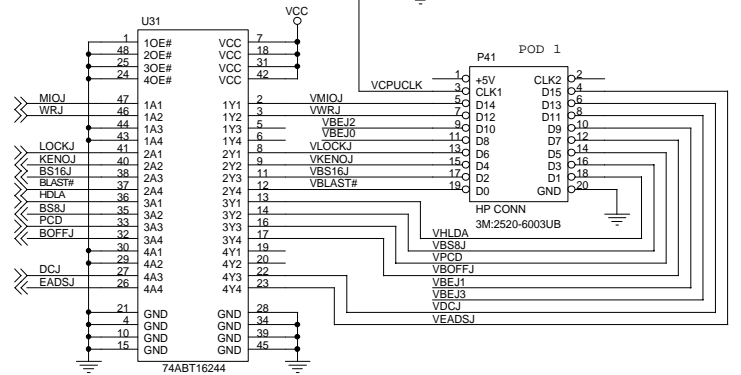
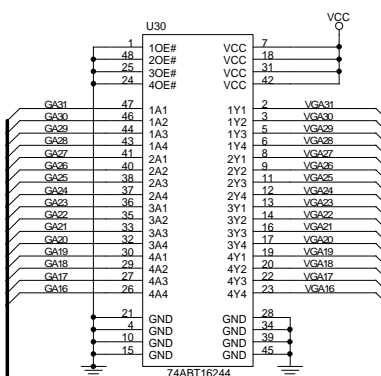
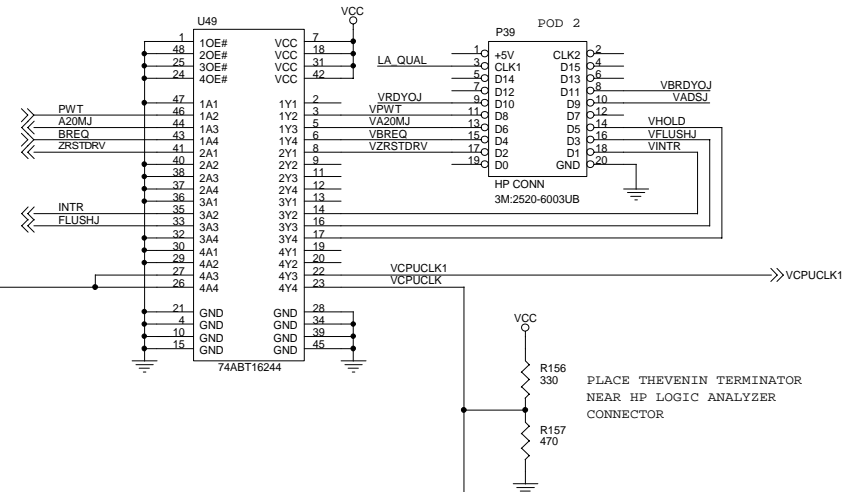
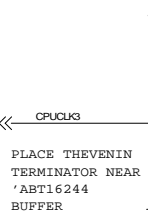
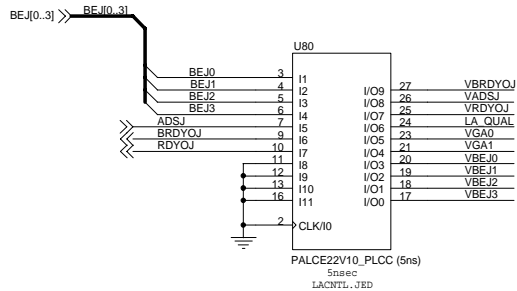
POWER CONNECTOR, CPU PULLUPS, CPU POWER SUPPLY, CPU BYPASS CAPACITORS



Power Connector(s)
● = Connector Polarizing Key

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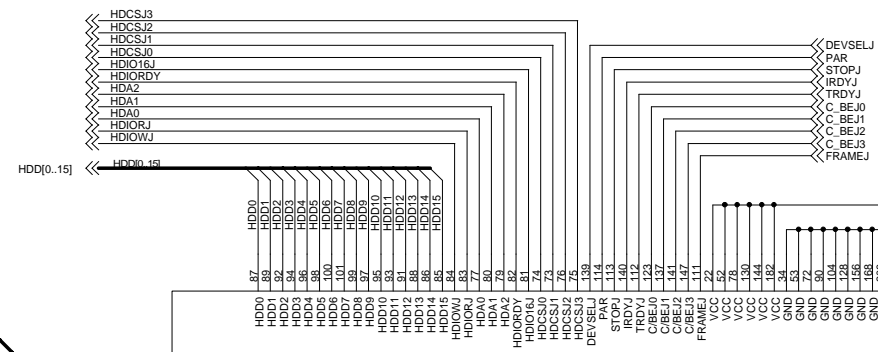
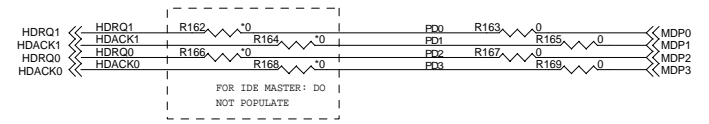
BUFFERS AND LOGIC ANALYZER HEADERS FOR CPU SIGNALS, AND PAL TO AID LOGIC ANALYZER USE



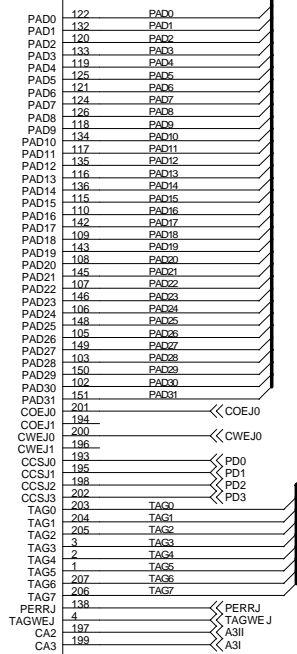
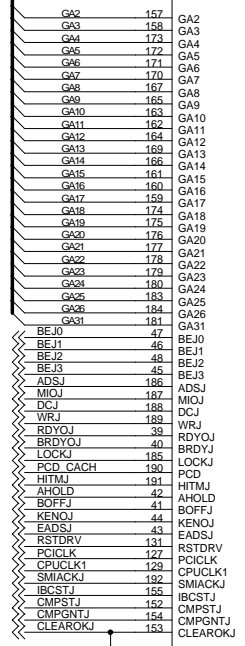
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Size		PCI CUSTOMER DEVELOPMENT PLATFORM	
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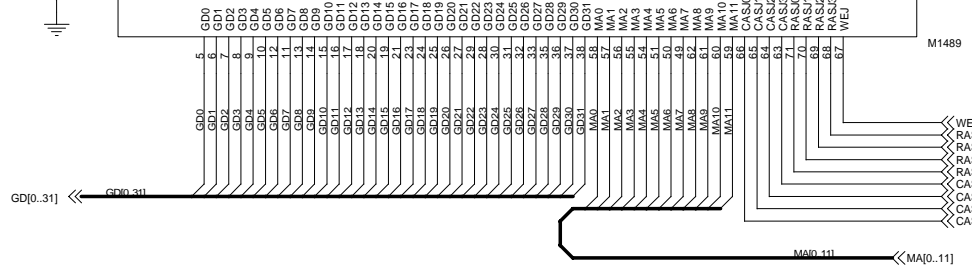
PARITY



GA[2..31] << GA[2..31]



R85 1K



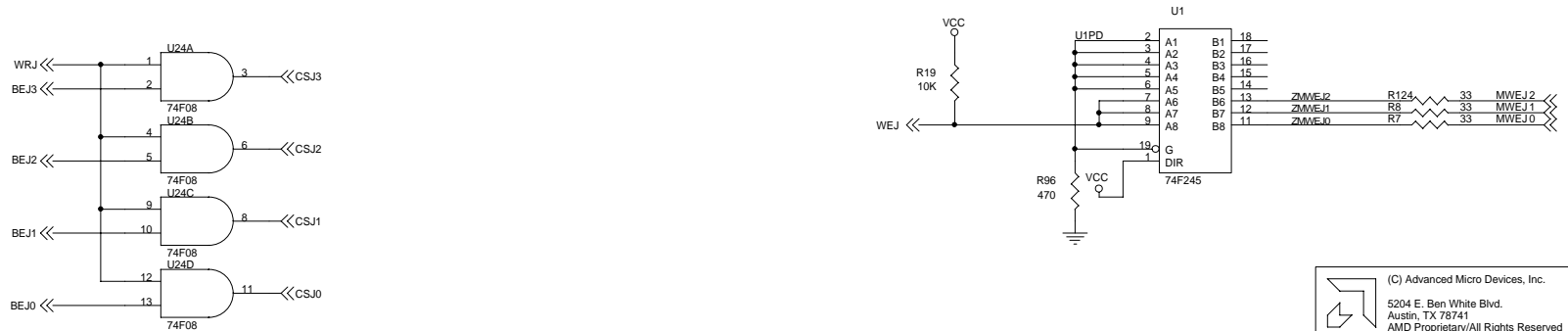
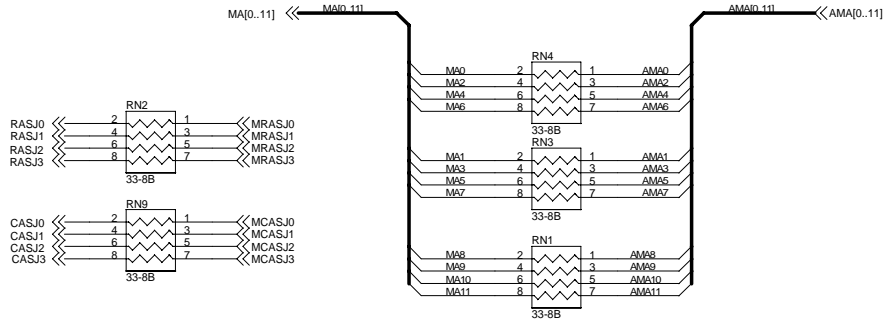
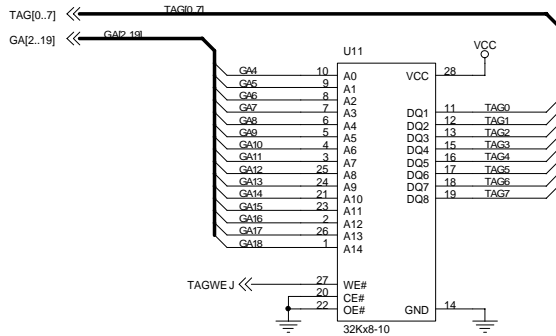
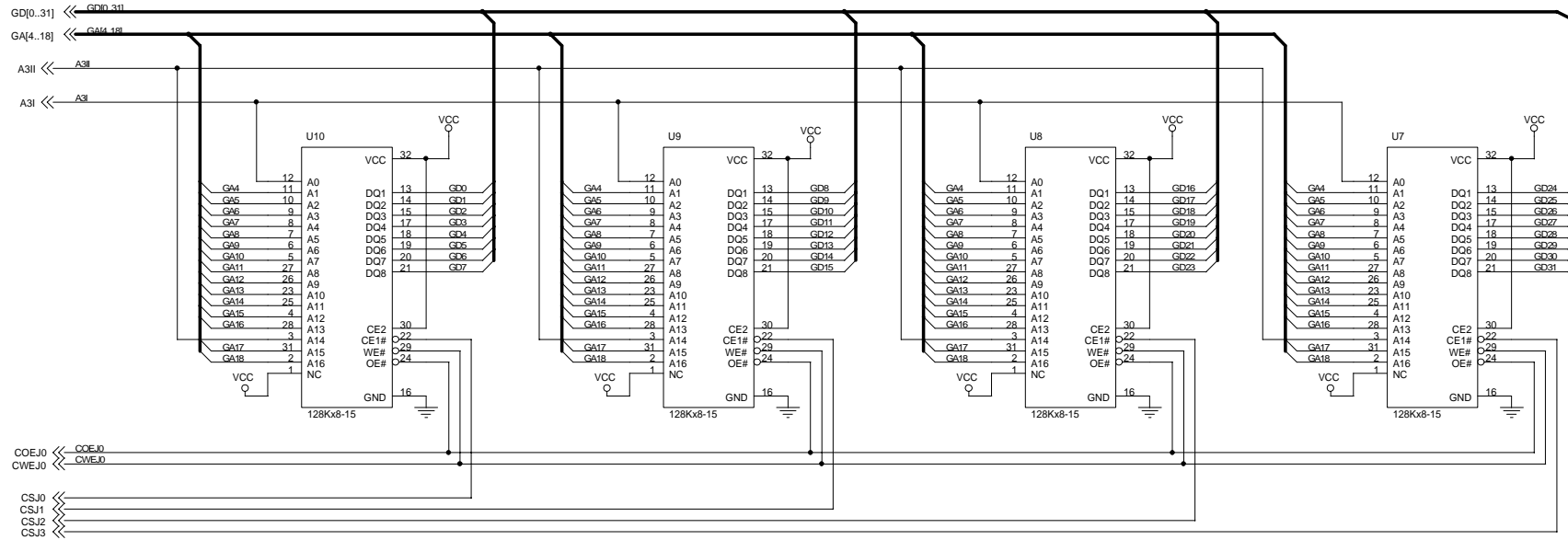
GD[0..31] << GD[0..31]

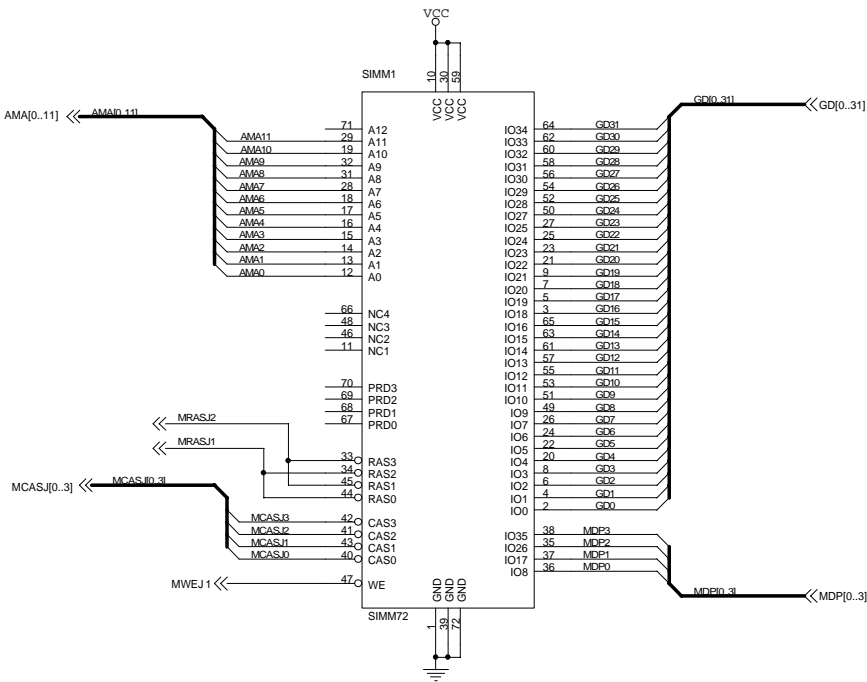
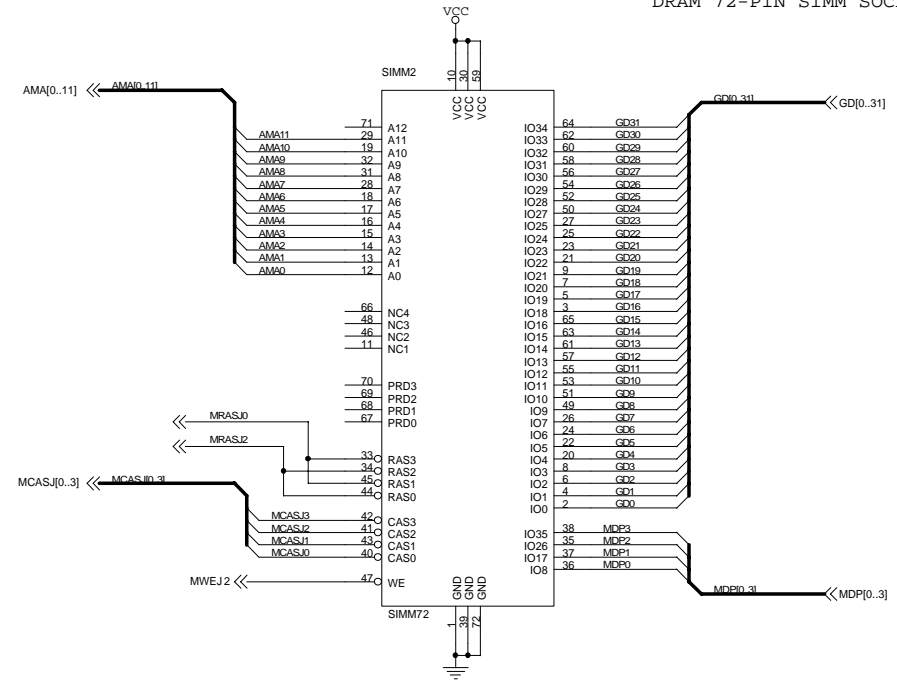
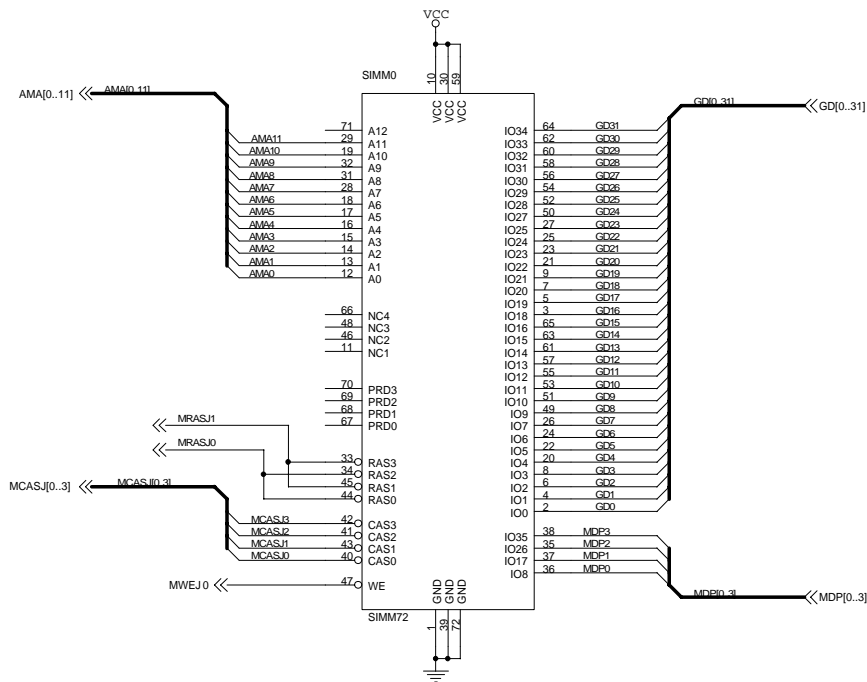
MA0..11 << MA[0..11]

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L2 CACHE TAG AND DATA SRAMS AND BYTE CONTROL; DRAM SERIES TERMINATION AND WE* FANOUT





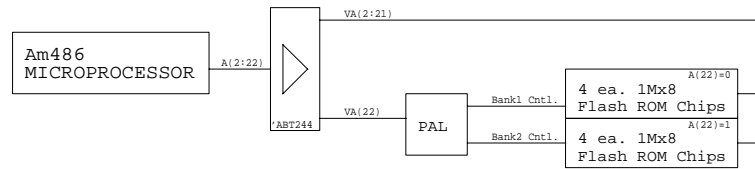
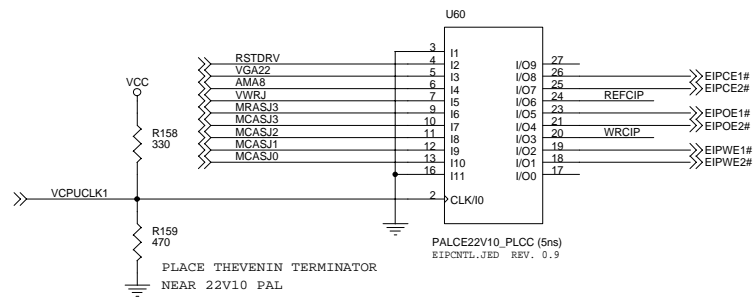
SIMM SOCKET POPULATION CHART

SIMM0	SIMM1	SIMM2
SINGLE BANK	SINGLE BANK	SINGLE BANK
DOUBLE BANK	SINGLE BANK	X

SIMMS CAN BE SINGLE BANK OR DOUBLE BANK, USING 1Mbit, 4Mbit, or 16Mbit DRAM CHIPS. POPULATE SIMM SOCKETS AS SHOWN IN THIS CHART.

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Title		Am486 MICROPROCESSOR	
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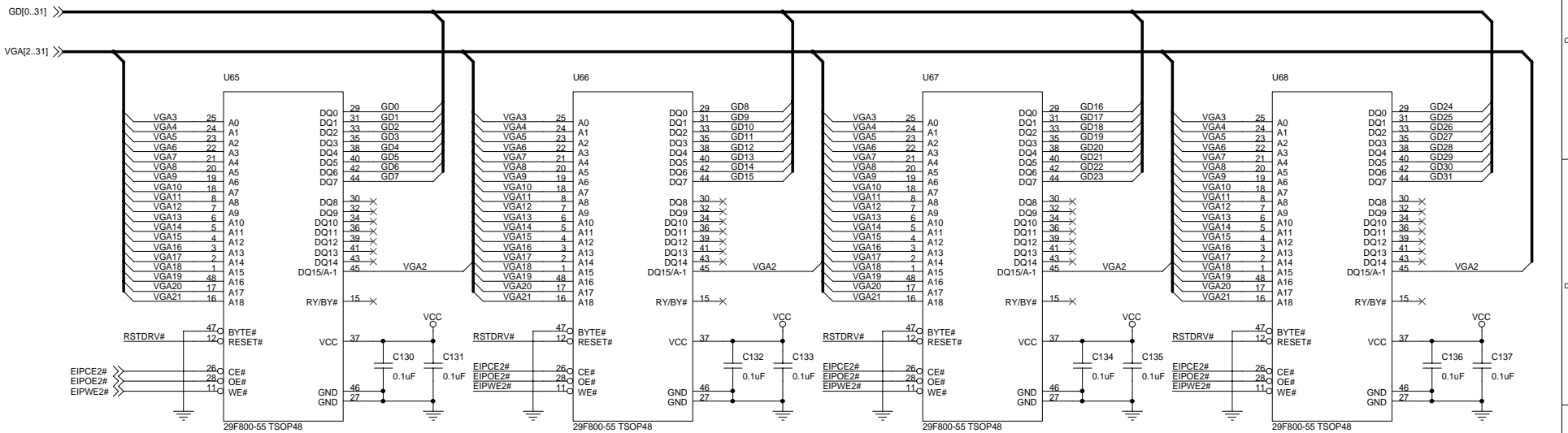
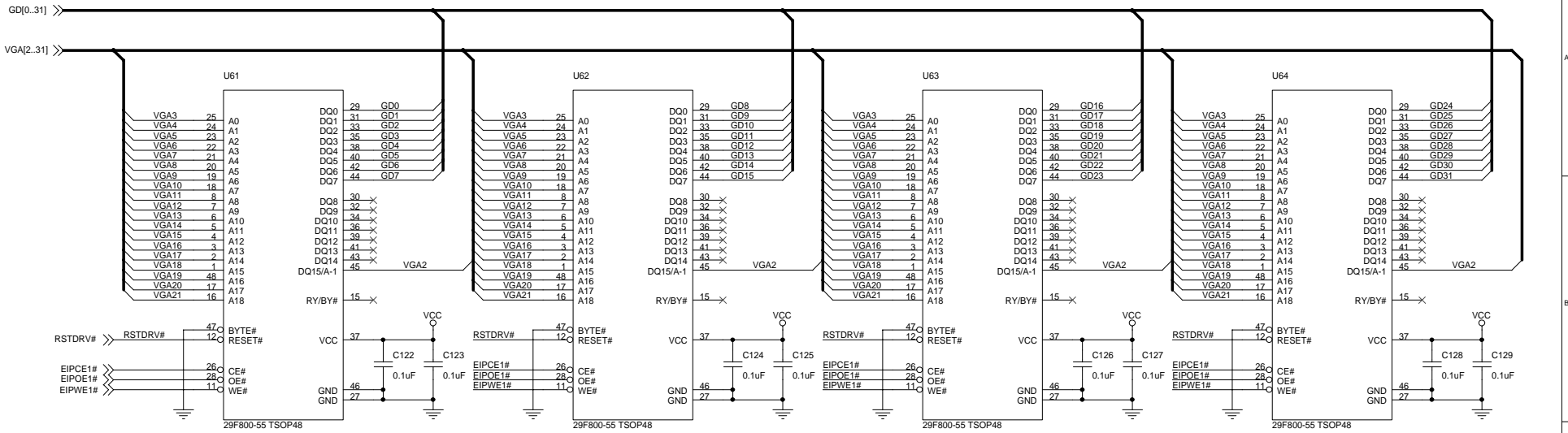


CPU Address Bit A(22) Used As Flash Bank Select

Makes 2 banks of 1Mx32 Flash ROM appear as 1 bank of 2Mx32 DRAM (70ns, FPM) to M1489 Memory Controller. Program M1489 for 2Mx8 (11/10) DRAM chips. MA8 (CPU A22) used as Flash ROM Bank Select when RAS3# asserted by M1489 Memory Controller.

Limitations and Operation of the EIP Interface:

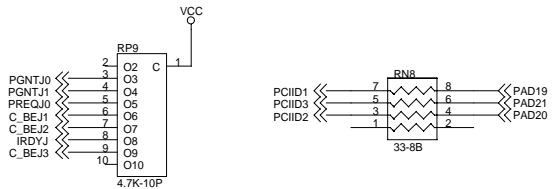
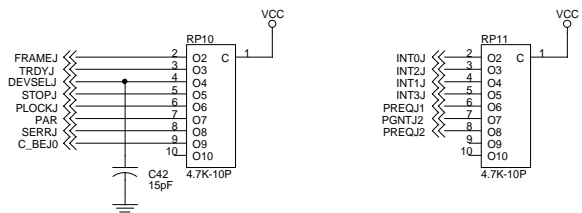
- Access as 32-bits wide always
- Supports burst Read Cycles or single-beat Read Cycles
- Supports single-beat Write Cycles only; no back-to-back Write Cycles
- Compatible with CAS-before-RAS Refresh Cycles only
- Set M1489 Memory Controller to "Fast" for proper operation, even if installed DRAM is 60ns and can run at the "Fastest" setting
- Flash chip A0 pin tied to Am486 Microprocessor A2 pin, so multiply desired Flash chip address by 4h to find Am486 Microprocessor address needed to access the desired memory cell (ex: Flash Chip AAAh accessed by Am486 Microprocessor at 2AA8h)
- EIP Flash Array start address moves, depending on how much DRAM is installed (ex: 48MByte DRAM puts EIP start address at 48MB or 3000000h for first bank of Flash ROMs and 3400000h start address for second bank of Flash ROMs)
- Uses 29F800T, 55ns devices in "Byte" mode
- Accessible from Am486 Microprocessor only; not accessible from PCI Bus Masters
- Uses fourth DRAM bank of M1489 Memory Controller



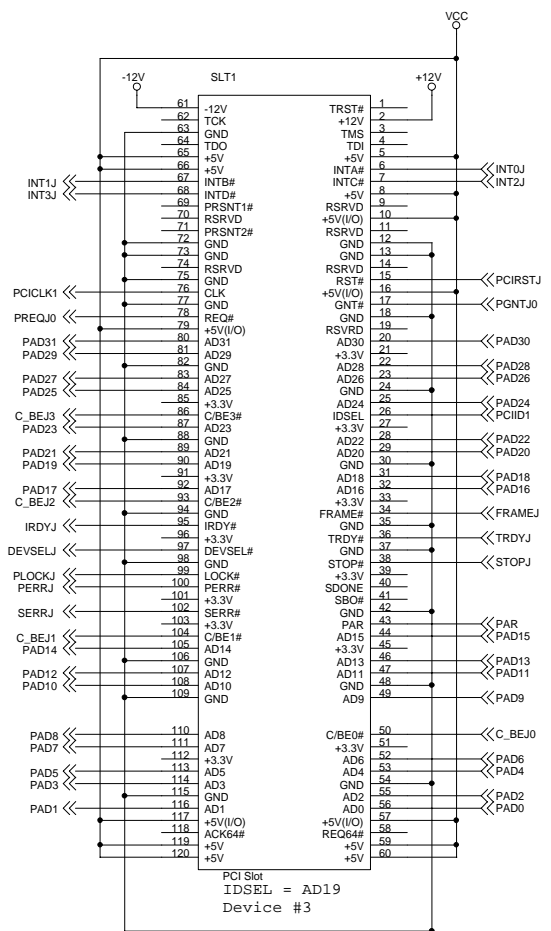
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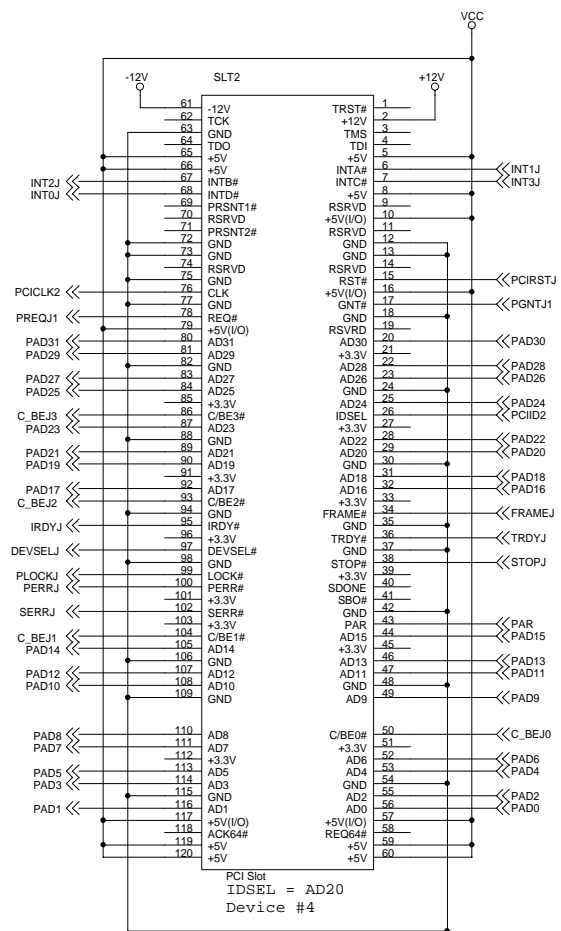
PCI PULLUPS AND SLOT CONNECTORS; PCI IDSEL GENERATION



PCIBus	INT	Slot1	Slot2	Ethernet
INT0#	INTA#	INTD#		
INT1#	INTB#	INTA#		
INT2#	INTC#	INTB#	INTA#	
INT3#	INTC#	INTC#		



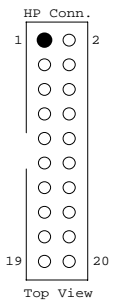
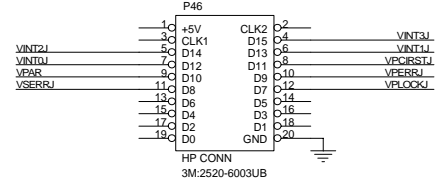
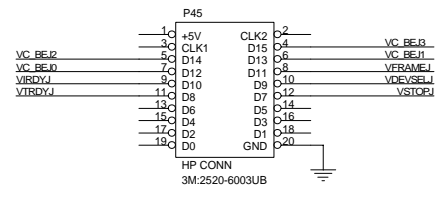
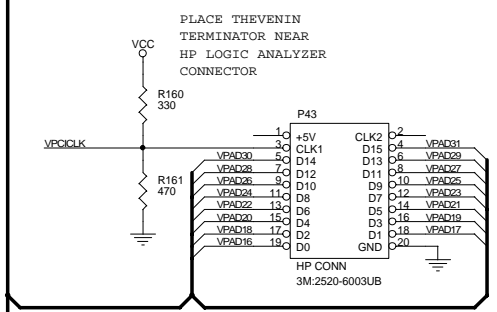
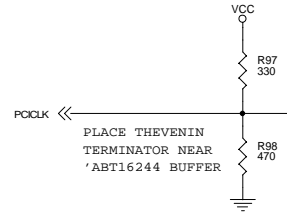
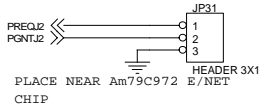
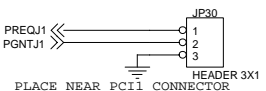
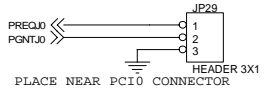
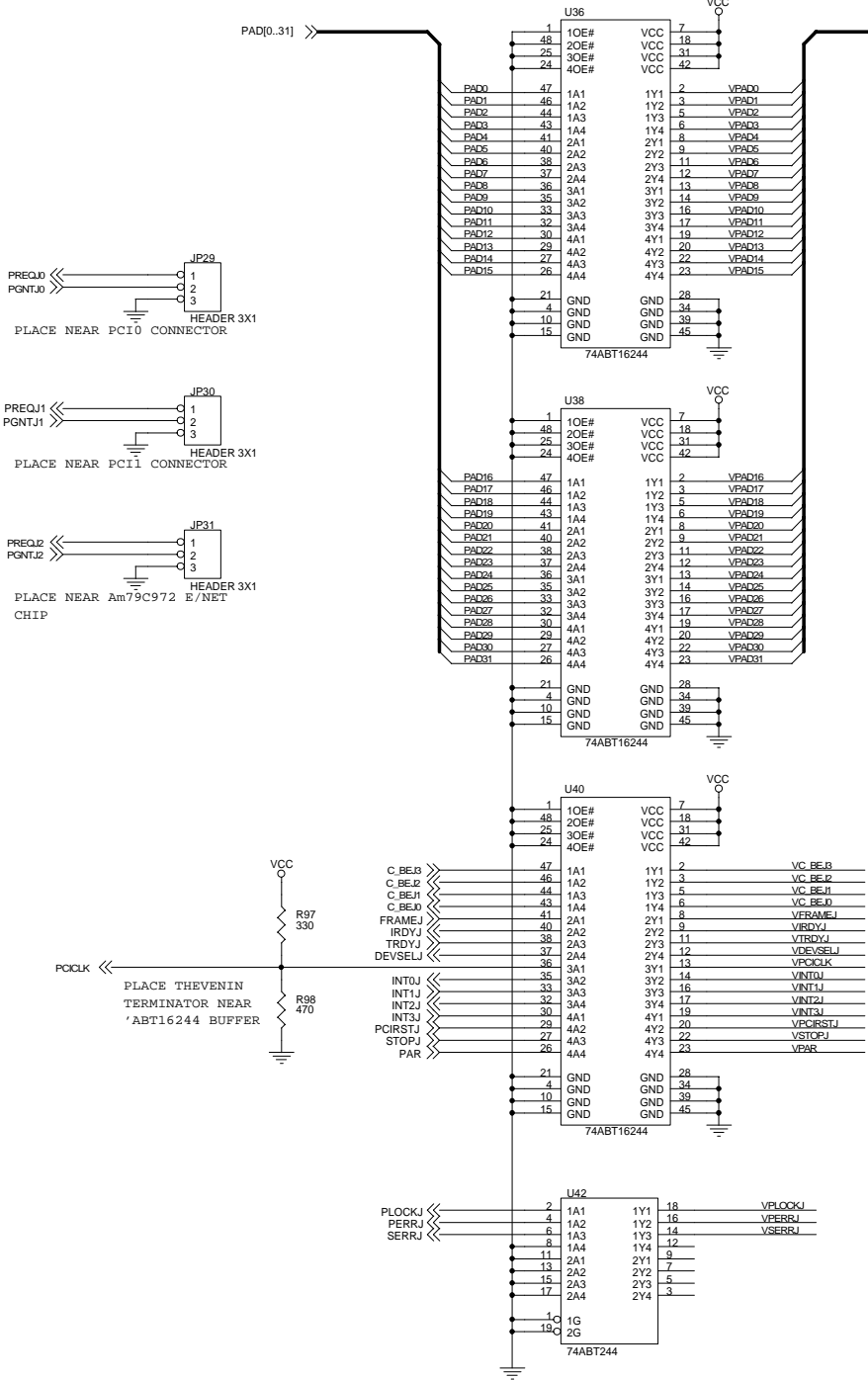
PCI Slot
IDSEL = AD19
Device #3



PCI Slot
IDSEL = AD20
Device #4

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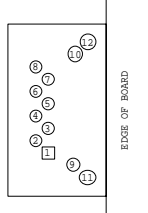
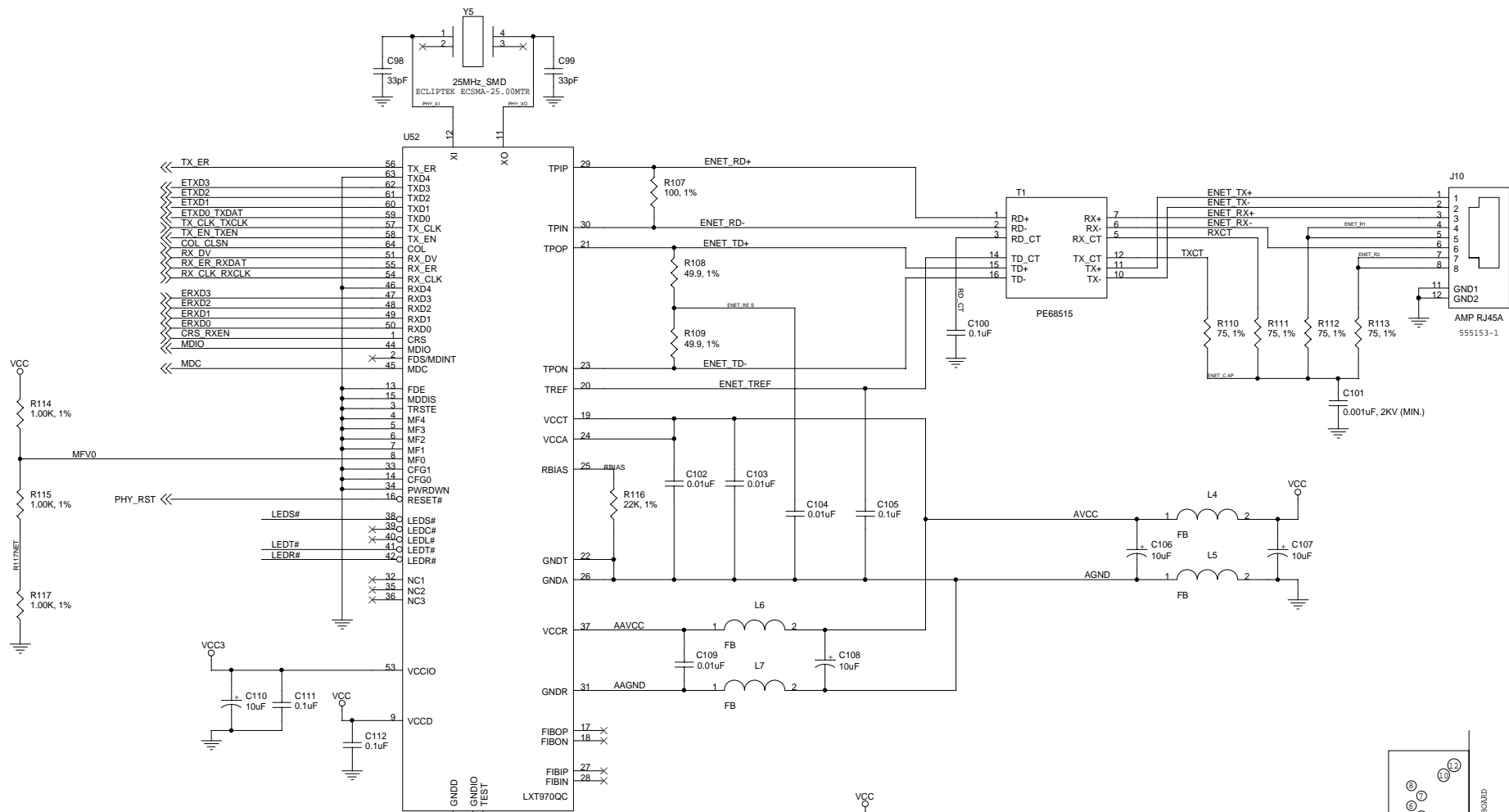
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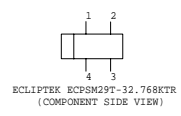
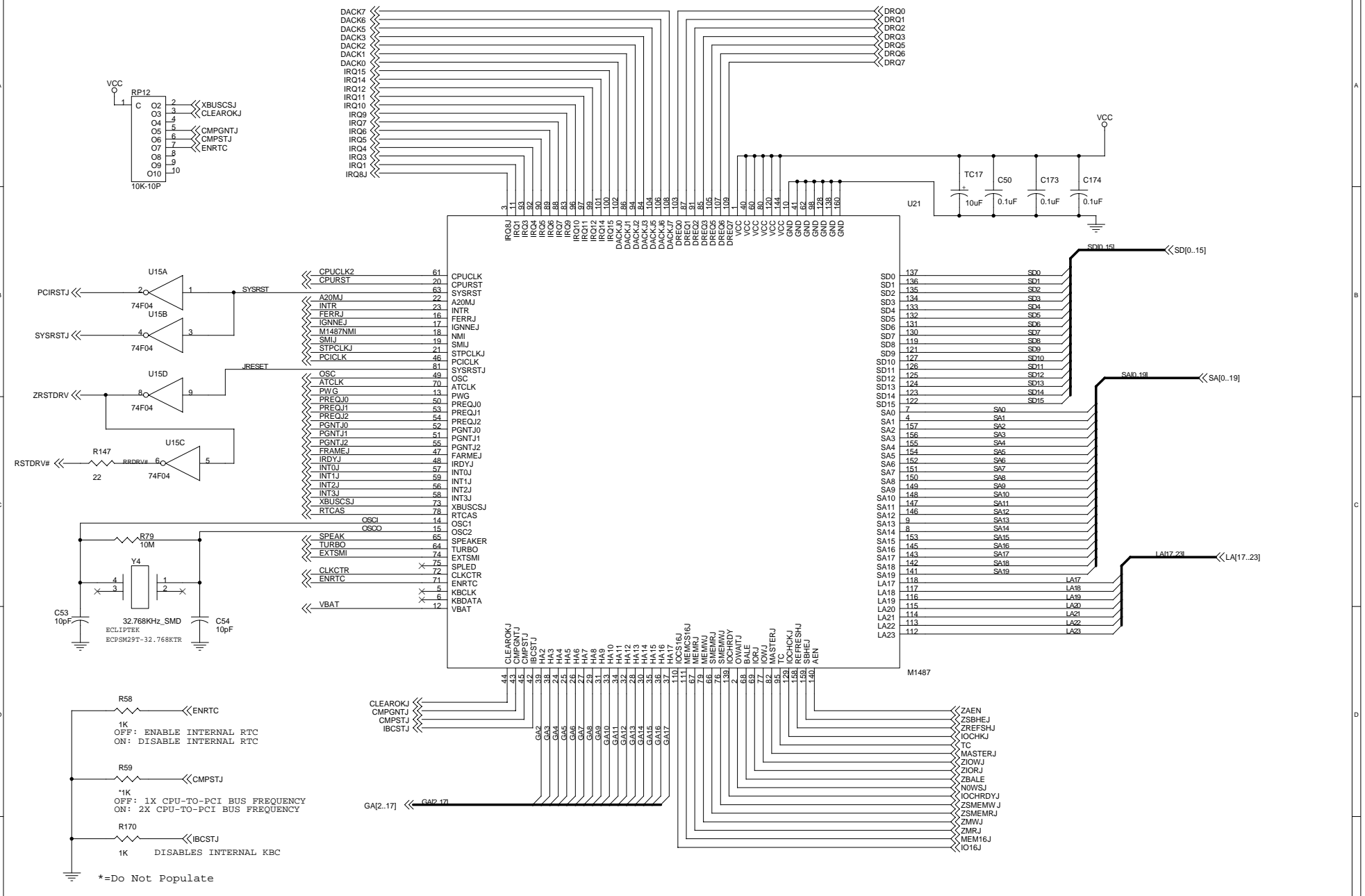
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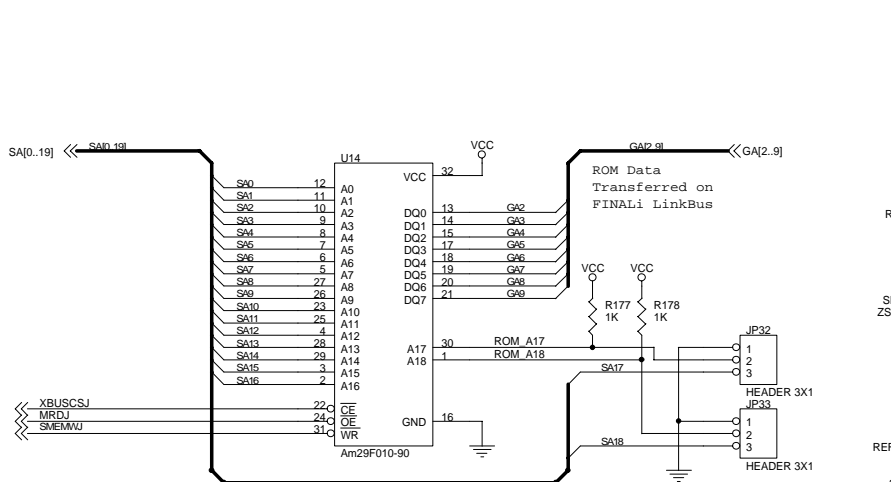
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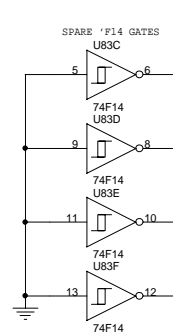
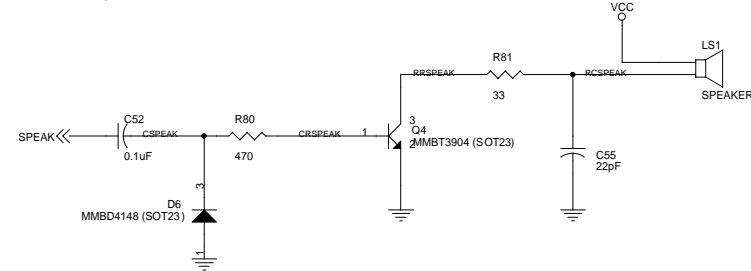
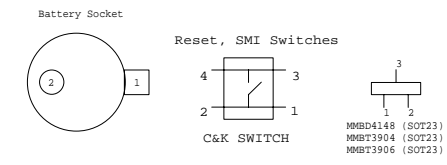
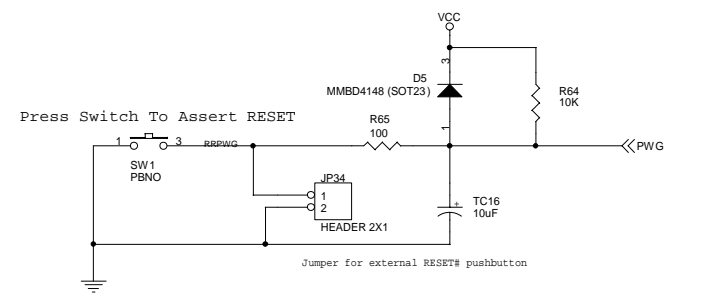
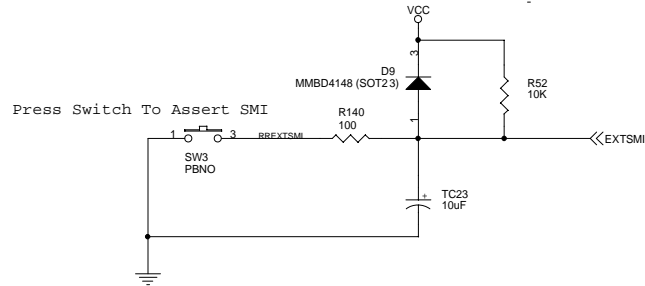
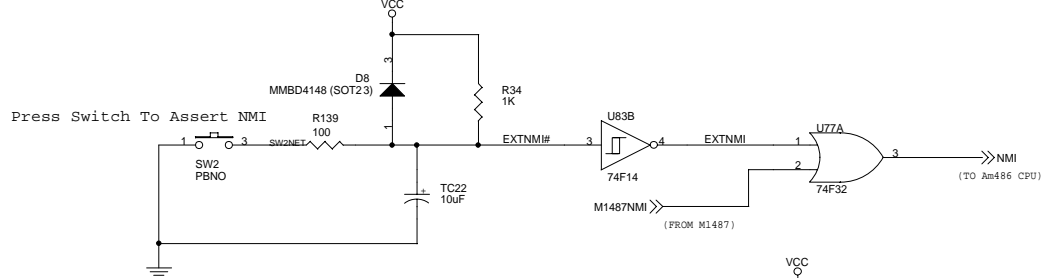
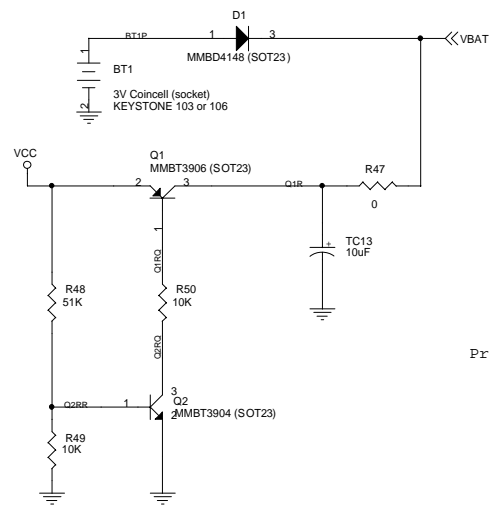
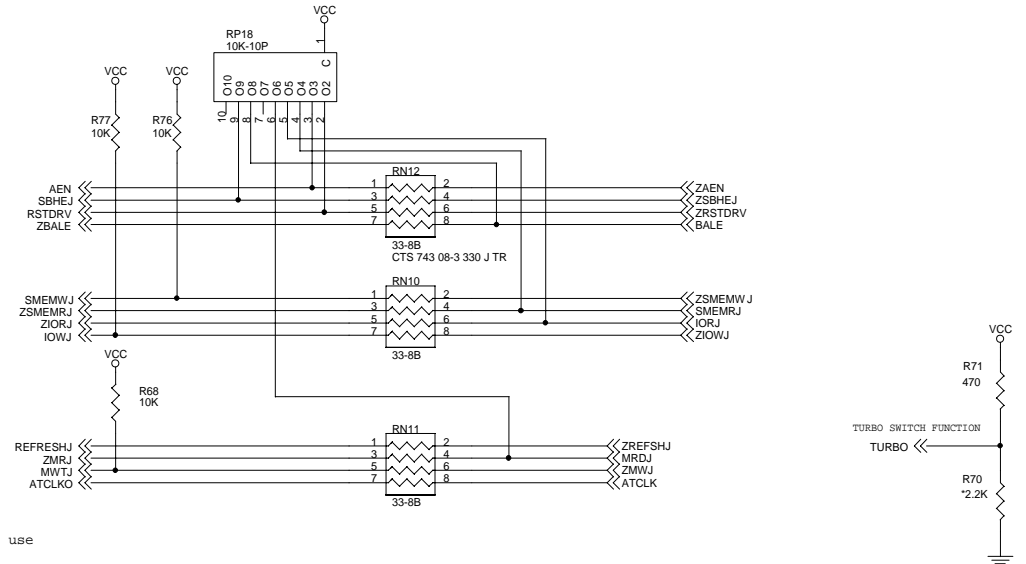
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BIOS ROM, ISA SIGNAL SERIES TERMINATION; BATTERY AND SPEAKER CIRCUITS; RESET, SMI, AND NMI PUSHBUTTONS



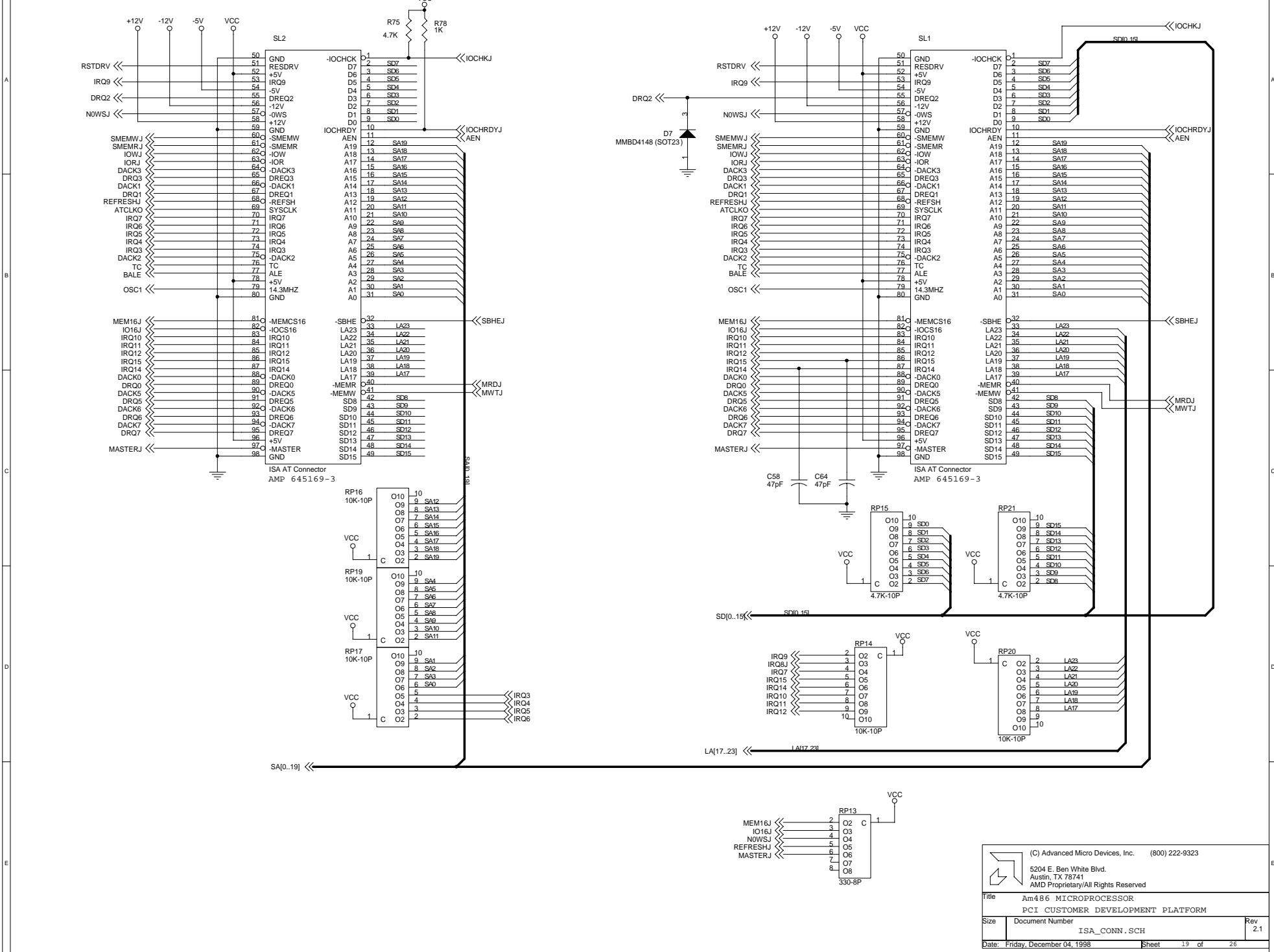
FINALi only supports 1Mbit Flash ROM chip (128Kx8 worth of address space) for legacy, desktop PC applications

Jumpers to allow multiple 128K BIOS images in the same Flash ROM chip and/or non-PC applications that can use more than 128Kx8 BIOS ROM



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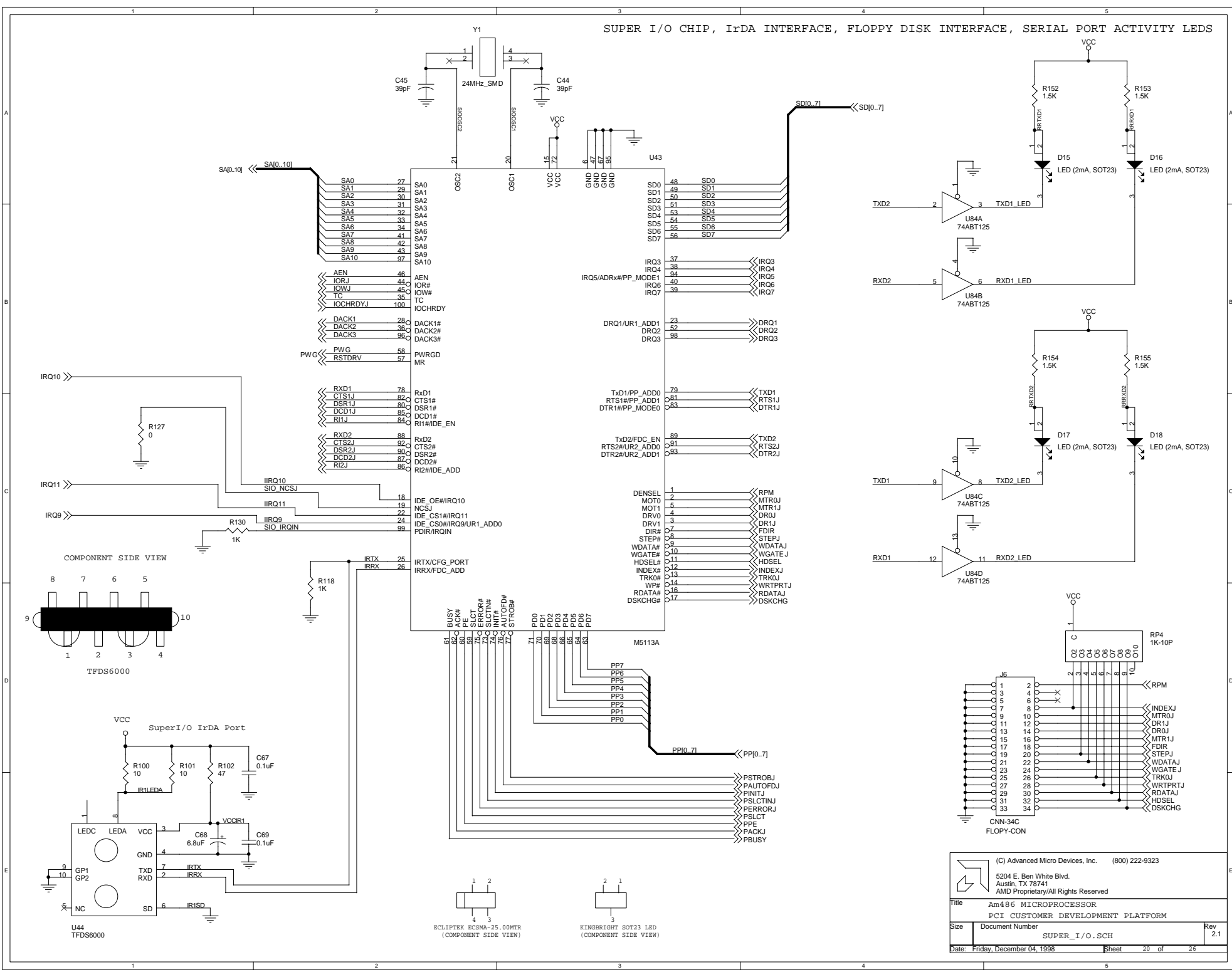
ISA BUS CONNECTORS AND PULLUPS



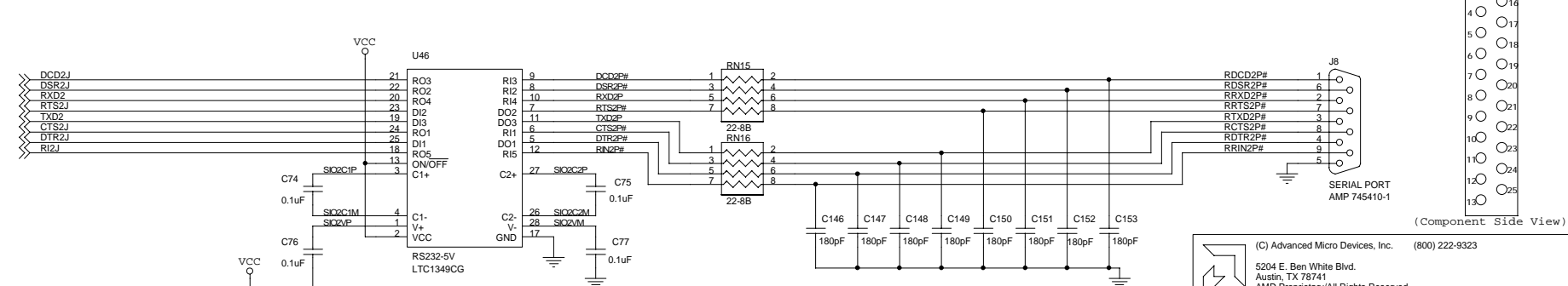
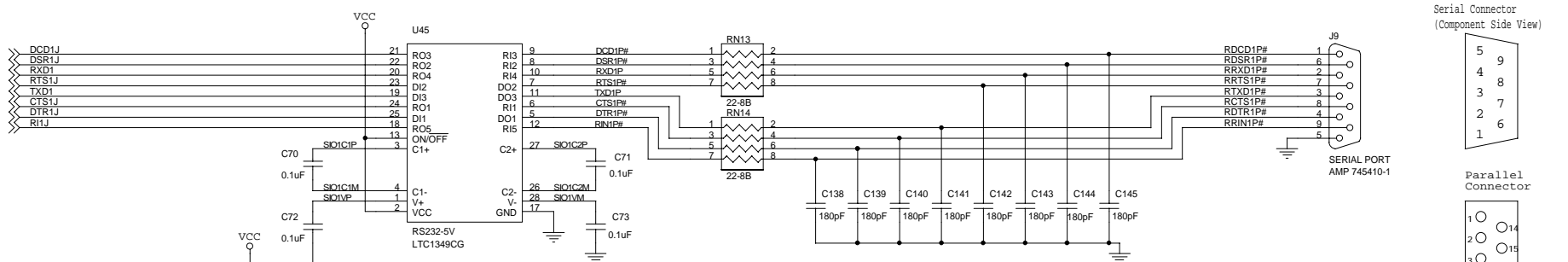
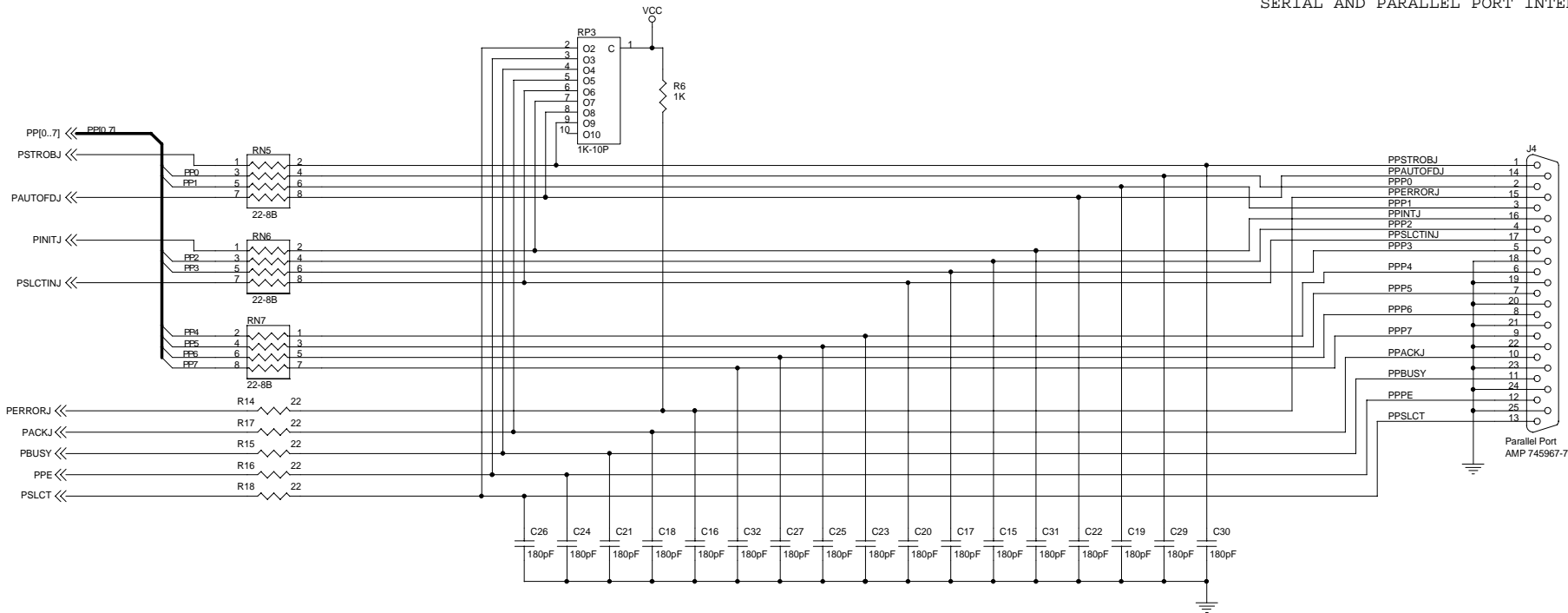
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SUPER I/O CHIP, IrDA INTERFACE, FLOPPY DISK INTERFACE, SERIAL PORT ACTIVITY LEADS



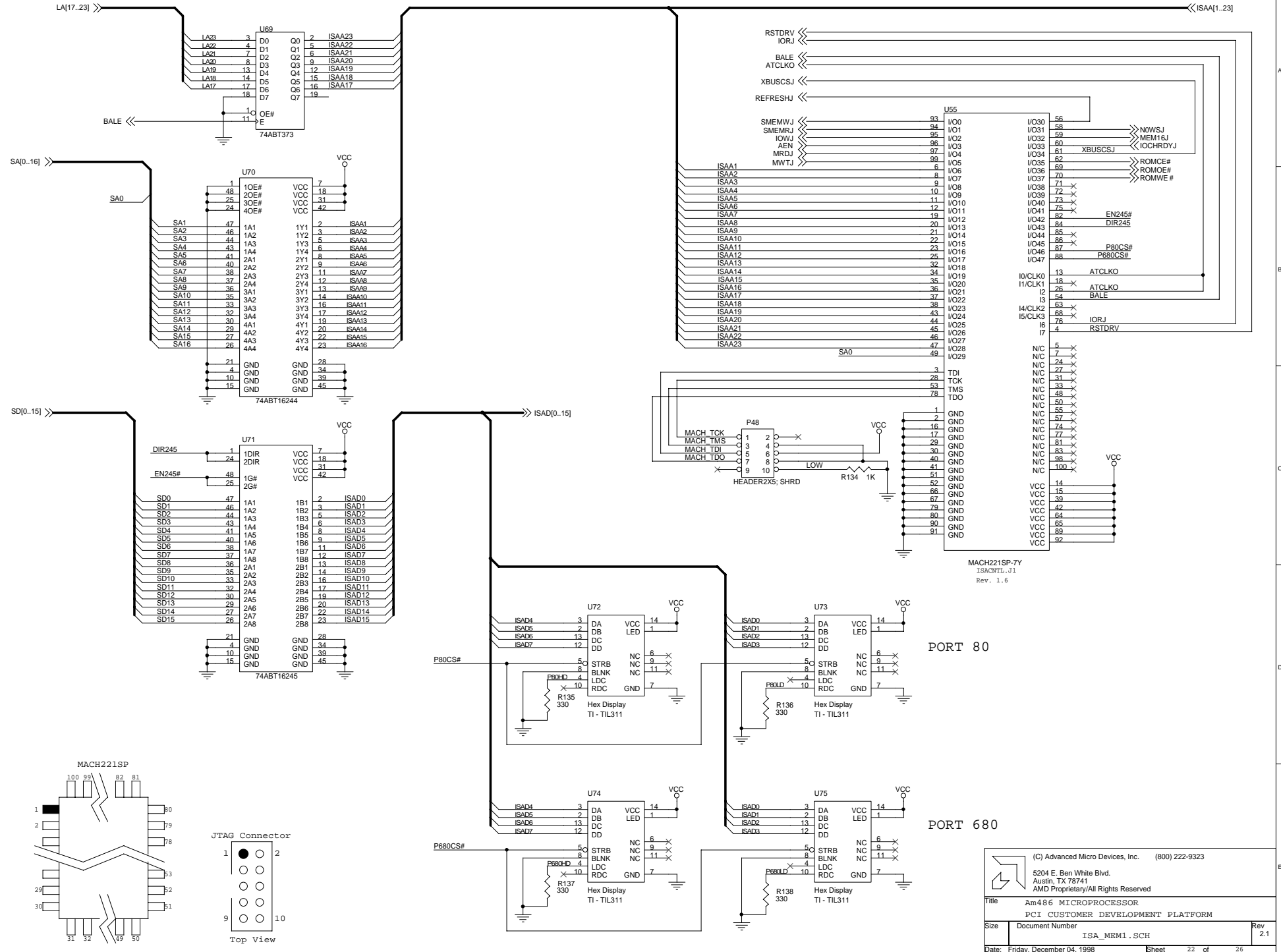
SERIAL AND PARALLEL PORT INTERFACES



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INTERFACE FOR ISA BUS MEMORY AND HEX DISPLAYS



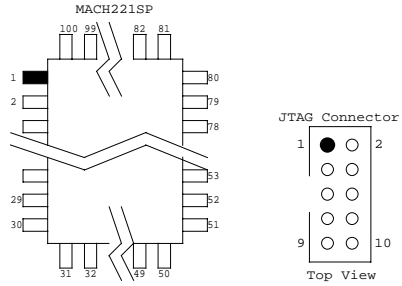
U55

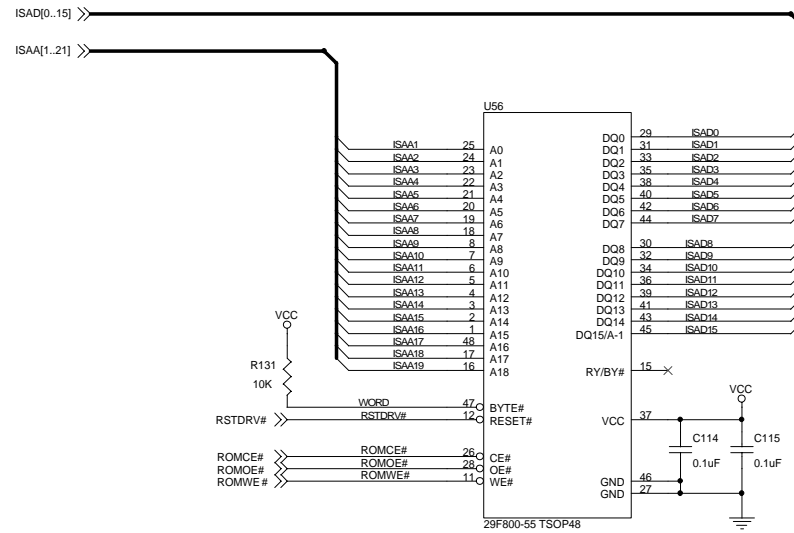
I/O30	93	I/O0	56
I/O31	94	I/O1	57
I/O32	95	I/O2	58
I/O33	96	I/O3	59
I/O34	97	I/O4	60
I/O35	98	I/O5	61
I/O36	99	I/O6	62
I/O37	100	I/O7	63
I/O38	101	I/O8	64
I/O39	102	I/O9	65
I/O40	103	I/O10	66
I/O41	104	I/O11	67
I/O42	105	I/O12	68
I/O43	106	I/O13	69
I/O44	107	I/O14	70
I/O45	108	I/O15	71
I/O46	109	I/O16	72
I/O47	110	I/O17	73
I/O48	111	I/O18	74
I/O49	112	I/O19	75
I/O50	113	I/O20	76
I/O51	114	I/O21	77
I/O52	115	I/O22	78
I/O53	116	I/O23	79
I/O54	117	I/O24	80
I/O55	118	I/O25	81
I/O56	119	I/O26	82
I/O57	120	I/O27	83
I/O58	121	I/O28	84
I/O59	122	I/O29	85
I/O60	123	I/O30	86
I/O61	124	I/O31	87
I/O62	125	I/O32	88
I/O63	126	I/O33	89
I/O64	127	I/O34	90
I/O65	128	I/O35	91
I/O66	129	I/O36	92
I/O67	130	I/O37	93
I/O68	131	I/O38	94
I/O69	132	I/O39	95
I/O70	133	I/O40	96
I/O71	134	I/O41	97
I/O72	135	I/O42	98
I/O73	136	I/O43	99
I/O74	137	I/O44	100
I/O75	138	I/O45	101
I/O76	139	I/O46	102
I/O77	140	I/O47	103
I/O78	141	I/O48	104
I/O79	142	I/O49	105
I/O80	143	I/O50	106
I/O81	144	I/O51	107
I/O82	145	I/O52	108
I/O83	146	I/O53	109
I/O84	147	I/O54	110
I/O85	148	I/O55	111
I/O86	149	I/O56	112
I/O87	150	I/O57	113
I/O88	151	I/O58	114
I/O89	152	I/O59	115
I/O90	153	I/O60	116
I/O91	154	I/O61	117
I/O92	155	I/O62	118
I/O93	156	I/O63	119
I/O94	157	I/O64	120
I/O95	158	I/O65	121
I/O96	159	I/O66	122
I/O97	160	I/O67	123
I/O98	161	I/O68	124
I/O99	162	I/O69	125
I/O100	163	I/O70	126
I/O101	164	I/O71	127
I/O102	165	I/O72	128
I/O103	166	I/O73	129
I/O104	167	I/O74	130
I/O105	168	I/O75	131
I/O106	169	I/O76	132
I/O107	170	I/O77	133
I/O108	171	I/O78	134
I/O109	172	I/O79	135
I/O110	173	I/O80	136
I/O111	174	I/O81	137
I/O112	175	I/O82	138
I/O113	176	I/O83	139
I/O114	177	I/O84	140
I/O115	178	I/O85	141
I/O116	179	I/O86	142
I/O117	180	I/O87	143
I/O118	181	I/O88	144
I/O119	182	I/O89	145
I/O120	183	I/O90	146
I/O121	184	I/O91	147
I/O122	185	I/O92	148
I/O123	186	I/O93	149
I/O124	187	I/O94	150
I/O125	188	I/O95	151
I/O126	189	I/O96	152
I/O127	190	I/O97	153
I/O128	191	I/O98	154
I/O129	192	I/O99	155
I/O130	193	I/O100	156

MACH221SP-7Y
ISACNTL.J1
Rev. 1.6

PORT 80

PORT 680





1MByte ISA Flash Memory

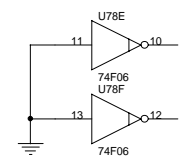
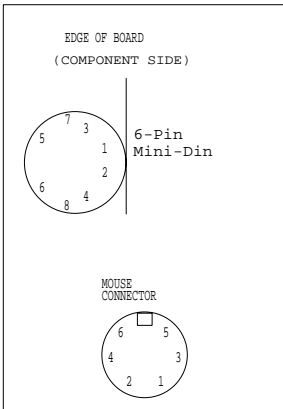
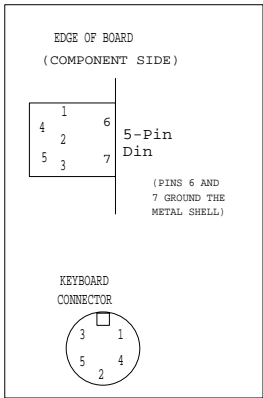
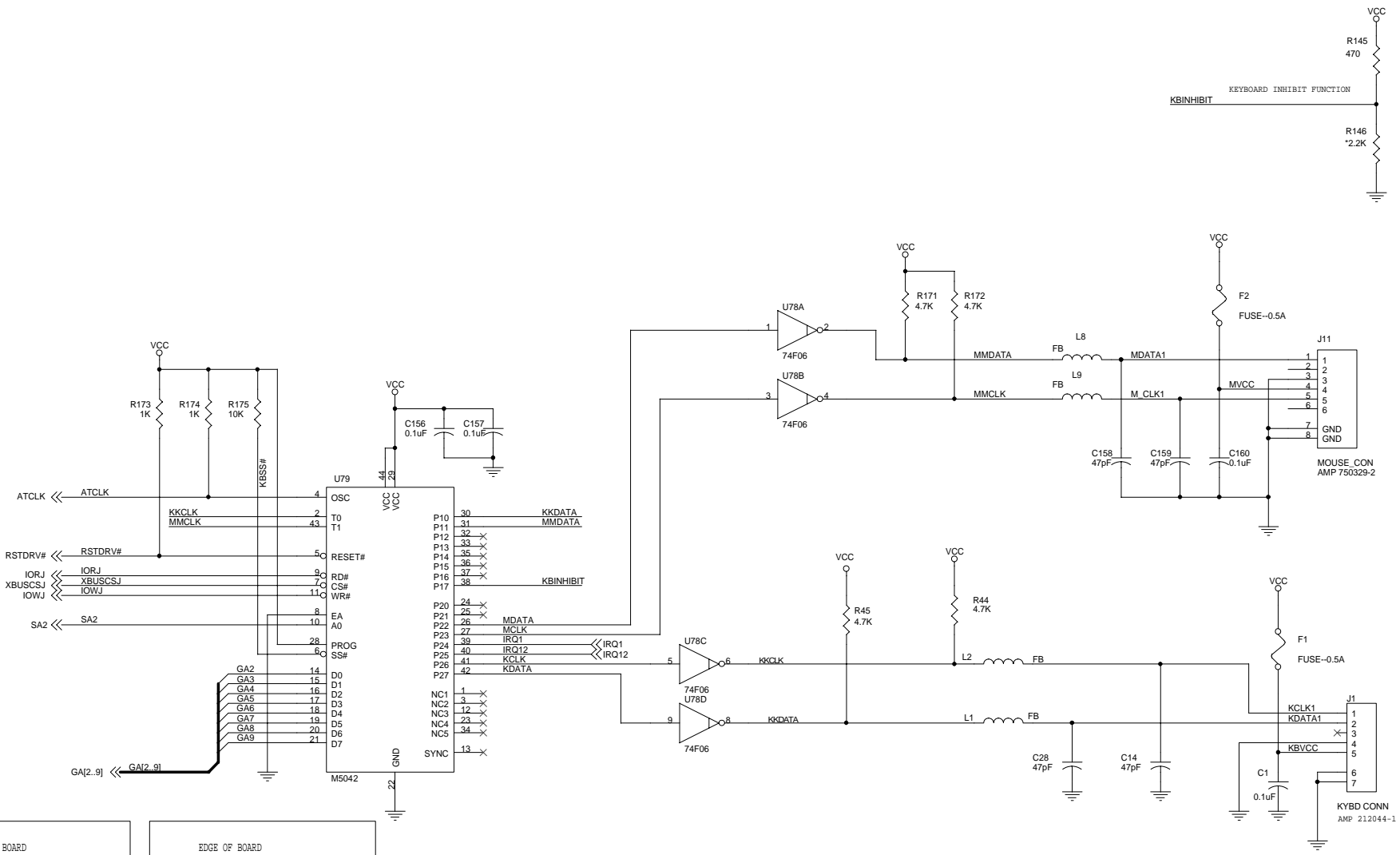
Configured as 512Kx16bit (29F800T device in "word" mode)

Access at even ISA Memory addresses between 15MB and 16MB-1

Use CSR 12h bit 3 to access 0f00000-0fffffh as ISA Memory (instead of DRAM, if installed)

Flash chip A0 pin tied to ISA Address Bit 1; multiply desired
Flash chip address by 2h to find correct ISA address for access
(ex: Flash chip address 555h is accessed at ISA address AAAh)

PC KEYBOARD AND MOUSE INTERFACE

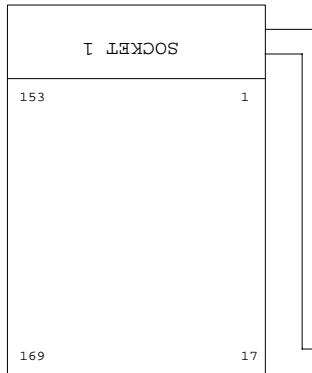


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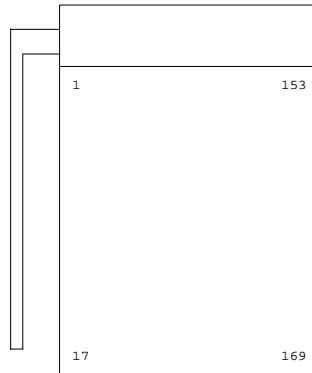
Title		Am486 MICROPROCESSOR	
Size		Document Number	
Date:		KEYBOARD .SCH	
Rev		2.1	
Date: Friday, December 04, 1998		Sheet 25 of 26	

SOCKET1
Am486 MICROPROCESSOR
(PIN #)-PIN DESIGNATION
(PIN SIDE VIEW)


(1)-D20	(18)-D19	(35)-D11	(52)-D9	(59)-GND	(65)-DP1	(71)-GND	(77)-GND	(83)-INC	(89)-GND	(95)-GND	(101)-GND	(107)-D2	(113)-D0	(119)-A31	(136)-A28	(153)-A27										
(2)-D22	(19)-D21	(36)-D18	(53)-D13	(60)-VCC	(66)-D8	(72)-VCC	(78)-D3	(84)-D5	(90)-VCC	(96)-D6	(102)-VCC	(108)-D1	(114)-A29	(120)-GND	(137)-A25	(154)-A26										
(3)-TCK	(20)-GND	(37)-CLK	(54)-D17	(61)-D10	(67)-D15	(73)-D12	(79)-DP2	(85)-D16	(91)-D14	(97)-D7	(103)-D4	(109)-DP0	(115)-A30	(121)-A17	(138)-VCC	(155)-A23										
(4)-D23	(21)-GND	(38)-VCC	(55)-SKT1_NC	Am486 MICROPROCESSOR PIN SIDE VIEW										(122)-A19	(139)-GND	(156)-VOLDET										
(5)-DP3	(22)-GND	(39)-VCC												(123)-A21	(140)-A18	(157)-A14										
(6)-D24	(23)-D25	(40)-D27												(124)-A24	(141)-VCC	(158)-GND										
(7)-GND	(24)-VCC	(41)-D26												(125)-A22	(142)-A15	(159)-A12										
(8)-D29	(25)-D31	(42)-D28												(126)-A20	(143)-VCC	(160)-GND										
(9)-GND	(26)-VCC	(43)-D30												(127)-A16	(144)-VCC	(161)-GND										
(10)-INV	(27)-SMI#	(44)-SRESET												(128)-A13	(145)-VCC	(162)-GND										
(11)-GND	(28)-VCC	(45)-UP#												(129)-A9	(146)-VCC	(163)-GND										
(12)-HITM#	(29)-CACHE#	(46)-SMIACT#												(130)-A5	(147)-A11	(164)-GND										
(13)-INC	(30)-WB/WT#	(47)-INC												(131)-A7	(148)-A8	(165)-A10										
(14)-TDI	(31)-TMS	(48)-FERR#												(132)-A2	(149)-VCC	(166)-GND										
(15)-IGNEE#	(32)-NMI	(49)-FLUSH#	(56)-A20M#											(62)-HOLD	(68)-KEN#	(74)-STPCLK#	(80)-BRDY#	(86)-BE2#	(92)-BE0#	(98)-PWT	(104)-D/C#	(110)-LOCK#	(116)-HLDA	(133)-BREQ	(150)-A3	(167)-A6
(16)-INTR	(33)-TDO	(50)-RESET	(57)-BS8#											(63)-VCC	(69)-RDY#	(75)-VCC	(81)-VCC	(87)-BE1#	(93)-VCC	(99)-VCC	(105)-VCC	(111)-M/IO#	(117)-VCC	(134)-PLOCK#	(151)-BLAST#	(168)-A4
(17)-AHOLD	(34)-EADS#	(51)-BS16#	(58)-BOFF#											(64)-GND	(70)-BE3#	(76)-GND	(82)-GND	(88)-PCD	(94)-GND	(100)-GND	(106)-GND	(112)-W/R#	(118)-GND	(135)-PCHK#	(152)-CLKMUL	(169)-ADS#



COMPONENT SIDE VIEW



SOLDER SIDE VIEW

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