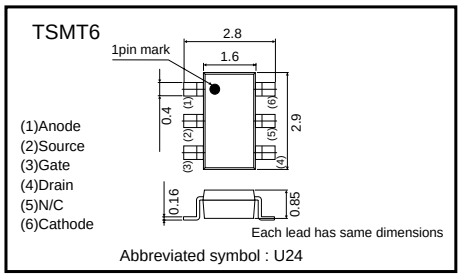
Small switching (–30V, –1A)

QS6U24

●Features

1) The QS6U24 conbines Pch Treueh MOSFET with a Schottky barrier diode in a single TSMT6 package.
2) Pch Treueh MOSFET have a low on-state resisternce with a fast switching.
3) Pch Treueh MOSFET is neucted a low voltage drive (4V).
4) The independently connected Schottky barrier diode have a low forward voltage.

●External dimensions (Units : mm)



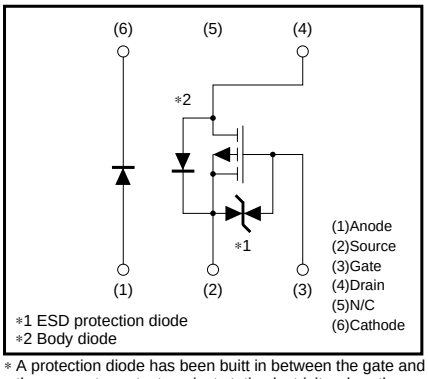
●Applications

load switch, DC/DC conversion

●Structure

Silicon P-channel MOS FET
Schottky Barrier DIODE

●Equivalent circuit



∗ A protection diode has been buitt in between the gate and the source to protect against static electricity when the product is in use. Use the protection circuit when rated voltages are exceeded.

●Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
QS6U24		○

●Absolute maximum ratings (Ta=25°C)

<MOSFET>

Parameter		Symbol	Limits	Unit
Drain-source voltage		V_{DSS}	–30	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	Continuous	I_D	±1.0	A
	Pulsed	I_{DP}	±2.0	A ∗1
Source current (Body diode)	Continuous	I_S	–0.3	A
	Pulsed	I_{SP}	–1.2	A ∗1
Channel temperature		Tch	150	°C

<Di>

Parameter	Symbol	Limits	Unit
Repetitive peak reverse voltage	V_{RM}	25	V
Reverse voltage	V_R	20	V
Forward current	I_F	0.7	A
Forward current surge peak	I_{FSM}	3.0	A ∗2
Junction temperature	Tj	125	°C

<MOSFET AND Di>

Parameter	Symbol	Limits	Unit
Total power dissipatino	P_D	1.0	W/Total ∗3
Range of strage temperature	Tstg	–40~+125	°C

∗1 Pw≤10μs, Duty cycle≤1% ∗2 60Hz・1cyc. ∗3 Total mounted on a ceramic board

●Electrical characteristics (Ta=25°C)

<MOSFET>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	–	–	±10	μA	V_{GS}=±20V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)\ DSS}$	−30	–	–	V	I_D=−1mA, V_{GS}=0V
Zero gate voltage drain current	I_{DSS}	–	–	−1	μA	V_{DS}=−30V, V_{GS}=0V
Gate threshold voltage	$V_{GS\ (th)}$	−1.0	–	−2.5	V	V_{DS}=−10V, I_D=−1mA
Static drain-source on-starte resistance	$R_{DS\ (on)}$	–	300	400	mΩ	I_D=−1A, V_{GS}=−10V
		–	500	700	mΩ	I_D=−0.5A, V_{GS}=−4.5V *
		–	600	800	mΩ	I_D=−0.5A, V_{GS}=−4V
Forward transfer admittance	$\|Y_{fs}\|$	0.5	–	–	S	V_{DS}=−10V, I_D=−0.5A *
Input capacitance	C_{iss}	–	90	–	pF	V_{DS}=−10V
Output capacitance	C_{oss}	–	25	–	pF	V_{GS}=0V
Reverse transfer capacitance	C_{rss}	–	16	–	pF	f=1MHz
Turn-on delay time	$t_{d\ (on)}$	–	9	–	ns	I_D=−0.5A * V_{DD}≒−15V * V_{GS}=−10V * R_L=30Ω * R_{GS}=10Ω
Rise time	t_r	–	7	–	ns	
Turn-off delay time	$t_{d\ (off)}$	–	18	–	ns	
Fall time	t_f	–	7	–	ns	
Total gate charge	Q_g	–	1.7	–	nC	V_{DD}≒−15V
Gate-source charge	Q_{gs}	–	0.6	–	nC	V_{GS}=−5V
Gate-drain charge	Q_{gd}	–	0.4	–	nC	I_D=−1.0A

* Pulsed

●Body diode (Source-drain)

<MOSFET>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD}	–	–	−1.2	V	I_S=−0.3A, V_{GS}=0V

<Di>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage drop	V_F	–	–	0.49	V	I_F=0.7A
Reverse leakage	I_R	–	–	200	μA	V_R=20V

●Electrical characteristic curves

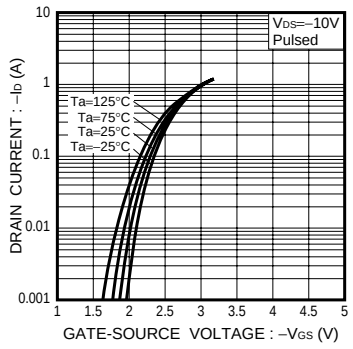


Fig.1 Typical Transfer Characteristics

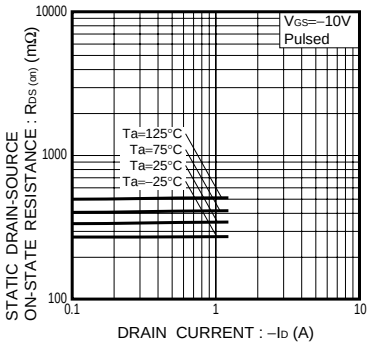


Fig.2 Static Drain-Source On-State Resistance vs. Drain Current (I)

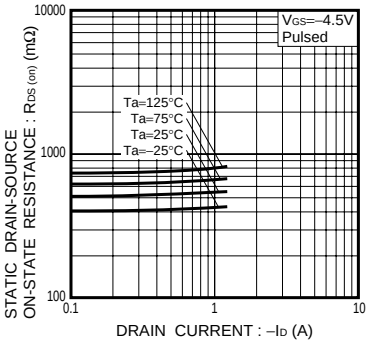


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current (II)

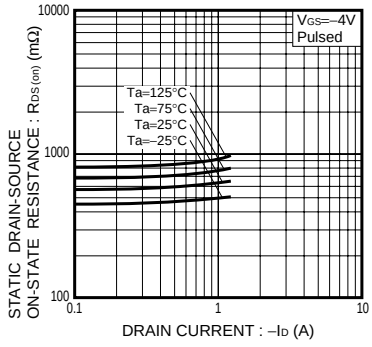


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current (III)

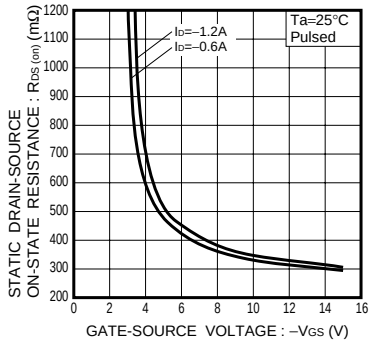


Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

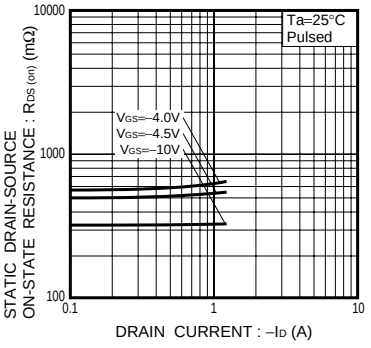


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current (Ⅳ)

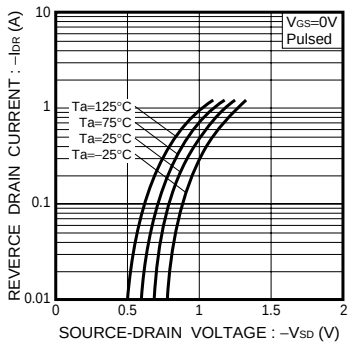


Fig.7 Reverse Drain Current vs. Source-Drain Voltage

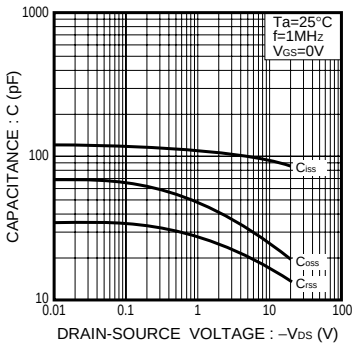


Fig.8 Typical Capacitance vs. Drain-Source Voltage

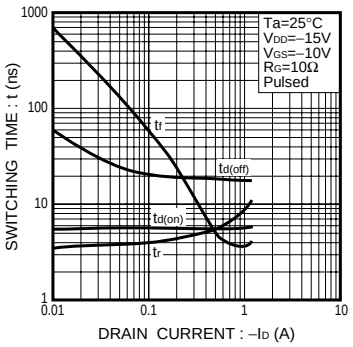


Fig.9 Switching Characteristics

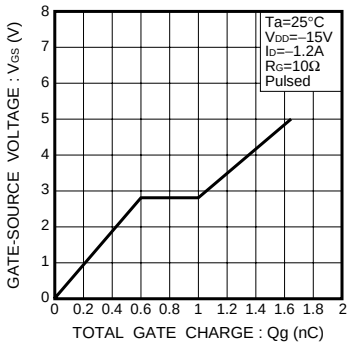


Fig.10 Dynamic Input Characteristics

●Measurement circuits

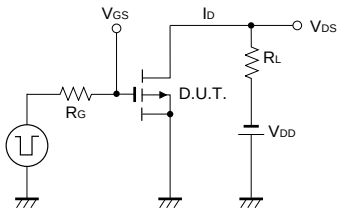


Fig.11 Switching Time Measurement Circuit

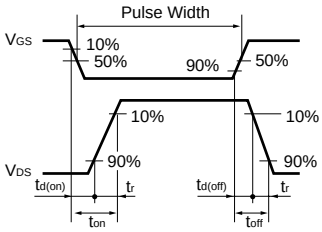


Fig.12 Switching Waveforms

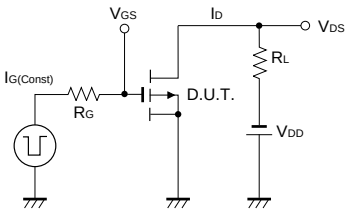


Fig.13 Gate Charge Measurement Circuit

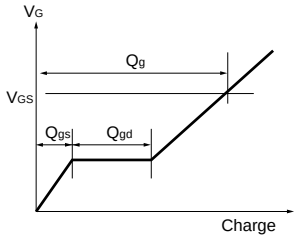


Fig.14 Gate Charge Waveforms