PHE13003C

NPN power transistor

Rev. 1 — 29 July 2010 Preliminary data sheet

1. Product profile

1.1 General description

High voltage, high speed, planar passivated NPN power switching transistor in a SOT54 (TO-92) 3 leads plastic package.

1.2 Features and benefits

- Fast switching
- High typical DC current gain
- High voltage capability of 700 V

1.3 Applications

- Compact fluorescent lamps (CFL)
- Low power electronic lighting ballasts
- Off-line self-oscillating power supplies (SOPS) for battery charging

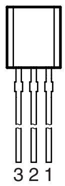
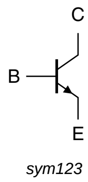
1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_C	collector current	DC	-	-	1.5	A
P_{tot}	total power dissipation	$T_{lead} \leq 25$ °C; see Figure 1	-	-	2.1	W
V_{CESM}	collector-emitter peak voltage	$V_{BE} = 0$ V	-	-	700	V
Static characteristics						
h_{FE}	DC current gain	$I_C = 0.5$ A; $V_{CE} = 2$ V; $T_{lead} = 25$ °C	8	17	25	

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	B	base	 SOT54 (TO-92)	
2	C	collector		
3	E	emitter		

3. Ordering information

Table 3. Ordering information

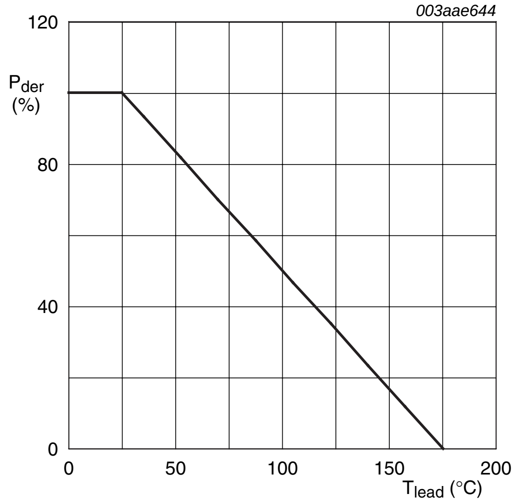
Type number	Package		
	Name	Description	Version
PHE13003C	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CESM}	collector-emitter peak voltage	V_{BE} = 0 V	-	700	V
V_{CBO}	collector-base voltage	I_E = 0 A	-	700	V
V_{CEO}	collector-emitter voltage	I_B = 0 A	-	400	V
I_C	collector current	DC	-	1.5	A
I_{CM}	peak collector current		-	3	A
I_B	base current	DC	-	0.75	A
I_{BM}	peak base current		-	1.5	A
P_{tot}	total power dissipation	$T_{lead} \leq 25$ °C; see Figure 1	-	2.1	W
T_{stg}	storage temperature		-65	150	°C
T_j	junction temperature		-	150	°C
V_{EBO}	emitter-base voltage	I_C = 0 A; I(Emitter) = 10 mA	-	9	V



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\,\%$$

Fig 1. Normalized total power dissipation as a function of lead temperature

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j\text{-}lead)}$	thermal resistance from junction to lead	see Figure 2	-	-	60	K/W
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient	in free air; printed-circuit board mounted; lead length = 4 mm	-	150	-	K/W

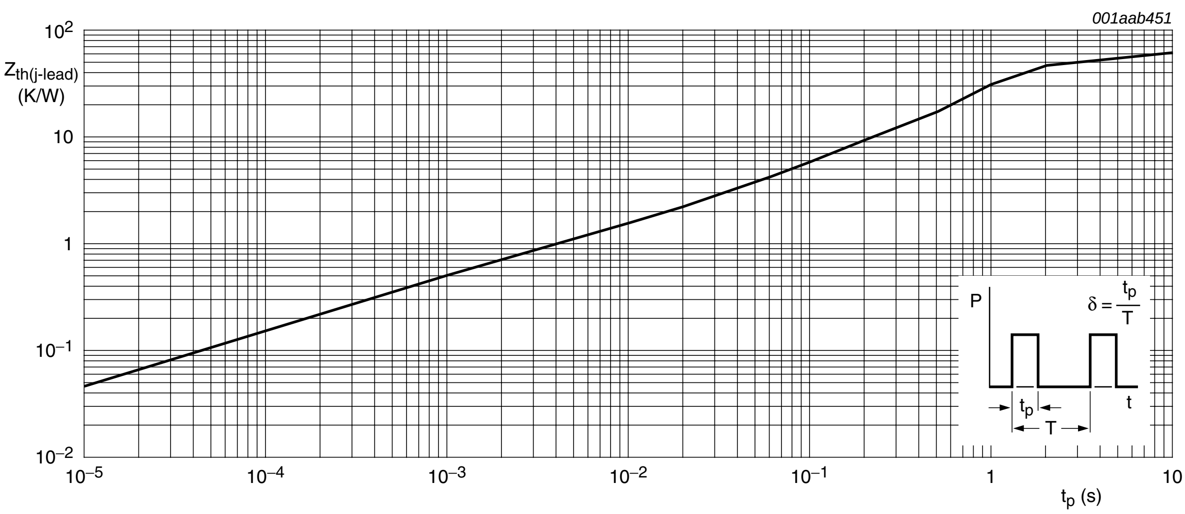


Fig 2. Transient thermal impedance from junction to lead as a function of pulse width

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{CES}	collector-emitter cut-off current	V_{BE} = 0 V; V_{CE} = 700 V; T_j = 125 °C	-	-	5	mA
		V_{BE} = 0 V; V_{CE} = 700 V; T_j = 25 °C	-	-	1	mA
I_{CEO}	collector-emitter cut-off current	V_{CE} = 400 V; I_B = 0 A; T_{lead} = 25 °C	-	-	0.1	mA
I_{EBO}	emitter-base cut-off current	V_{EB} = 9 V; I_C = 0 A; T_{lead} = 25 °C	-	-	1	mA
V_{CEOsus}	collector-emitter sustaining voltage	I_B = 0 A; I_C = 1 mA; L_C = 25 mH; T_{lead} = 25 °C; see Figure 3; see Figure 4	400	-	-	V
V_{CEsat}	collector-emitter saturation voltage	I_C = 0.5 A; I_B = 0.1 A; T_{lead} = 25 °C	-	-	0.5	V
		I_C = 1 A; I_B = 0.25 A; T_{lead} = 25 °C	-	-	1	V
		I_C = 1.5 A; I_B = 0.5 A; T_{lead} = 25 °C	-	-	1.5	V
V_{BEsat}	base-emitter saturation voltage	I_C = 0.5 A; I_B = 0.1 A; T_{lead} = 25 °C	-	-	1	V
		I_C = 1 A; I_B = 0.25 A; T_{lead} = 25 °C	-	-	1.2	V
h_{FE}	DC current gain	I_C = 0.5 A; V_{CE} = 2 V; T_{lead} = 25 °C	8	17	25	
		I_C = 1 A; V_{CE} = 2 V; T_{lead} = 25 °C	5	9	15	
Dynamic characteristics						
t_{on}	turn-on time	I_C = 1 A; I_{Bon} = 0.2 A; I_{Boff} = -0.2 A; R_L = 75 Ω; T_{lead} = 25 °C; resistive load; see Figure 5; see Figure 6	-	-	1	µs
t_s	storage time		-	-	4	µs
		I_C = 1 A; I_{Bon} = 0.2 A; V_{BB} = -5 V; L_B = 1 µH; T_{lead} = 25 °C; inductive load; see Figure 7; see Figure 8	-	0.8	-	µs
t_f	fall time	I_C = 1 A; I_{Bon} = 0.2 A; I_{Boff} = -0.2 A; R_L = 75 Ω; T_{lead} = 25 °C; resistive load; see Figure 5; see Figure 6	-	-	0.7	µs
		I_C = 0.5 A; I_{Bon} = 0.1 A; V_{BB} = -5 V; L_B = 1 µH; T_{lead} = 25 °C; inductive load; see Figure 7; see Figure 8	-	0.1	-	µs

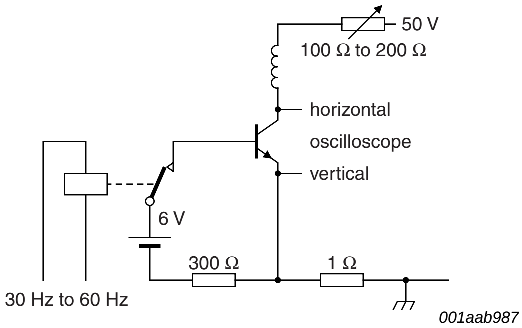


Fig 3. Test circuit for collector-emitter sustaining voltage

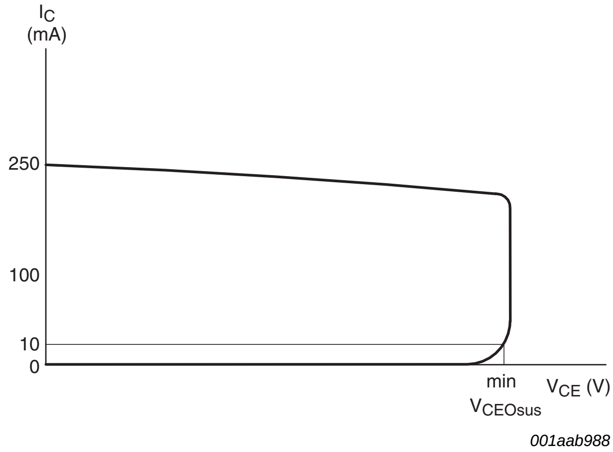
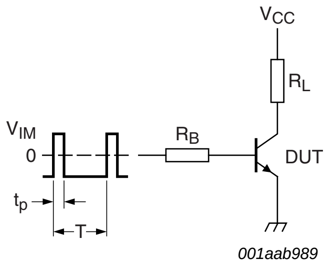


Fig 4. Oscilloscope display for collector-emitter sustaining voltage test waveform



$V_{IM} = -6$ to $+8$ V; $V_{CC} = 250$ V; $t_p = 20$ μs; $\delta = \frac{t_p}{T} = 0.01$

R_B and R_L calculated from I_{Con} and I_{Bon} requirements.

Fig 5. Test circuit for resistive load switching

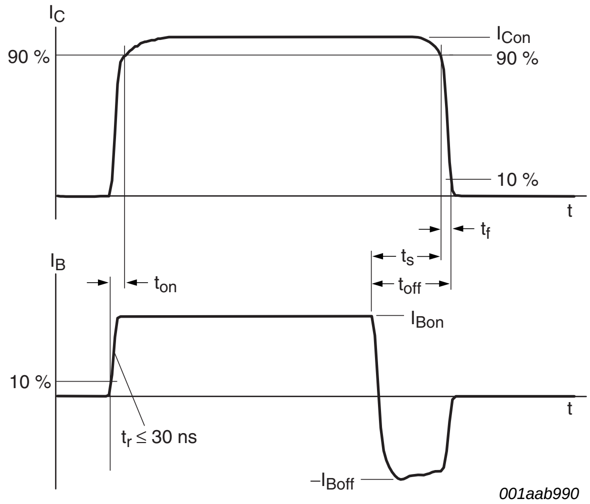
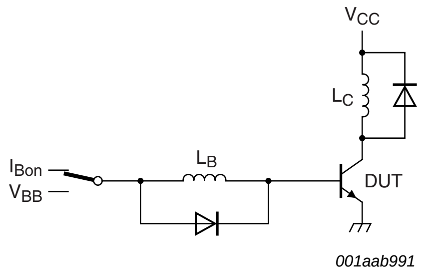


Fig 6. Switching times waveforms for resistive load



$$V_{CC} = 300\ V; V_{BB} = -5\ V; L_C = 200\ \mu H; L_B = 1\ \mu H$$

Fig 7. Test circuit for inductive load switching

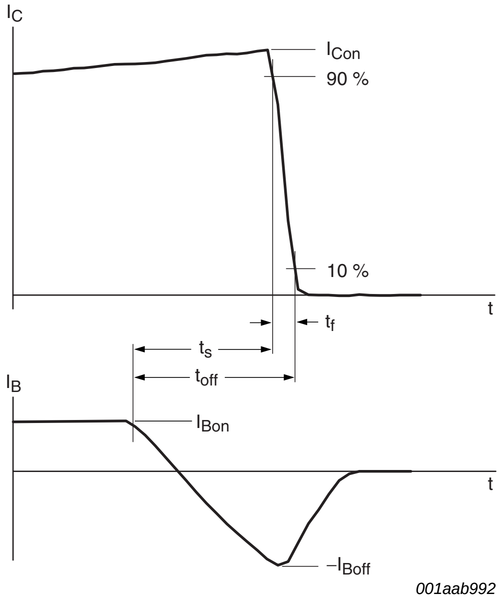
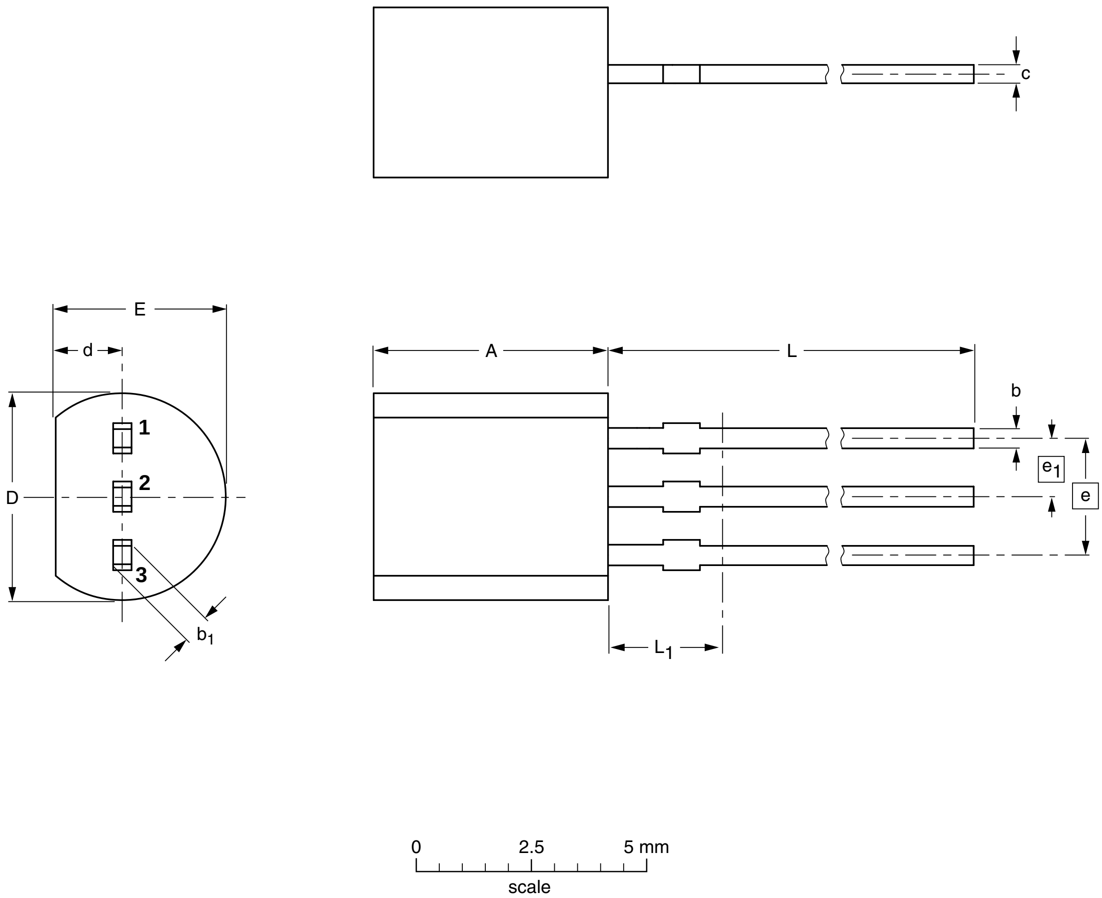


Fig 8. Switching times waveforms for inductive load

7. Package outline

Plastic single-ended leaded (through hole) package; 3 leads **SOT54**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b_1	c	D	d	E	e	e_1	L	L_1(1) max.
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

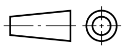
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT54		TO-92	SC-43A			~~04-06-28~~ 04-11-16

Fig 9. Package outline SOT54 (TO-92)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHE13003C v.1	20100729	Preliminary data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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11. Contents

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