

**÷2, ÷4, ÷8 Clock
Generation Chip**

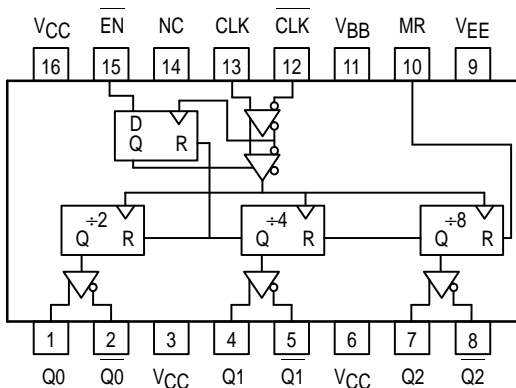
The MC10/100EL34 is a low skew ÷2, ÷4, ÷8 clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. In addition, by using the V_{BB} output, a sinusoidal source can be AC coupled into the device (see Interfacing section of the ECLinPS™ Data Book DL140/D). If a single-ended input is to be used, the V_{BB} output should be connected to the CLK input and bypassed to ground via a 0.01µF capacitor. The V_{BB} output is designed to act as the switching reference for the input of the EL34 under single-ended input conditions, as a result, this pin can only source/sink up to 0.5mA of current.

The common enable (EN) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

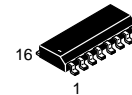
Upon startup, the internal flip-flops will attain a random state; the master reset (MR) input allows for the synchronization of the internal dividers, as well as multiple EL34s in a system.

- 50ps Output-to-Output Skew
- Synchronous Enable/Disable
- Master Reset for Synchronization
- 75kΩ Internal Input Pulldown Resistors
- >1000V ESD Protection

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



**MC10EL34
MC100EL34**



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B-05

PIN DESCRIPTION

PIN	FUNCTION
CLK	Diff Clock Inputs
EN	Sync Enable
MR	Master Reset
V _{BB}	Reference Output
Q ₀	Diff ÷2 Outputs
Q ₁	Diff ÷4 Outputs
Q ₂	Diff ÷8 Outputs

FUNCTION TABLE

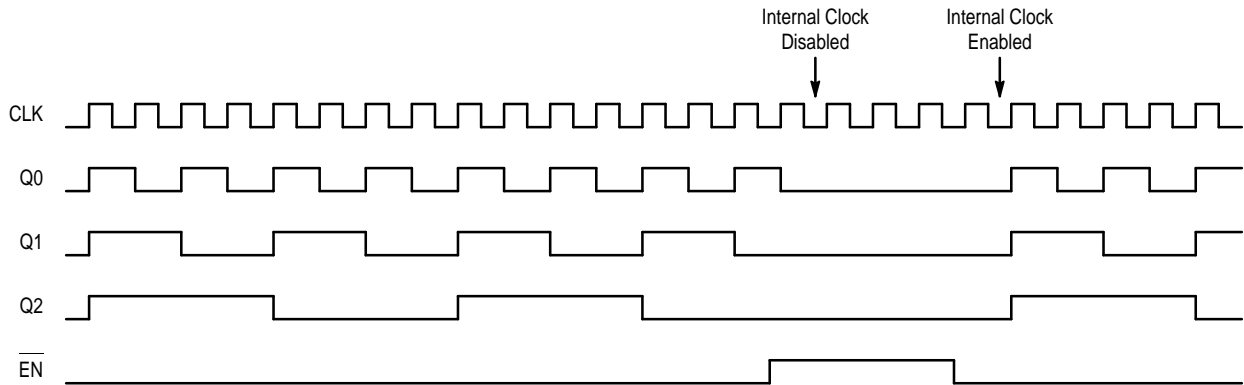
CLK	EN	MR	FUNCTION
Z	L	L	Divide
ZZ	H	L	Hold Q ₀₋₃
X	X	H	Reset Q ₀₋₃

Z = Low-to-High Transition
ZZ = High-to-Low Transition



AC/DC CHARACTERISTICS ($V_{EE} = V_{EE(min)}$ to $V_{EE(max)}$; $V_{CC} = GND$)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{MAX}	Max Toggle Frequency	1100			1100			1100			1100			MHz
I _{EE}	Power Supply Current			39 39			39 39			39 39			39 42	mA
V _{BB}	Output Reference Voltage	10EL 100EL	-1.43 -1.38	-1.30 -1.26	-1.38 -1.38		-1.27 -1.26	-1.35 -1.38		-1.25 -1.26	-1.31 -1.38		-1.19 -1.26	V
I _{IH}	Input High Current		150				150			150			150	μA
t _{PLH} t _{PHL}	Propagation Delay to Output	CLK→Q0 CLK→Q1,2 MR→Q	960 900 750	1200 1140 1060	960 900 750	1200 1140 1060	960 900 750	1200 1140 1060	970 910 790	1210 1150 1090				ps
t _{SKEW}	Within-Device Skew		100		100		100		100		100			ps
t _S	Setup Time EN		400		400		400		400		400			ps
t _H	Hold Time EN		250		250		250		250		250			ps
V _{PP}	Minimum Input Swing CLK		250		250		250		250		250			mV
V _{CMR}	Common Mode Range CLK		-2.0	-0.4	-2.0	-0.4	-2.0	-0.4	-2.0	-0.4	-2.0	-0.4		V
t _r t _f	Output Rise/Fall Times Q (20% – 80%)		275	525	275	525	275	525	275	525	275	525		ps

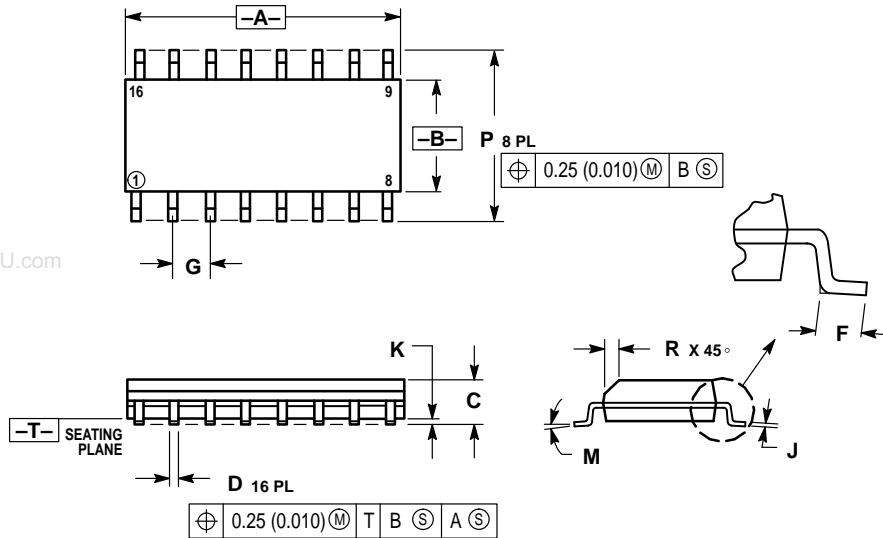


The EN signal will freeze the internal clocks to the flip-flops on the first falling edge of CLK after its assertion. The internal dividers will maintain their state during the internal clock freeze and will return to clocking once the internal clocks are unfrozen. The outputs will transition to their next states in the same manner, time and relationship as they would have had the EN signal not been asserted.

Figure 1. Timing Diagram

OUTLINE DIMENSIONS

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B-05
ISSUE J



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

How to reach us:

USA/EUROPE/Locations Not Listed: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036. 1-800-441-2447 or 602-303-5454

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, 6F Seibu-Butsuryu-Center, 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-81-3521-8315

MFAX: RMFAX0@email.sps.mot.com - TOUCHTONE 602-244-6609
INTERNET: <http://Design-NET.com>

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

