RFH45N05, RFH45N06

File Number 1635

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

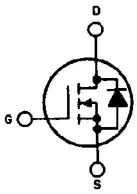
45 A, 50 V - 60 V

$r_{DS(on)}$ = 0.040 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*
- *High-current, low-inductance package*

TERMINAL DIAGRAM



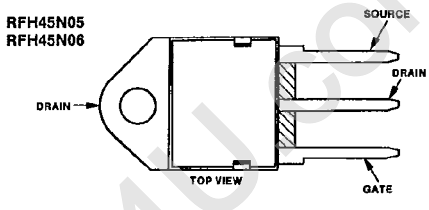
N-CHANNEL ENHANCEMENT MODE

The RFH45N05 and RFH45N06* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFH-types are supplied in the JEDEC TO-218AC plastic package.

*The RFH45N05 and RFH45N06 types were formerly RCA developmental numbers TA9480A and TA9480B respectively.

TERMINAL DESIGNATIONS



JEDEC TO-218AC

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25° C):*

		RFH45N05	RFH45N06	
DRAIN-SOURCE VOLTAGE	V_{DSS}	50	60	V
DRAIN-GATE VOLTAGE, R_{gs} = 1 MΩ	V_{DGR}	50	60	V
GATE-SOURCE VOLTAGE	V_{GS}	±20		V
DRAIN CURRENT, RMS Continuous	I_D	45		A
Pulsed	I_{DM}	100		A
POWER DISSIPATION @ T_C = 25° C	P_T	150		W
Derate above T_C = 25° C		1.2		W/° C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150		° C

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25°C unless otherwise specified.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS RFH45N05 Min.	LIMITS RFH45N05 Max.	LIMITS RFH45N06 Min.	LIMITS RFH45N06 Max.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	50	—	60	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V	—	1	—	—	μA
		V_{DS} = 50 V	—	—	—	1	
		T_C = 125°C, V_{DS} = 40 V	—	50	—	—	
		V_{DS} = 50 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V, V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 22.5 A, V_{GS} = 10 V	—	0.9	—	0.9	V
		I_D = 45 A, V_{GS} = 10 V	—	3.6	—	3.6	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 22.5 A, V_{GS} = 10 V	—	.04	—	.04	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V, I_D = 22.5 A	10	—	10	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	1800	—	1800	
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	750	—	750	
Turn-On Delay Time	$t_d(on)$	V_{DS} = 30 V	40(typ)	80	40(typ)	80	ns
Rise Time	t_r	I_D = 22.5 A	310(typ)	475	310(typ)	475	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50Ω	220(typ)	350	220(typ)	350	
Fall Time	t_f	V_{GS} = 10 V	240(typ)	375	240(typ)	375	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFH45N05, RFH45N06 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS RFH45N05 Min.	LIMITS RFH45N05 Max.	LIMITS RFH45N06 Min.	LIMITS RFH45N06 Max.	UNITS
Diode Forward Voltage	V_{SD} *	I_{SD} = 22.5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100 A/μs	150 (typ.)		150 (typ.)		ns

* Pulse Test: Width ≤ 300 μs, Duty cycle ≤ 2%.

RFH45N05, RFH45N06

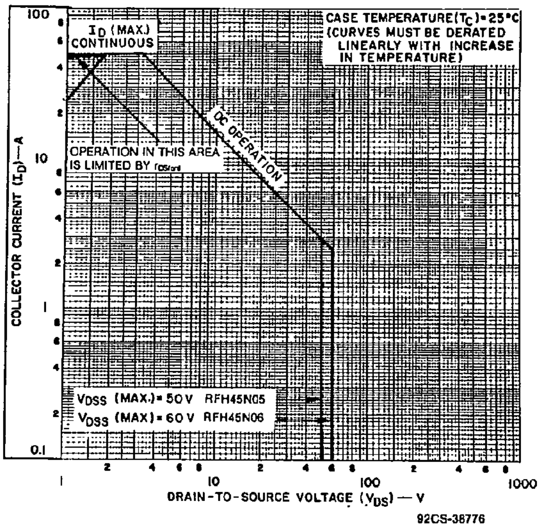


Fig. 1 - Maximum safe operating areas for all types.

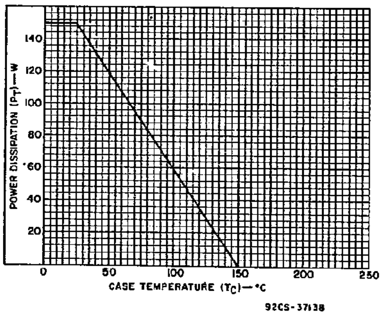


Fig. 2 - Power vs. temperature derating curve for all types.

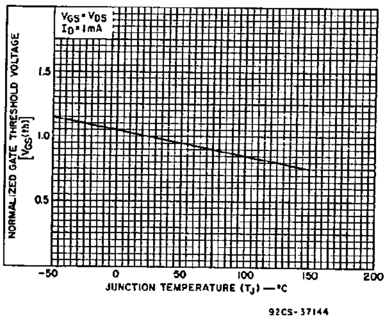


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

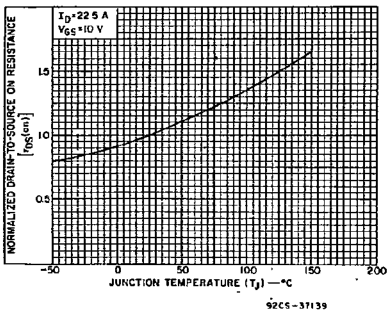


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

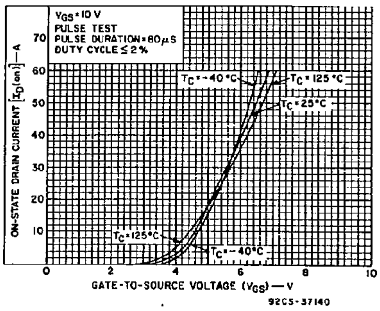


Fig. 5 - Typical transfer characteristics for all types.

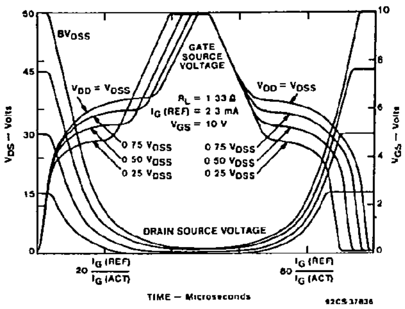


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

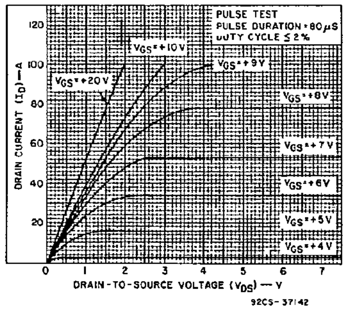


Fig. 7 - Typical saturation characteristics for all types.

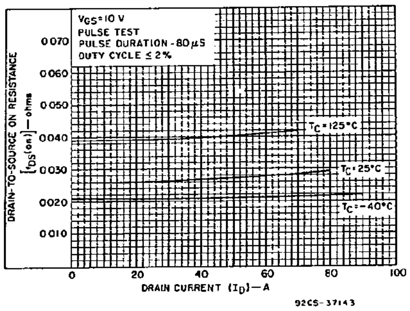


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

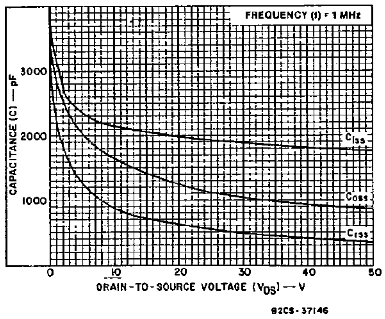


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

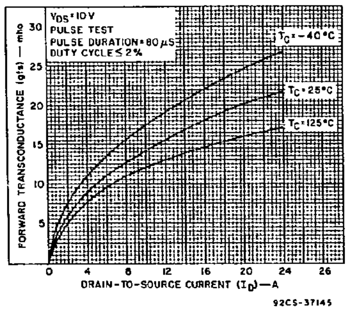


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

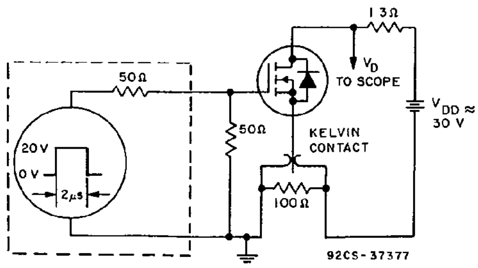


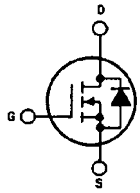
Fig. 11 - Switching Time Test Circuit.

RFK45N05, RFK45N06 File Number **1498**

N-Channel Enhancement-Mode Power Field-Effect Transistors

45 A, 50 V - 60 V
$r_{DS}(on) = 0.040\ \Omega$

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



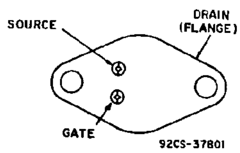
N-CHANNEL ENHANCEMENT MODE

The RFK45N05 and RFK45N06* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFK-types are supplied in the JEDEC TO-204AE steel package.

*The RFK45N05 and RFK45N06 types were formerly RCA developmental numbers TA9388A and TA9388B, respectively.

TERMINAL DESIGNATIONS



JEDEC TO-204AE

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

		RFK45N05		RFK45N06	
DRAIN-SOURCE VOLTAGE	V_{DSS}	50		60	V
DRAIN-GATE VOLTAGE, R_{GS}=1 MΩ	V_{DGR}	50		60	V
GATE-SOURCE VOLTAGE	V_{GS}		±20		V
DRAIN CURRENT, RMS Continuous	I_D		45		A
Pulsed	I_{DM}		100		A
POWER DISSIPATION @ T_C=25°C	P_T		150		W
Derate above T_C=25°C			1.2		W/°C
OPERATING AND STORAGE TEMPERATURE	T_J, T_{stg}		-55 to +150		°C

RFK45N05, RFK45N06

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25°C unless otherwise specified.*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS RFK45N05 MIN.	MAX.	RFK45N06 MIN.	MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	50	—	60	—	V
Gate Threshold Voltage	$V_{GS}(th)$	$V_{GS}=V_{DS}$ I_D=1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40 V V_{DS}=50 V	— —	1 —	— —	— 1	μA
		T_C=125°c V_{DS}=40 V V_{DS}=50 V	— —	50 —	— —	— 50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$*	I_D=22.5 A V_{GS}=10 V	—	0.9	—	0.9	V
		I_D=45 A V_{GS}=10 V	—	3.6	—	3.6	
Static Drain-Source On Resistance	$r_{DS}(on)$*	I_D=22.5 A V_{GS}=10 V	—	.04	—	.04	Ω
Forward Transconductance	g_{fs}*	V_{DS}=10 V I_D=22.5 A	10	—	10	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	1800	—	1800	
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	750	—	750	
Turn-On Delay Time	$t_d(on)$	V_{DD} = 30 V	40(typ)	80	40(typ)	80	ns
Rise Time	t_r	I_D=22.5 A	310(typ)	475	310(typ)	475	
Turn-Off Delay Time	$t_d(off)$	$R_{gen}=R_{gs}$=50 Ω	220(typ)	350	220(typ)	350	
Fall Time	t_f	V_{GS}=10 V	240(typ)	375	240(typ)	375	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFK45N05, RFK45N06 Series	—	0.83	—	0.83	°C/W

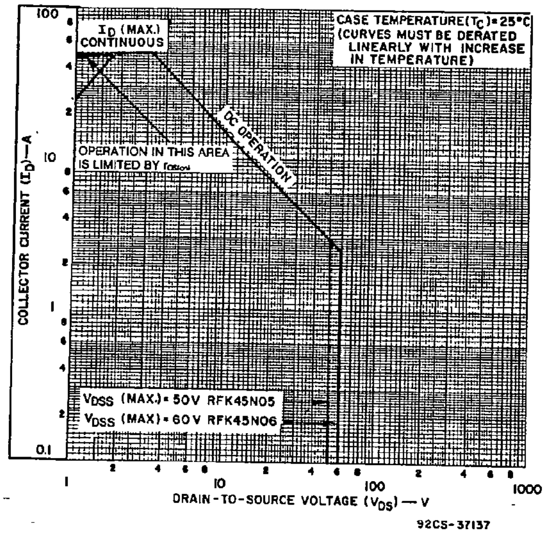
*Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS RFK45N05 Min.	Max.	RFK45N06 Min.	Max.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 22.5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A d_{IF}/d_t = 100A/μs	150(typ.)		150(typ.)		ns

*Pulse Test: Width ≤ 300 μs, Duty Cycle ≤ 2%.

RFK45N05, RFK45N06



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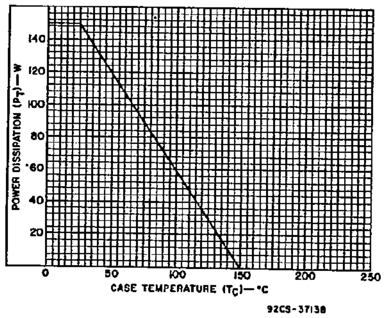


Fig. 2 — Power vs. temperature derating curve for all types.

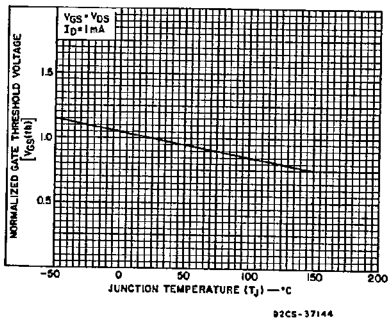


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

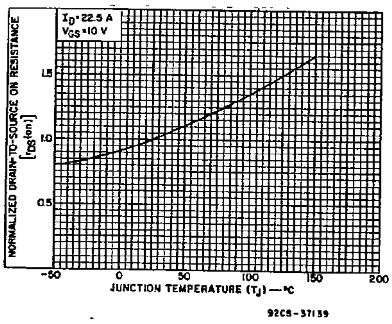
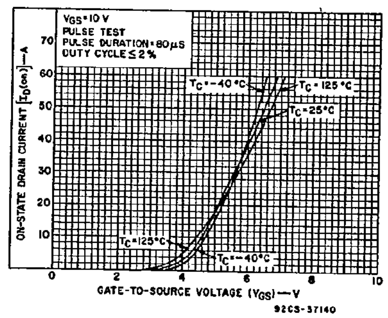


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.



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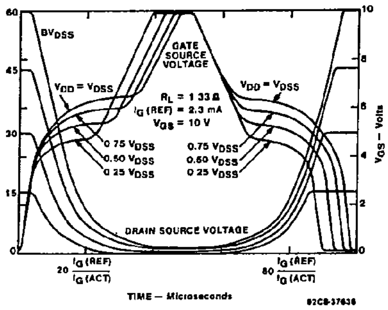

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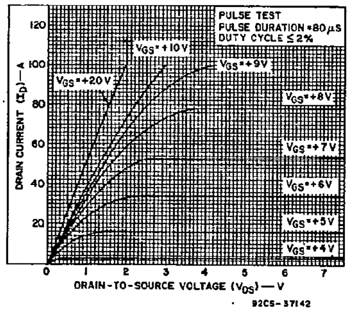

Fig. 7 — Typical saturation characteristics for all types.

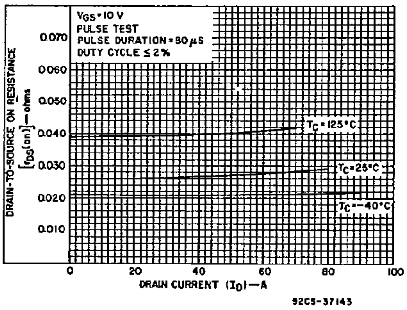

Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

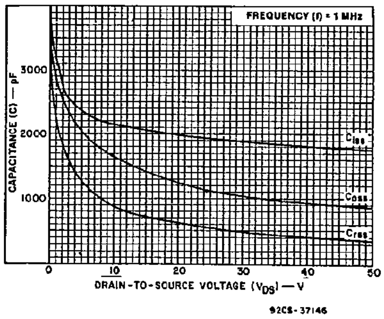

Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

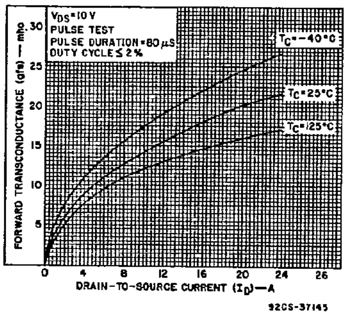

Fig. 10 — Typical forward transconductance as a function of drain current for all types.

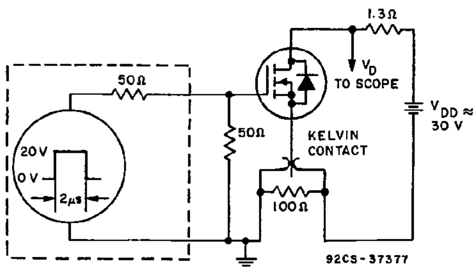

Fig. 11 - Switching Time Test Circuit.