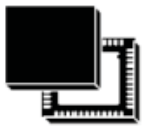
PM6602

8-row 30-mA LED driver with boost regulator, dual dimming mode, SMBus interface and DPST for LCD panel backlights

Preliminary data

Features

- 2 dimming modes: SMBus or PWM
- Boost section
  - 3.3 V to 28 V input voltage range
  - Internal power MOSFET
  - Internal +3.3 V LDO for device supply
  - Up to 36 V output voltage
  - Constant frequency peak current mode control
  - 500 kHz to 2 MHz adjustable switching frequency
  - Pulse-skip power saving mode at light loads
  - Built-in soft-start feature
  - Programmable OVP protection
  - Stable with ceramic output capacitors
  - Thermal shutdown
- Backlight driver section
  - 8 rows with 30 mA maximum current capability (adjustable)
  - Row disabling option
  - 500 ns minimum dimming time (1% minimum dimming duty-cycle at 20 kHz)
  - ±3% current accuracy
  - ±2% current balance
  - LED failure (open and short circuit) detection



VFQFPN-24 4x4

AM03692v1

Description

The PM6602 consists of a high-efficiency monolithic boost converter and eight controlled current generators (ROWs), specifically designed to supply LED arrays used in the backlights of LCD panels. The device can manage a nominal output voltage of up to 36 V. The generators can be externally programmed to sink up to 30 mA and they can be dimmed in two different modes: via a PWM signal (1% dimming duty-cycle at 20 kHz can be managed) or in SMBus mode. The device can detect and manage the open and shorted LED faults. The device detects the unused ROWs (connected to SGND). Basic protections (output overvoltage, internal MOSFET overcurrent and thermal shutdown) are provided.

Applications

- Backlights of notebook monitors
- Backlights of UMPC monitors

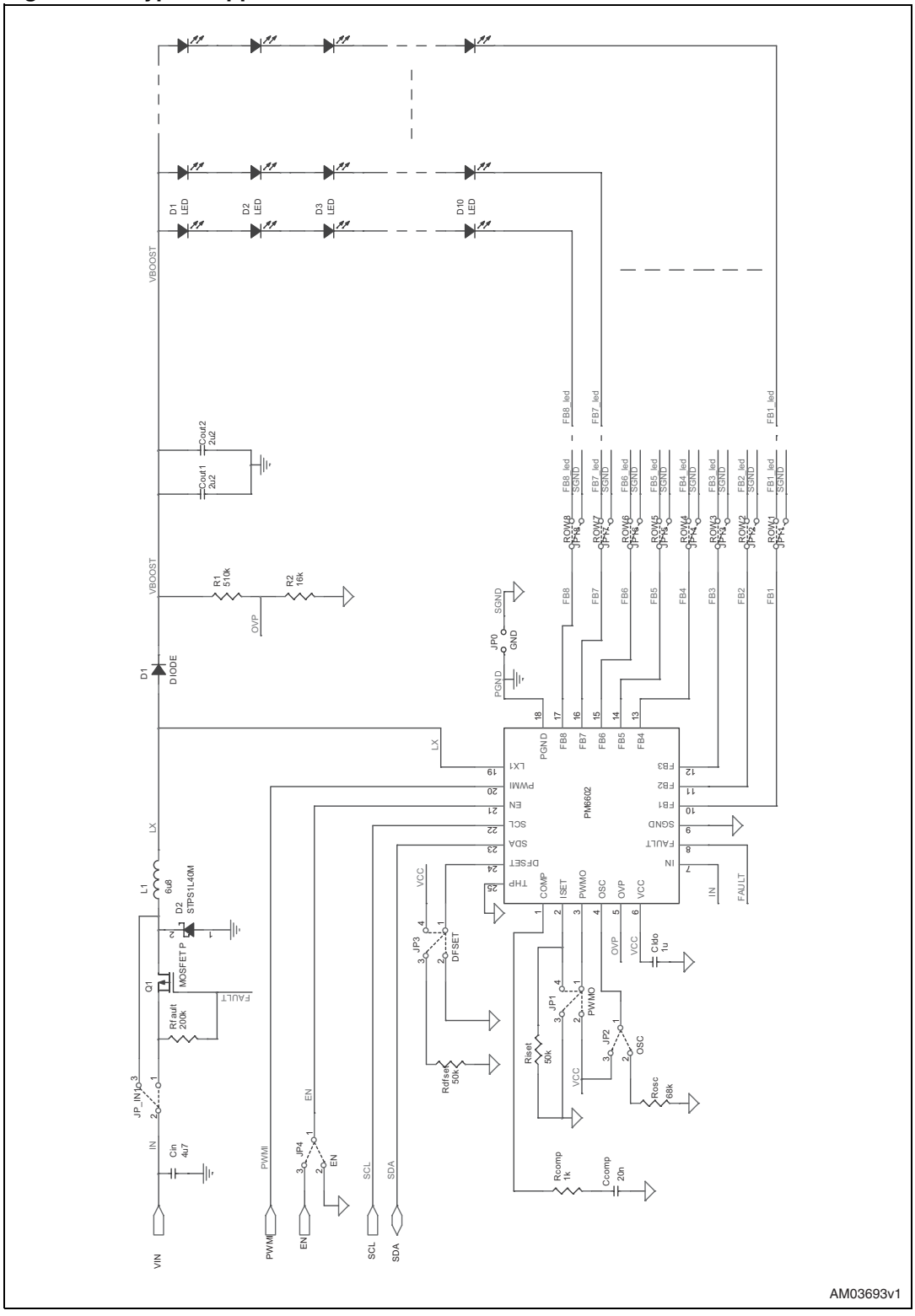
Table 1. Device summary

Part number	Package	Packaging
PM6602	VFQFPN-24 4 mm x 4 mm (exposed pad)	Tube
PM6602TR		Tape and reel

Contents

1 Typical application circuit

Figure 1. Typical application circuit



2 Device pinout

Figure 2. Device pinout (top view)

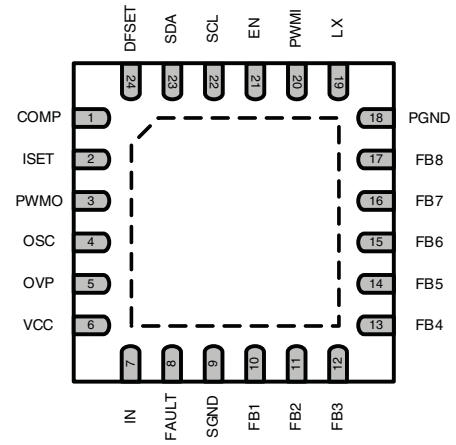


Table 2. Pin description

Pin #	Name	Description
1	COMP	Error amplifier output. A simple RC series between this pin and ground is needed to compensate the loop of the boost regulator.
2	ISET	Current limit setting for the output generators. The output current of the ROWs can be programmed by connecting a resistor to SGND.
3	PWMO	PWI filter corner frequency selection. Leave the pin floating to set 195.6 Hz as corner frequency. Short directly to GND to set 12.225 Hz.
4	OSC	Switching frequency selection. A resistor to SGND is used to set the desired switching frequency.
5	OVP	Overvoltage selection. Used to set the desired OV threshold by an external resistor divider.
6	VCC	+3.3 V LDO output
7	IN	Input voltage. Connect to the main supply rail.
8	FAULT	External power MOSFET driver output. Open drain pin.
9	SGND	Signal ground. Supply return for the analog circuitry and current generators.
10-17	FB1 to FB8	Row driver output #1 to row driver output #8. If a FBx is unused, short the pin to SGND.
18	PGND	Power ground. Internal power MOSFET ground.
19	LX	Switching node. Drain of the internal power MOSFET.
20	PWMI	Dimming input. Used to externally set the brightness by using a PWM signal.
21	EN	Device enable Input in PWM dimming mode. Unused in SMBus mode, to be connected to SGND.

Table 2. Pin description (continued)

Pin #	Name	Description
22	SCL	SMBus clock
23	SDA	SMBus data
24	DFSET	Dimming frequency selection in SMBus mode, using a rusticator to SGND. Directly connect to SGND to setup the PWM dimming mode

3 Absolute maximum ratings

Table 3. Absolute maximum ratings(1)

Symbol	Parameter	Value	Unit
V_{CC}	V_{CC} to SGND	-0.3 to 3.6	V
	PGND to SGND	-0.3 to 0.3	
V_{IN}	IN to PGND	-0.3 to 30	
V_{LX}	LX to SGND, LX to PGND	-0.3 to 40	
	ISET, PWMO, OVP, OSC, COMP, DFSET to SGND	-0.3 to V_{AVCC} +0.3	
	EN, PWMI to SGND	-0.3 to 6	
	SDA, SCL to SGND	-0.3 to 6	
	FBx to PGND/SGND	-0.3 to 40	
	FAULT to SGND	-0.3 to 30	
	Maximum LX RMS current	2.0	A
P_{TOT}	Power dissipation T_{amb} = 25° C	2.3	W
	Maximum withstanding voltage range test condition: CDF-AEC-Q100-002: "human body model" acceptance criteria: "normal performance"	TBD(2)	kV
	ESD machine model	TBD(2)	V

1. Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. ESD test to be performed at ±2 kV HBM and ±200 V MM.

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction to ambient	42	°C/W
$T_{storage}$	Storage temperature range	-50 to 150	°C
T_j	Junction operating temperature range	-40 to 125	°C
T_{amb}	Operating ambient temperature range	-40 to 85	°C

Note: Solderability specification according to JEDEC standard #J-STD-020D.

Table 5. Recommended operating conditions

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply section						
V_{IN}	Input voltage range		3.3		28	V
Boost section						
	Boost supply		3.3		28	V
V_{BST}	Output voltage range				36	
f_{SW}	Adjustable switching frequency	OSC connected to R_{FSW}	500		2000	kHz
	FBs output maximum current				30	mA
	PWMI input frequency	PWM mode	0.1		30	kHz
		SMBus mode	9.5	10	10.5	

4 Electrical characteristics

Table 6. Electrical characteristics
(V_{IN} = 12 V, T_{amb} = T_j = 25° C unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply section						
$I_{IN,Q}$	Operating quiescent current	R_{ISET} = 50 kΩ Current generators turned off		1		mA
$I_{IN,SHDN}$	Operating current in shutdown	EN low and BL_CTL = 0, V_{IN} = 12 V, Device OFF		35		µA
LDO linear regulator						
	LDO output voltage	EN high, I_{LDO} = 0 mA		3.3		V
Boost section						
	Adjustable switching frequency	OSC to SGND with a resistor	500		2000	kHz
	Internal power mos $R_{DS(on)}$			200		mΩ
	LX leakage current	LX = 40 V		5		µA
	Peak current limit			2.3		A
OV and fault protections						
$V_{TH,OVP}$	Hard overvoltage protection reference (OVP) threshold			1.35		V
$V_{TH,FRD}$	Floating row detection (OVP) threshold			1.25		V
T_{SHDN} (1)	Thermal shutdown turn-off temperature			150		°C
Soft-start and power management						
	EN, high level threshold	TTL level	2.1			V
	EN, low level threshold	TTL level			0.8	
	PWMI, high level threshold	TTL level	2.1			
	PWMI, low level threshold	TTL level			0.8	
Current generators section						
	FBs current minimum on time	RISET = 50 kΩ		500		ns
T_{DIMMAX}	The time that occurs before the device goes into a new soft-start in case of 0% brightness			30		ms
	FBs output maximum current			30		mA
	FBs leakage current			5		µA
	Dimming oscillator frequency		100		5000	Hz

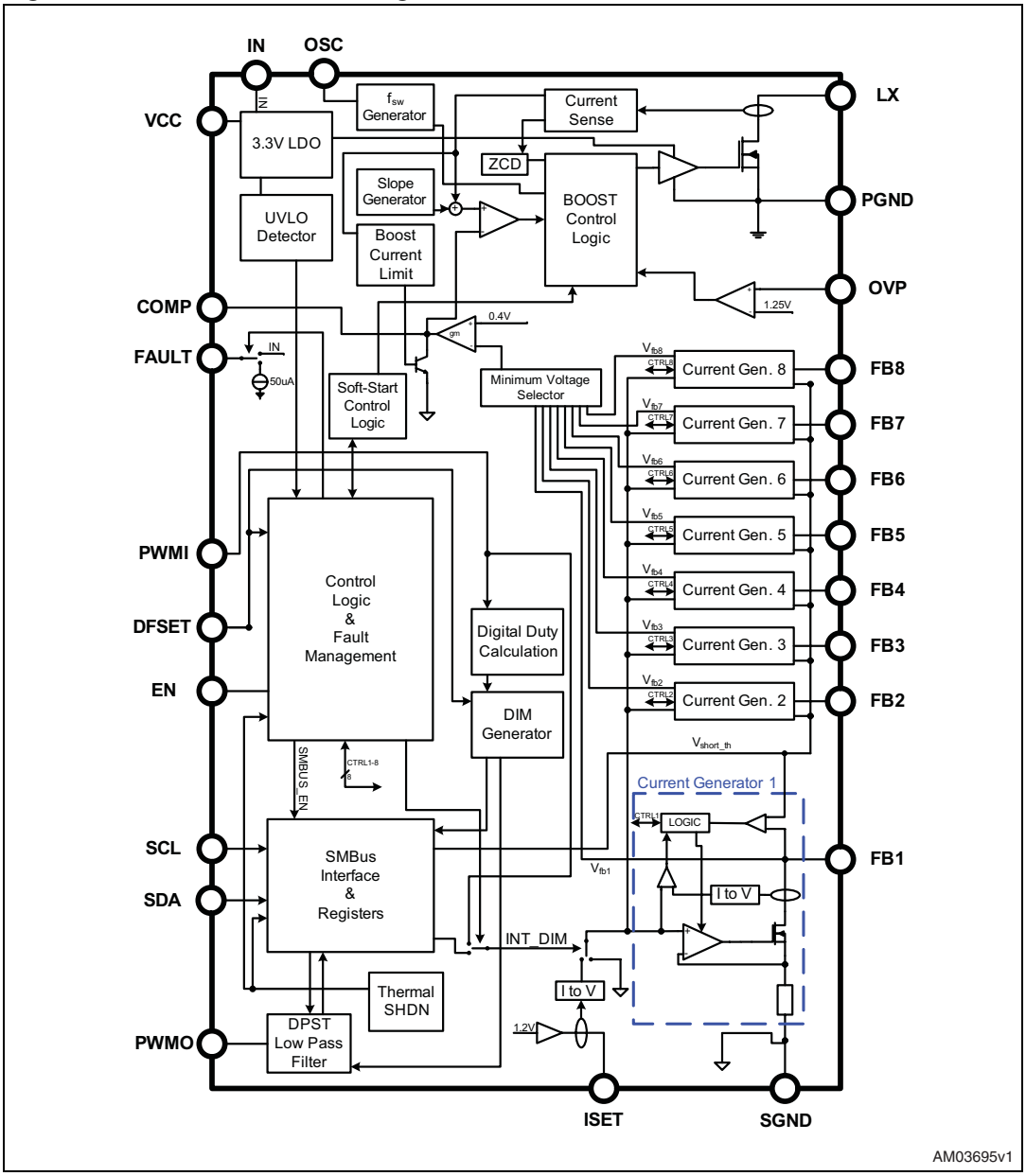
Table 6. Electrical characteristics (V_{IN} = 12 V, T_{amb} = T_j = 25° C unless otherwise specified) (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
SMBus interface (SMBus follows DELL and SMBus 2.0 standards)						
	SMBus frequency		10		100	kHz
	Bus free time			4.7		µs
	Start condition hold time from SCL			4		
	Start condition setup time from SCL			4.7		
	Stop condition setup time from SCL			4		
	SDA hold time from SCL			300		ns
	SDA setup time from SCL			250		
	SCL low period			4.7		µs
	SCL high period			4		
	SDA, SCL high level threshold	TTL level	2.1			V
	SDA, SCL low level threshold	TTL level			0.8	

1. Guaranteed by design.

4.1 Block diagram

Figure 3. STMAFD01 block diagram



5 SMBus interface

The SMBus serial interface is used to turn on the device, monitor faults, set dimming mode and brightness settings and configure the device in general.

The address is set to 0x58. No address pin is provided (compliant with DELL specifications), nor any ROM address configuration.

Additional configuration bits and registers added for device configuration (other than those specified in the DELL specification) include the *shorted led threshold* (2 bits).

The brightness control interface implements the SMBus read byte protocol.

The brightness control interface implements the SMBus write byte protocol.

The brightness control interface's SMBus component operates correctly when the SMBus master clock operates at a frequency of 55 kHz.

The brightness control interface's SMBus component may use clock stretching, but it shall not add more than 10 milliseconds of clock low time between any SMBus start condition and its corresponding stop.

The brightness control interface sends a NAK signal (not acknowledge) in response to any SMBus operation directed to it that does not use the SMBus read byte or write byte protocol.

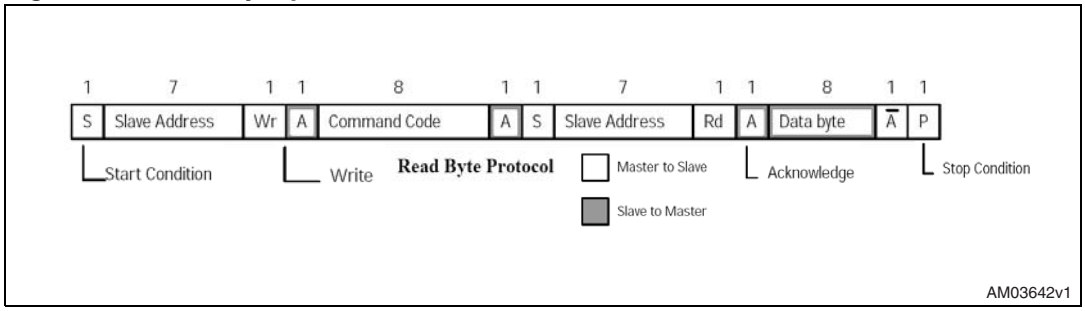
The brightness control interface sends a NAK signal in response to any SMBus operation directed to it that addresses a register that is not defined in this specification.

When the SMBus interface is not powered, the SMBus interface pins provide a high impedance interface to the bus.

Read byte

As shown in *Figure 4*, the four-byte-long read byte protocol starts out with the slave address followed by the "command code" which translates to the "register index". Then the bus direction turns around with the re-broadcast of the slave address with bit 0 indicating a read ("Rd") cycle. The fourth byte contains the data being returned by the backlight controller. That byte value in the data byte should reflect the value of the register being queried at the "command code" index. A dark grey outline is used on cycles during which the backlight controller "owns" or "drives" the data line. All other cycles are driven by the "host".

Figure 4. Read byte protocol

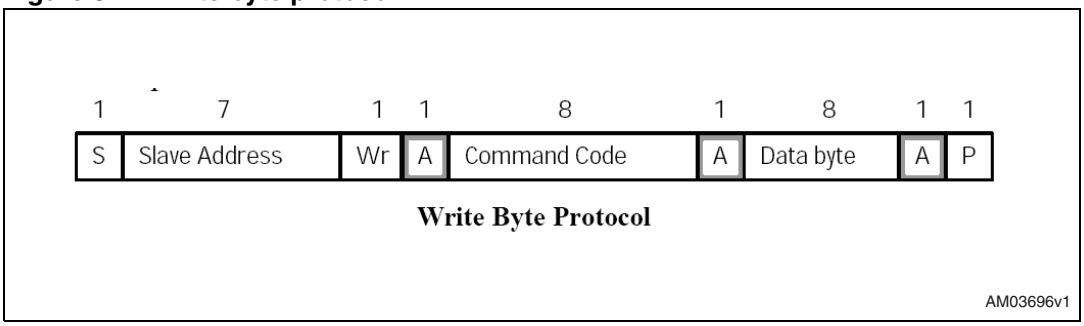


Note that any other protocol missing the "command code" as implemented in some previous backlight controller devices will no longer be supported.

Write byte

The write byte protocol is only three bytes long. The first byte starts with the slave address again followed by the "command code" which translates to the "register index" being written. The third byte contains the data byte that must be written into the register selected by the "command code". Again note the bus directions as highlighted by the dark grey outline.

Figure 5. Write byte protocol



SMB clock stretching

For special cases where clock stretching must be implemented, the maximum clock stretching allowed is 10 ms cumulative per SMB packet (from "start" condition to "stop" condition).

SMBus register definitions

All backlight controller registers are byte-wide and accessible via the read/write_byte protocols. Their bit assignments are provided in the following sections with reserved bits containing a default value of "0".

Brightness control register (0x00)

Due to the Intel® DPST (display power savings technology) the granularity of the brightness control register is 256 steps.

Table 7. Brightness control register

Register 0x00				Brightness control register			
BRT7	BRT6	BRT5	BRT4	BRT3	BRT2	BRT1	BRT0
Bit 7	Bit 6	Bit 5		Bit 3			
(R/W)	(R/W)	(R/W)	Bit 4 (R/W)	(R/W)	Bit 2 (R/W)	Bit 1 (R/W)	Bit 0 (R/W)

Note: BRT [7..0] = 256 steps of brightness.

Specificities of register 0

An SMBus write byte cycle to register 0 sets the brightness level if the backlight controller is in SMBus mode.

A write byte cycle to register 0 has no effect when the backlight controller is not in SMBus mode.

An SMBus read byte cycle to register 0 returns the current brightness level regardless of the value of PWM_SEL.

An SMBus setting of 0xFF for register 0 sets the backlight controller to the maximum brightness output.

An SMBus setting of 0x00 for register 0 sets the backlight controller to the minimum brightness output.

The default value for register 0 is 0xFF.

Device control register (0x01)

This register has two bits that control the operating mode of the backlight controller and a single bit that controls the BL ON/OFF state.

Table 8. Register description

Register 0x00				Device control register			
Reserved	Reserved	Reserved	Reserved	Reserved	PWM_MD	PWM_SEL	BL_CTL
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2 (R/W)	Bit 1 (R/W)	Bit 0 (R/W)

Table 9. Bit field definitions

PWM_MD	= PWM mode select (1 = absolute brightness, 0 =% change) default = 0
PWM_SEL	= Brightness MUX select (1 = PWM pin, 0 = SMBus value) default = 0
BL_CTL	= BL On/Off (1 = On, 0 = Off) default = 0

The PWM_MD bit selects the manner in which the PWM input is to be interpreted. When this bit is 0, the PWM input reflects a percentage change in the current brightness (that is, DPST mode) and should follow the following equation.

Equation 1

$$\text{DPST brightness} = C_{bt}\,(\text{PWM})$$

Where:

- C_{bt} = current brightness setting from SMBus with out influence from the PWM.
- PWM = percentage of duty cycle

The PWM signal starts from 100% when operating in DPST mode.

When PWM_MD is 1, the PWM input has no effect on the brightness setting unless the backlight controller is in PWM mode. When operating in PWM mode, this bit is a don't care.

The PWM_SEL bit determines whether the SMBus or PWM input should drive the brightness.

The relationships between these two control bits can be thought of as specifying an operating mode for the backlight controller. The defined modes are shown in *Table 10 on page 14*.

Note: Depending on the settings of some bits, other bits have no effect and are "don't care". They are shown with a value of X in Table 10.

Table 10. Backlight controller modes selected by device control register bits 1 & 2

PWM_MD	PWM_SEL	Mode
X	1	PWM mode
1	0	SMBus mode
0	0	SMBus mode with DPST

Specificities of register 1

All reserved bits return "0" when read.

All reserved bits are ignored by the backlight controller when written.

All defined control bits return their current, latched value when read.

The backlight controller properly handles any SMBus write that causes multiple control bits to change value.

A value of 1 written to BL_CTL turns on the BL in 10 milliseconds or less after the write cycle completes. The BL is deemed to be on when bit 3 of register 2 is 1.

A value of 0 written to BL_CTL immediately turns off the BL. The BL is deemed to be off when bit 3 of register 2 is 0.

When an SMBus mode is selected, register 0x00 must reflect the last value written to it. However, when any non-SMBus mode is selected, register 0x00 must reflect the current brightness value based on the current mode of operation, with the exception of SMBus mode with DPST.

When SMBus mode with DPST is selected, register 0x00 must reflect the last value written from the SMBus.

When a write to register 1 causes the backlight controller to transition to SMBus mode, the brightness of the BL does not change.

When a write to register 1 causes the backlight controller to transition to a non-SMBus mode, the brightness of the BL changes as appropriate for the new mode.

The default value for register 1 is 0x00

Fault/status register (0x02)

This register has six status bits that allow monitoring the backlight controller's operating state. Bit 0 is a logical "OR" of all fault codes to simplify error detection. Not all of the bits in this register are fault-related - bit 3 is a simple BL status indicator. All reserved bits must return a "0" when read and ignore the bit value when written. All bits in this register are read-only.

Table 11. Register description

Register 0x02				Fault/status register			
Reserved	Reserved	2_CH_SD	1_CH_SD	BL_STAT	OV_CURR	THRM_SHDN	FAULT
Bit 7 (R)	Bit 6 (R)	Bit 5 (R)	Bit 4 (R)	Bit 3 (R)	Bit 2 (R)	Bit 1 (R)	Bit 0 (R)

Table 12. Bit field definitions

Bit num.	Description	Value
Bit 5	2_CH_SD	The number of faulted strings is reported in bits 5 and 4. (00 = no faults, 01 = one string fault, 11 = two or more string faults)
Bit 4	1_CH_SD	
Bit 3	BL_STAT	BL status (1 = BL on, 0 = BL off)
Bit 2	OV_CURR	Input over-current (1 = over-current condition, 0 = current OK)
Bit 1	THRM_SHDN	Thermal shutdown (1 = thermal fault, 0 = thermal OK)
Bit 0	FAULT	Fault occurred (logic "OR" of all of the fault conditions)

Specificities of register 2

All reserved bits return "0" when read.

A write byte cycle to register 2 has no effect. This register is read-only.

A read byte cycle to register 2 always indicates the current BL on/off status in BL_STAT (1 if the BL is on, 0 if the BL is off).

A read byte cycle to register 2 always returns FAULT as the logical OR of THRM_SHDN and OV_CURR and 1_CH_SD and 2_CH_SD only (bits 1, 2, 4 and 5).

The THRM_SHDN bit is optional. If not implemented it always returns 0 when read.

If implemented, the value of THRM_SHDN is 1 when the backlight controller shuts down due to a thermal event. In all other cases the value of THRM_SHDN is 0.

The value of OV_CURR is 1 when the backlight controller shuts down due to an input over-current event. In all other cases, the value of OV_CURR is 0.

A fault does not occur or is not reported when the BL is commanded *on* and immediately *off* by the system.

The value of BL_STAT is 1 whenever the BL is on.

The value of BL_STAT is 0 whenever the BL is off.

The default value for register 2 is 0x00.

When FAULT is set to 1, it is cleared when the BL_CTL bit of the device control register is toggled. At that time, if the fault condition is still present or reoccurs, FAULT is again set to 1.

The device does not indicate a fault if the voltage VBL+ is removed, regardless of whether or not the BL was *on* at the time of the power loss.

In the event that the controller shuts down due to an over-current fault or other fault condition, the controller cannot re-start until a power cycle of VBL+ occurs.

Identification register (0x03)

The ID register contains two bit fields to denote the manufacturer and the silicon revision of the controller IC.

Table 13. Register description

Register 0x03				ID register			
LED panel	MFG3	MFG2	MFG1	MFG0	REV2	REV1	REV0
Bit 7=1	Bit 6 (R)	Bit 5 (R)	Bit 4 (R)	Bit 3 (R)	Bit 2 (R)	Bit 1 (R)	Bit 0 (R)

Table 14. Bit field definitions

MFG [3..0]	Manufacturer ID=5+ST (according to DELL specifications)
REV [2..0]	Silicon rev (Revs 0-7 allowed for silicon spins)

Specificities of register 3

A write byte cycle to register 3 has no effect. This register is read-only.

The value of MFG is 5 for the ST device.

Configuration register (0x04)

The ID register contains two bit fields to set the shorted LED voltage threshold. Three different values are available.

Table 15. Register description

Register 0x03				ID register			
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	VTH1	VTH0
Bit 7=1	Bit 6 (R)	Bit 5 (R)	Bit 4 (R)	Bit 3 (R)	Bit 2 (R)	Bit 1 (R/W)	Bit 0 (R/W)

Table 16. Backlight controller modes

VTH1	VTH0	Mode
0	0	Default value $V_{FBx,FAULT}$=8 V
1	0	$V_{FBx,FAULT}$=2 V
0	1	$V_{FBx,FAULT}$=3.3 V
1	1	No protection

Note: VTH0, VTH1 = shorted LED threshold selection bits.

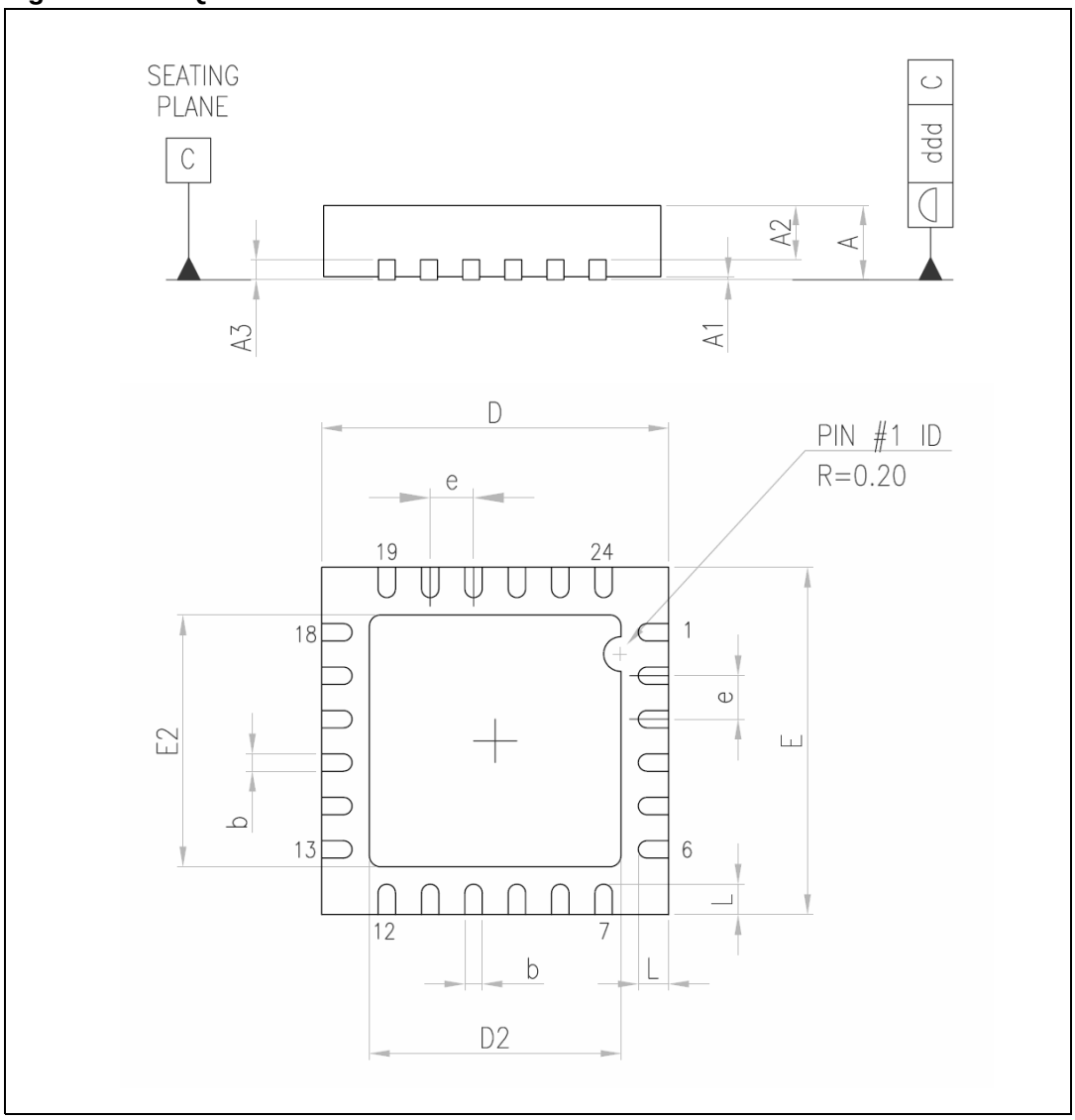
6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 17. VFQFPN-24 mechanical data

Dim.	Min	Typ	Max
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20	
b	0.18	0.25	0.30
D	3.85	4.00	4.15
D2	2.5	2.6	2.7
E	3.85	4.00	4.15
E2	2.5	2.6	2.7
e		0.50	
L	0.30	0.40	0.50
ddd			0.08

Figure 6. VFQFPN-24 mechanical data



7 Revision history

Table 18. Document revision history

Date	Revision	Changes
03-June-2009	1	Initial release.

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