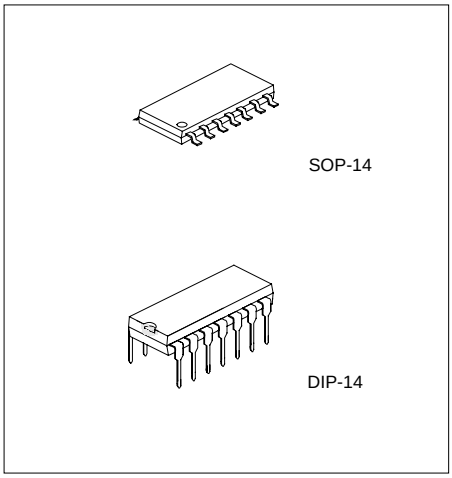
PROGRAMMABLE TIMER



*Pb-free plating product number: CD4541L

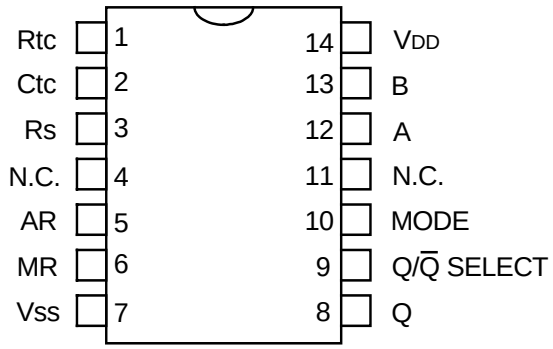
DESCRIPTION

The UTC **CD4541** programmable timer comprise a 16-stage binary counter, an integrated oscillator for use with an external capacitor and two resistors, output control logic, and a special power-on reset circuit. The counter divides the oscillator frequency by any of 4 digitally controlled division ratios.

FEATURES

*Operates at 2^n frequency divider or as single transition timer
*Increments on positive edge clock transitions
*Wide supply voltage range: 3.0V ~ 15V
*Built-in low power RC oscillator
*Oscillator frequency range ~ DC to 100 kHz
*External clock applied to Pin 3 can be used instead of oscillator
*Available division ratios 2^8, 2^{10}, 2^{13}, or 2^{16}
*High noise immunity: 0.45 V_{DD} (typ.)
*Master reset totally independent of automatic reset operation
*Automatic reset initializes all counters when power turns on
*Q/$\overline{Q}$ select provides output logic level flexibility
*High output drive min. one TTL load
*Maximum input leakage 1 μA at 15V over full temperature range

PIN CONFIGURATION



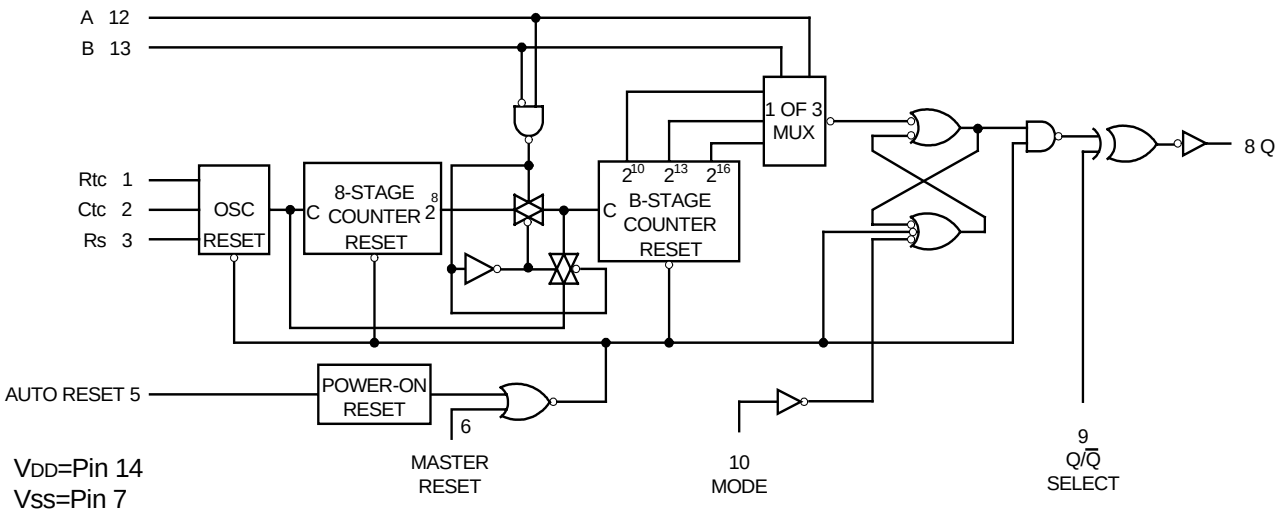
TRUTH TABLE

PIN	STATE	
	0	1
5	Auto Reset Operating	Auto Reset Disabled
6	Timer Operational	Master Reset On
9	Output Initially Low after Reset	Output Initially High after Reset
10	Single Cycle Mode	Recycle Mode

DIVISION RATIO TABLE

A	B	Number of Counter Stages n	Count 2^n
0	0	13	8192
0	1	10	1024
1	0	8	256
1	1	16	65536

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Note 1, 2)

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage		V_{DD}	-0.5 ~ +18	V
Input Voltage		V_{IN}	-0.5 ~ V_{DD}+0.5	V
Power Dissipation	DIP-14	P_D	700	mW
	SOP-14		500	
Lead Temperature (soldering, 10 seconds)		T_L	260	℃
Storage Temperature Range		T_{stg}	-65 ~ +150	℃

RECOMMENDED OPERATING CONDITIONS

(Note 2)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	3 ~ 15	V
Input Voltage	V_{IN}	0 ~ V_{DD}	V
Operating Temperature Range	T_{opr}	-40 ~ +85	℃

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS}=0V unless otherwise specified.

DC ELECTRICAL CHARACTERISTICS

(Note 2, Ta=25℃, unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Quiescent Device Current	I_{DD}	V_{DD}=5V, V_{IN}=V_{DD} or Vss		0.005	20	μA
		V_{DD}=10V, V_{IN}=V_{DD} or Vss		0.010	40	
		V_{DD}=15V, V_{IN}=V_{DD} or Vss		0.015	80	
LOW Level Output Voltage	V_{OL}	V_{DD}=5V		0	0.05	V
		V_{DD}=10V, I I_O I<1 μA		0	0.05	
		V_{DD}=15V		0	0.05	
HIGH Level Output Voltage	V_{OH}	V_{DD}=5V	4.95	5		V
		V_{DD}=10V, I I_O I<1 μA	9.95	10		
		V_{DD}=15V	14.95	15		
LOW Level Input Voltage	V_{IL}	V_{DD}=5V, Vo=0.5V or 4.5V		2	1.5	V
		V_{DD}=10V, Vo=1.0V or 9.0V		4	3.0	
		V_{DD}=15V, Vo=1.5V or 13.5V		6	4.0	
HIGH Level Input Voltage	V_{IH}	V_{DD}=5V, Vo=0.5V or 4.5V	3.5	3		V
		VDD=10V, Vo=1.0V or 9.0V	7.0	6		
		V_{DD}=15V, Vo=1.5V or 13.5V	11.0	9		
LOW Level Output Current (Note 3)	I_{OL}	V_{DD}=5V, Vo=0.4V	1.96	3.6		mA
		V_{DD}=10V, Vo=0.5V	2.66	9.0		
		V_{DD}=15V, Vo=1.5V	10.4	34.0		
HIGH Level Output Current (Note 3)	I_{OH}	V_{DD}=5V, Vo=2.5V	4.27	130		mA
		V_{DD}=10V, Vo=9.5V	2.25	8.0		
		V_{DD}=15V, Vo=13.5V	8.8	30.0		
Input Current	I_{IN}	V_{DD}=15V, V_{IN}=0V		-10^{-5}	-0.3	μA
		V_{DD}=15V, V_{IN}=15V		10^{-5}	0.3	

Note 3: I_{OH} and I_{OL} are tested one output at a time.

AC ELECTRICAL CHARACTERISTICS

(Note 4, Ta=25°C, CL=50pF (refer to test circuits))

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Rise Time	t_{TLH}	V_{DD}=5V V_{DD}=10V V_{DD}=15V		50 30 25	200 100 80	ns
Output Fall Time	t_{THL}	V_{DD}=5V V_{DD}=10V V_{DD}=15V		50 30 25	200 100 80	ns
Turn-Off, Turn-On Propagation Delay, Clock to Q (2^8 Output)	t_{PLH}, t_{PHL}	V_{DD}=5V V_{DD}=10V V_{DD}=15V		1.8 0.6 0.4	4.0 1.5 1.0	μs
Turn-On, Turn-Off Propagation Delay, Clock to Q (2^{16} Output)	t_{PHL}, t_{PLH}	V_{DD}=5V V_{DD}=10V V_{DD}=15V		3.2 1.5 1.0	8.0 3.0 2.0	μs
Clock Pulse Width	$t_{WH(CL)}$	V_{DD}=5V V_{DD}=10V V_{DD}=15V	400 200 150	200 100 70		ns
Clock Pulse Frequency	f_{CL}	V_{DD}=5V V_{DD}=10V V_{DD}=15V		2.5 6.0 8.5	1.0 3.0 4.0	MHz
MR Pulse Width	$t_{WH(R)}$	V_{DD}=5V V_{DD}=10V V_{DD}=15V	400 200 150	170 75 50		ns
Average Input Capacitance	C_I	Any Input		5.0	7.5	pF
Power Dissipation Capacitance (Note 5)	C_{PD}			100		pF

Note 4: AC Parameters are guaranteed by DC correlated testing.

Note 5: C_{PD} determines the no load AC power consumption of any CMOS device.

OPERATING CHARACTERISTICS

With Auto Reset pin set to a “0” the counter circuit is initialized by turning on power. Or with power already on, the counter circuit is reset when the Master Reset pin is set to a “1”. Both types of reset will result in synchronously resetting all counter stages independent of counter state.

The RC oscillator frequency is determined by the external RC network, i.e.:

$$f=\frac{1}{2.3\ RtcCtc} \text{ if } (1\ kHz \leqq f \leqq 100kHz)$$

and RS ~ 2 Rtc where RS≧10 kΩ

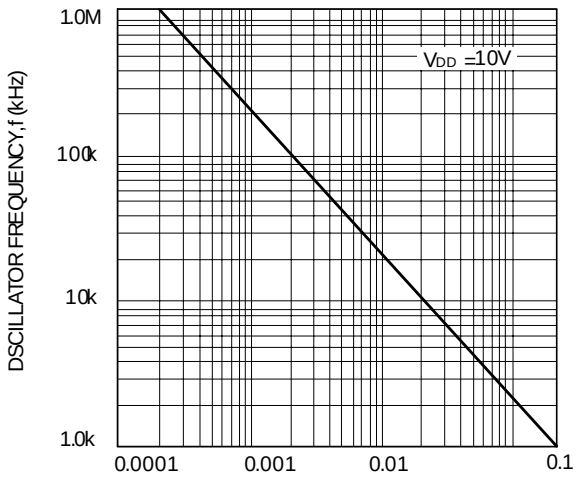
The time select inputs (A and B) provide a two-bit address to output any one of four counter stages (2^8, 2^{10}, 2^{13}, and 2^{16}). The 2^n counts as shown in the Division Ratio Table represent the Q output of the Nth stage of the counter. When A is “1”, 2^{16} is selected for both states of B.

However, when B is “0”, normal counting is interrupted and the 9th counter stage receives its clock directly from the oscillator (i.e., effectively outputting 2^8).

The Q/$\overline{Q}$ select output control pin provides for a choice of output level. When the counter is in a reset condition and Q/Q select pin is set to a “0” the Q output is a “0”. Correspondingly, when Q/Q select pin is set to a “1” the Q output is a “1”.

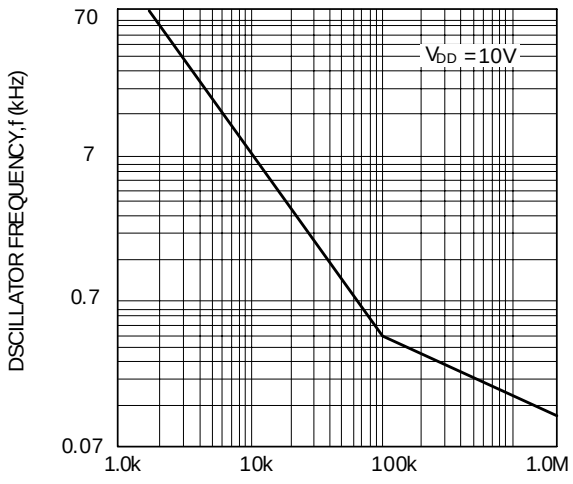
When the mode control pin is set to a “1”, the selected count is continually transmitted to the output. But, with mode pin “0” and after a reset condition the RS flip-flop resets (see Logic Diagram), counting commences and after 2^{n-1} counts the RS flip-flop sets which causes the output to change state. Hence, after another 2^{n-1} counts the output will not change. Thus, a Master Reset pulse must be applied or a change in the mode pin level is required to reset the single cycle operation.

RC Oscillator Frequency as a Function of R_{TC} and C



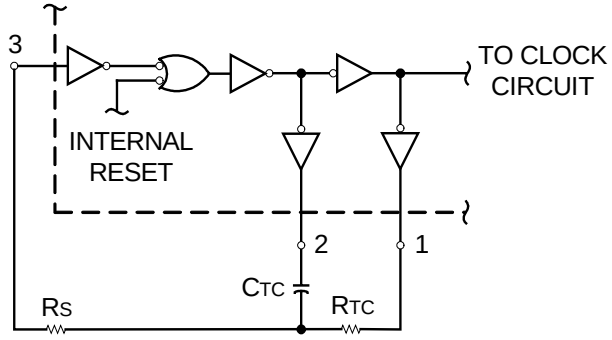
f as a function of C and (R_{TC} =56 KΩ, Rs =120k)

RC Oscillator Frequency as a Function of R_{TC} and C



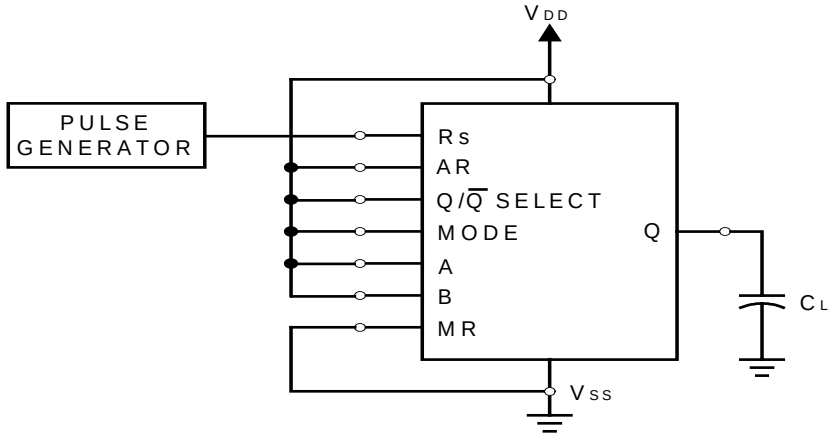
f as a function of R_{TC} and (C=100pF, Rs=2R_{TC})

Oscillator Circuit Using RC Configuration

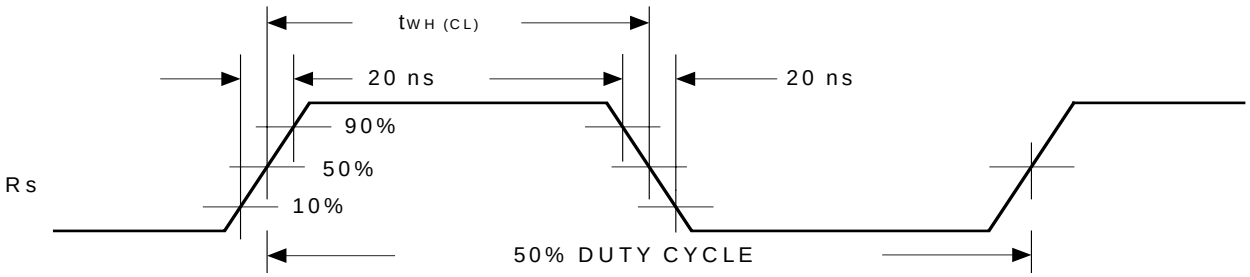


TEST CIRCUIT AND WAVEFORMS

Power Dissipation Test Circuit and Waveforms



(Rtc and Ctc outputs are left open)



Switching Time Test Circuit and Waveforms