

UT54ACTS220

Clock and Wait-State Generation Circuit

FEATURES

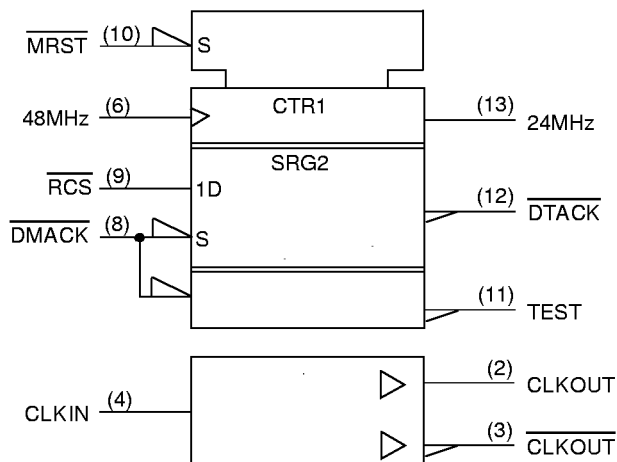
- 1.2 μ radiation-hardened CMOS
 - Latchup immune
- High speed
- Low power consumption
- Single 5-volt supply
- Available QML Q or V processes
- Flexible package
 - 14-pin DIP
 - 14-lead flatpack

DESCRIPTION

The UT54ACTS220 is designed to be a companion chip to UTMIC's UT69151 S μ MMIT family for the purpose of generating clock and wait-state signals. The device contains a divide by two circuit that accepts TTL input levels and drives CMOS output buffers. The chip accepts a 48MHz clock and generates a 24MHz clock. The 48MHz clock can have a duty cycle that varies by $\pm 20\%$. The UT54ACT220 generates a 24MHz clock with a $\pm 5\%$ duty cycle variation. The wait-state circuit generates a single wait-state by delaying the falling edge of $\overline{DTACK}$ into the S μ MMIT. The clock/timing device generates $\overline{DTACK}$ from the falling edge of input $\overline{RCS}$ which is synchronized by the falling edge of 24MHz. The S μ MMIT drives inputs $\overline{RCS}$ and $\overline{DMACK}$.

The devices are characterized over full military temperature range of -55°C to +125°C.

LOGIC SYMBOL

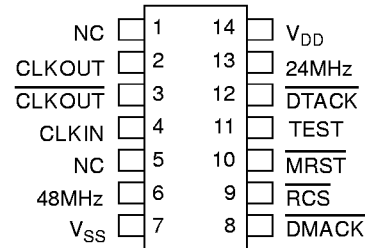


Note:

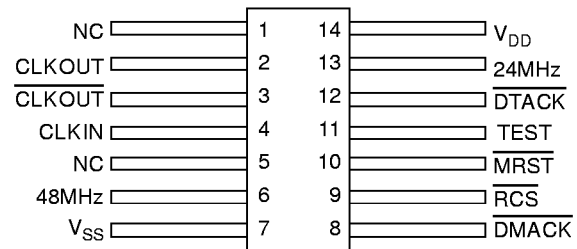
1. Logic symbol in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PINOUTS

14-Pin DIP
Top View



14-Lead Flatpack
Top View



PIN DESCRIPTION

Pin Number	Pin Name	Description
2	CLKOUT	Buffered version of CLKIN.
3	$\overline{\text{CLKOUT}}$	Inverted version of CLKIN.
4	CLKIN	Clock Input. This signal can be any arbitrary signal that the user wishes to buffer.
6	48MHz	48MHz Clock. The 24MHz clock is created by dividing this signal by two.
8	$\overline{\text{DMACK}}$	DMA Acknowledge. This input is generated by the S μ MMIT. When high, this signal will cause $\overline{\text{DTACK}}$ output to be forced high.
9	$\overline{\text{RCS}}$	RAM Chip Select. This input is generated by the S μ MMIT.
10	$\overline{\text{MRST}}$	Master Reset. This input can be used to preset 24MHz, $\overline{\text{DTACK}}$ and TEST. For normal operation tie $\overline{\text{MRST}}$ to V_{DD} through a resistor.
11	TEST	Test output signal.
12	$\overline{\text{DTACK}}$	Data Transfer Acknowledge. This signal can be used to drive the $\overline{\text{DTACK}}$ signal of the S μ MMIT if the user requires one wait state during the memory transfer.
13	24MHz	24MHz Clock. This output runs at half the frequency of the 48MHz input. The falling edge of 24MHz is the signal that latches the $\overline{\text{DTACK}}$ outputs. 24MHz is forced high whenever $\overline{\text{MRST}}$ is low. Properly loaded, 24MHz will have a 50% duty cycle $\pm 5\%$.

FUNCTIONAL TIMING: Single S μ MMIT Wait-State

For both read and write memory cycles, $\overline{\text{DTACK}}$ is an input to the S μ MMIT E and S μ MMIT LX/DXE. A non-wait state memory requires two clock cycles, T_1 and T_2 of figure 1. For accessing slower memory devices, the UT54ACTS220 holds $\overline{\text{DTACK}}$ to a logical "1". This results in the stretching of memory cycles by one clock to three clock cycles, T_W of figure 1. The S μ MMIT E and S μ MMIT LX/DXE samples the $\overline{\text{DTACK}}$ on the rising edge of the 24 MHz clock. If $\overline{\text{DTACK}}$ is not generated before the rising edge of the clock, the S μ MMIT E and S μ MMIT LX/DXE extends the memory cycle.

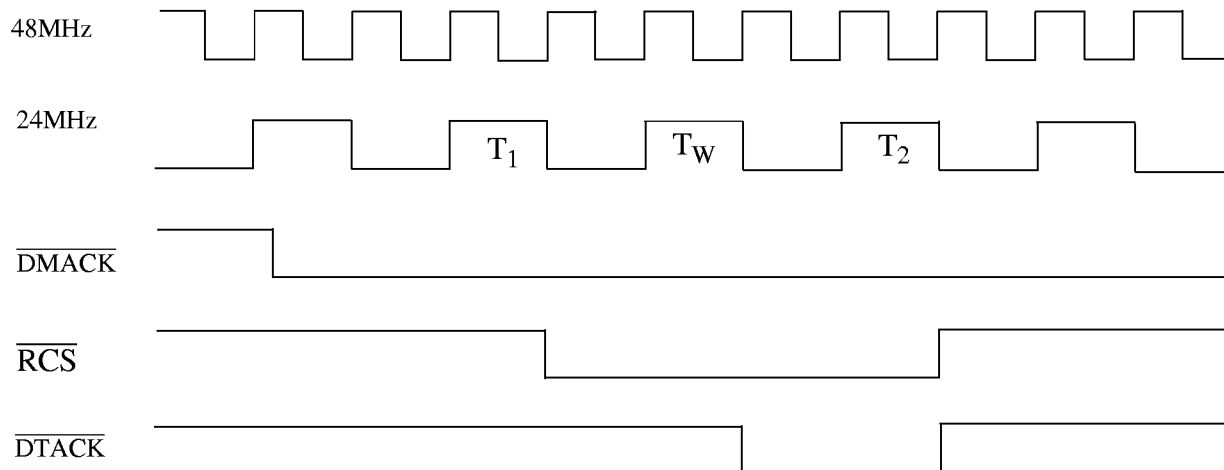
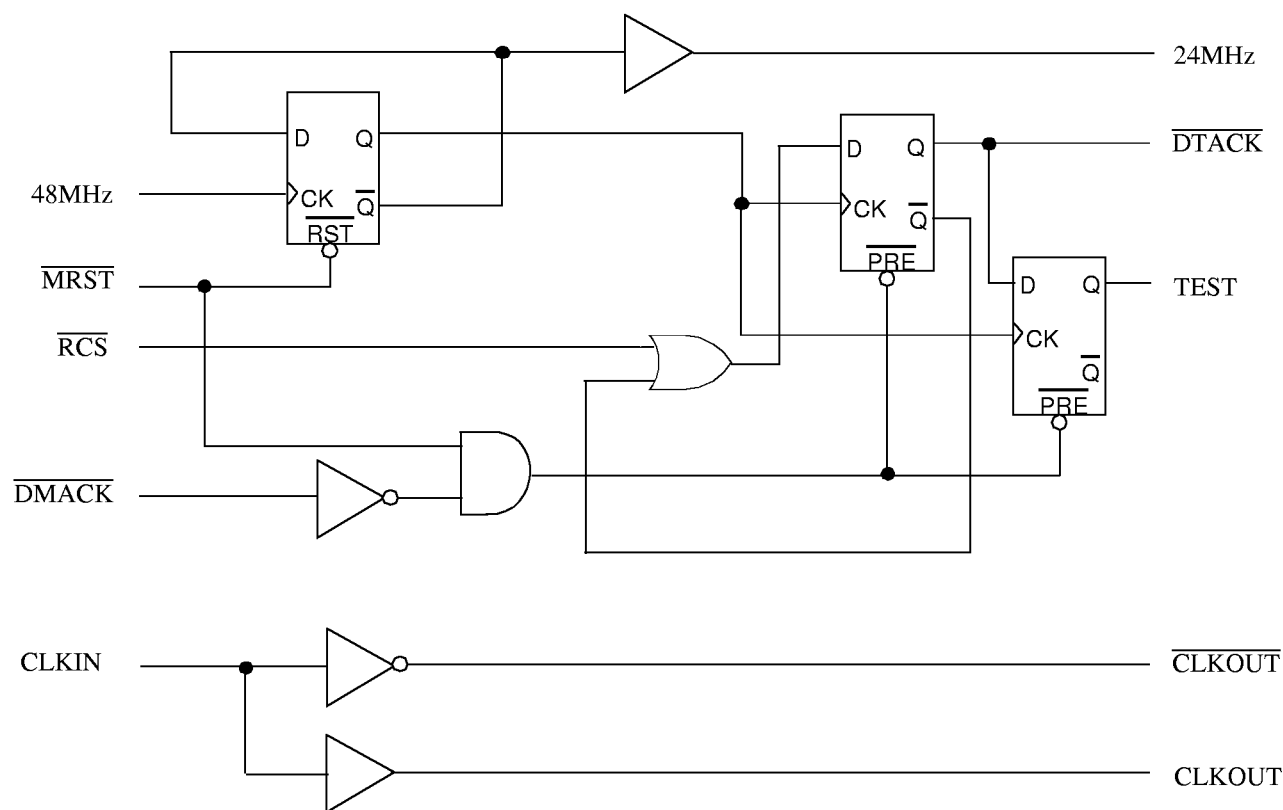


Figure 1. Functional Timing

LOGIC DIAGRAM



RADIATION HARDNESS SPECIFICATIONS ¹

PARAMETER	LIMIT	UNITS
Total Dose	1.0E6	rads(Si)
SEU Threshold ²	80	MeV-cm ² /mg
SEL Threshold	120	MeV-cm ² /mg
Neutron Fluence	1.0E14	n/cm ²

Notes:

1. Logic will not latchup during radiation exposure within the limits defined in the table.

2. Device storage elements are immune to SEU affects.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	LIMIT	UNITS
V _{DD}	Supply voltage	-0.3 to 7.0	V
V _{I/O}	Voltage any pin	-.3 to V _{DD} +.3	V
T _{STG}	Storage Temperature range	-65 to +150	°C
T _J	Maximum junction temperature	+175	°C
T _{LS}	Lead temperature (soldering 5 seconds)	+300	°C
Θ _{JC}	Thermal resistance junction to case	20	°C/W
I _I	DC input current	±10	mA
P _D	Maximum power dissipation	1	W

Note:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT	UNITS
V _{DD}	Supply voltage	4.5 to 5.5	V
V _{IN}	Input voltage any pin	0 to V _{DD}	V
T _C	Temperature range	-55 to +125	°C
48MHz	Duty Cycle	50 ± 20%	MHz

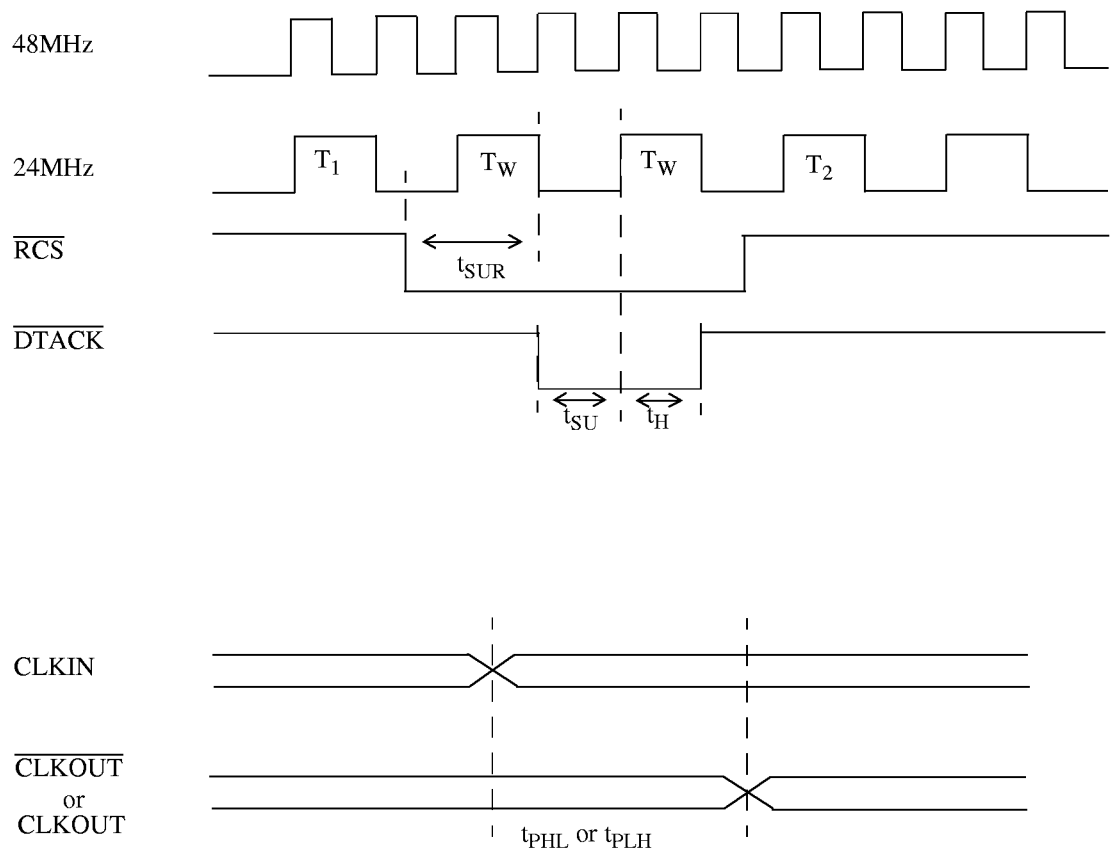
DC ELECTRICAL CHARACTERISTICS ⁷(V_{DD} = 5.0V ±10%; V_{SS} = 0V ⁶, -55°C < T_C < +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V _{IL}	Low-level input voltage ¹ TTL			0.8	V
V _{IH}	High-level input voltage ¹ TTL		.5V _{DD}		V
I _{IN}	Input leakage current TTL	V _{IN} = V _{DD} or V _{SS}	-1	1	μA
V _{OL1}	Low-level output voltage ³	I _{OL} = 8mA I _{OL} = 100μA		0.4 0.25	V
V _{OH1}	High-level output voltage ³	I _{OH} = -8mA I _{OH} = -100μA	.7V _{DD} V _{DD} -0.25		V
V _{OL2}	CLKOUT/ $\overline{\text{CLKOUT}}$ Low-level output voltage ³	I _{OL} = 12mA I _{OL} = 100μA		0.4 0.25	V
V _{OH2}	CLKOUT/ $\overline{\text{CLKOUT}}$ High-level output voltage ³	I _{OH} = -12mA I _{OH} = -100μA	.7V _{DD} V _{DD} -0.25		V
I _{OS}	Short-circuit output current ^{2,4}	V _O = V _{DD} and V _{SS}	-300	300	mA
I _{OL1}	Output current ¹⁰ (Sink)	V _{IN} = V _{DD} or V _{SS} V _{OL} = 0.4V	8		mA
I _{OH1}	Output current ¹⁰ (Source)	V _{IN} = V _{DD} or V _{SS} V _{OH} = V _{DD} - 0.4V	-8		mA
I _{OL2}	Output current ¹⁰ (Sink) CLKOUT/ $\overline{\text{CLKOUT}}$	V _{IN} = V _{DD} or V _{SS} V _{OL} = 0.4V	12		mA
I _{OH2}	Output current ¹⁰ (Source) CLKOUT/ $\overline{\text{CLKOUT}}$	V _{IN} = V _{DD} or V _{SS} V _{OH} = V _{DD} - 0.4V	-12		mA
P _{total}	Power dissipation ^{2, 8, 9}	C _L = 50pF		2.0	mW/ MHz
I _{DDQ}	Quiescent Supply Current	V _{DD} = 5.5V		10	μA
ΔI _{DDQ}	Quiescent Supply Current Delta	For input under test V _{IN} = V _{DD} - 2.1V For all other inputs V _{IN} = V _{DD} or V _{SS} V _{DD} = 5.5V		1.6	mA
C _{IN}	Input capacitance ⁵	f = 1MHz @ 0V		15	pF
C _{OUT}	Output capacitance ⁵	f = 1MHz @ 0V		15	pF

Notes:

1. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH(min)} + 20\%$, $- 0\%$; $V_{IL} = V_{IL(max)} + 0\%$, $- 50\%$, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH(min)}$ and $V_{IL(max)}$.
2. Supplied as a design limit but not guaranteed or tested.
3. Per MIL-PRF-38535, for current density $\leq 5.0E5$ amps/cm², the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF/MHz.
4. Not more than one output may be shorted at a time for maximum duration of one second.
5. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
6. Maximum allowable relative shift equals 50mV.
7. All specifications valid for radiation dose $\leq 1E6$ rads(Si).
8. Power does not include power contribution of any TTL output sink current.
9. Power dissipation specified per switching output.
10. This value is guaranteed based on characterization data, but not tested.

AC ELECTRICAL DIAGRAM



AC ELECTRICAL CHARACTERISTICS ²(V_{DD} = 5.0V ±10%; V_{SS} = 0V 1, -55°C < T_C < +125°C)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t _{PHL}	48MHz ↑ to 24MHz ↓	0	15	ns
t _{PLH}	48MHz ↑ to 24MHz ↑	0	15	ns
t _{PHL}	24MHz ↓ to $\overline{\text{DTACK}}$ ↓	0	7	ns
t _{PLH}	24MHz ↓ to $\overline{\text{DTACK}}$ ↑	0	6	ns
t _{PLH}	$\overline{\text{DMACK}}$ ↑ to $\overline{\text{DTACK}}$ ↑	3	16	ns
t _{PLH}	$\overline{\text{MRST}}$ ↓ to 24MHz, $\overline{\text{DTACK}}$ ↑	3	16	ns
t _{PHL}	CLKIN ↓ to CLKOUT ↓	0	11	ns
t _{PLH}	CLKIN ↑ to CLKOUT ↑	0	11	ns
t _{PHL}	CLKIN ↑ to $\overline{\text{CLKOUT}}$ ↓	0	11	ns
t _{PLH}	CLKIN ↓ to $\overline{\text{CLKOUT}}$ ↑	0	11	ns
t _{SU} ³	$\overline{\text{DTACK}}$ ↓ to 24MHz ↑	12		ns
t _H ³	24MHz ↑ to $\overline{\text{DTACK}}$ ↑	20		ns
t _{SUR}	Setup time from $\overline{\text{RCS}}$ ↓ to 24MHz ↓	7		ns
t _{WM}	$\overline{\text{MRST}}$ pulse width	5		ns
t _{WC}	CLKIN pulse width	12		ns
f _{MAX}	CLKIN		40	MHz

Notes:

1. Maximum allowable relative shift equals 50mV.
2. All specifications valid for radiation dose ≤ 1E6 rads(Si).
3. Guaranteed by design but not tested.