

HD151012

8-bit Binary Programmable Counter with Synchronous Preset Enable

REJ03D0299-0200Z
 (Previous ADE-205-132 (Z))
 Preliminary
 Rev.2.00
 Jul.16.2004

Description

The HD151012 has 8-bit binary down counter and D-type Flip Flop. The counter can set up to max 256 counts and synchronous preset (\overline{SPE}) input can preset the data. When the count value is 0, the next clock pulse presets the data to invert the output. D-type Flip Flop takes the counter output as clock pulse, whose data is transferred to output at the rise edge. It is applied to generate AC signal for STN type liquid crystal and general-use divider.

Features

- High speed operation
 $t_{pd}(\text{CLK or } \overline{\text{CLK}} \text{ to Q}) = 35 \text{ ns (typ)}$
- High output current
 Fanout of 10 LS TTL Loads
- Wide operating voltage
 $V_{CC} = 2 \text{ to } 6 \text{ V}$
- Low supply current ($T_a = 25^\circ\text{C}$)
 $I_{CC}(\text{Static}) = 4 \mu\text{A (max)}$
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD151012TELL	TSSOP-16 pin	TTP-16DAV	T	ELL (2,000 pcs/reel)

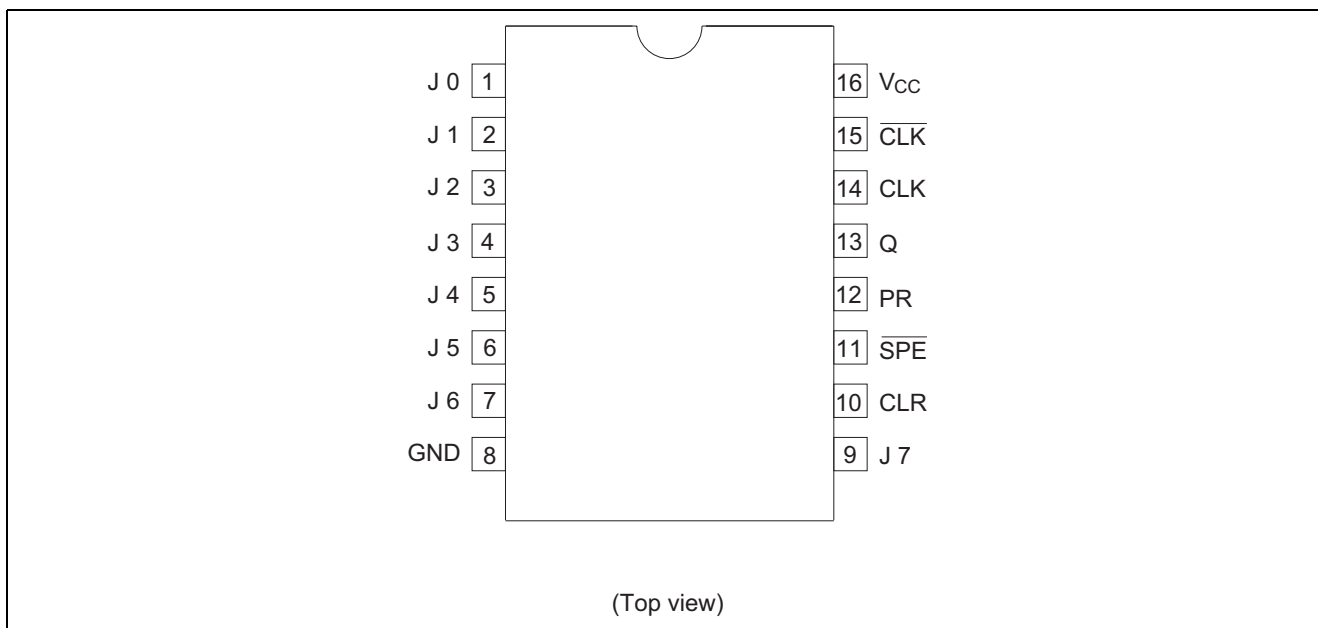
Function Table

Control Inputs			Mode	Operation Description
CLR	PR	\overline{SPE}		
H	H	H	Generally count	Down count at the rise edge of clock (CLK) Down count at the fall edge of clock (CLK)
X	X	L	Synchronous preset	Jn data is preset at the rise of clock (CLK), the fall of clock (CLK)
L	H	—	Initialize of Q output	Initialize of Q = "L"
H	L	—	Initialize of Q output	Initialize of Q = "H"

- Notes: 1. Synchronous preset (\overline{SPE}) input can set max 256 down counts.
 2. When the count value is 0, the next clock pulse presets the data to invert the output.
 3. CLR and PR inputs initialize output state.

H : High level
 L : Low level
 X : Immaterial
 — : Irrespective of condition

Pin Arrangement



Pin Description

Pin Name		Pin Description	
Input pins	J0 to J7	Count data input for option	
	CLK, CLK	Clock inputs	CLK : Rise edge trigger CLK : Fall edge trigger
	SPE	Preset input for Jn data	
	PR	Preset input for D-type Flip Flop (Initialize "L" at Q output)	
	CLR	Clear input for D-type Flip Flop (Initialize "H" at Q output)	
Output pins	Q	Output for D-type Flip Flop	

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	-0.5 to 7.0	V
Input / output voltage	V_{IN}/V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
VCC, GND current	I_{CC}, I_{GND}	±50	mA
Output current / pin	I_{OUT}	±25	mA
Power dissipation	P_T	500	mW
Storage temperature	T_{stg}	-65 to 150	°C
Input diode current	I_{IK}	±20	mA
Output diode current	I_{OK}	±20	mA

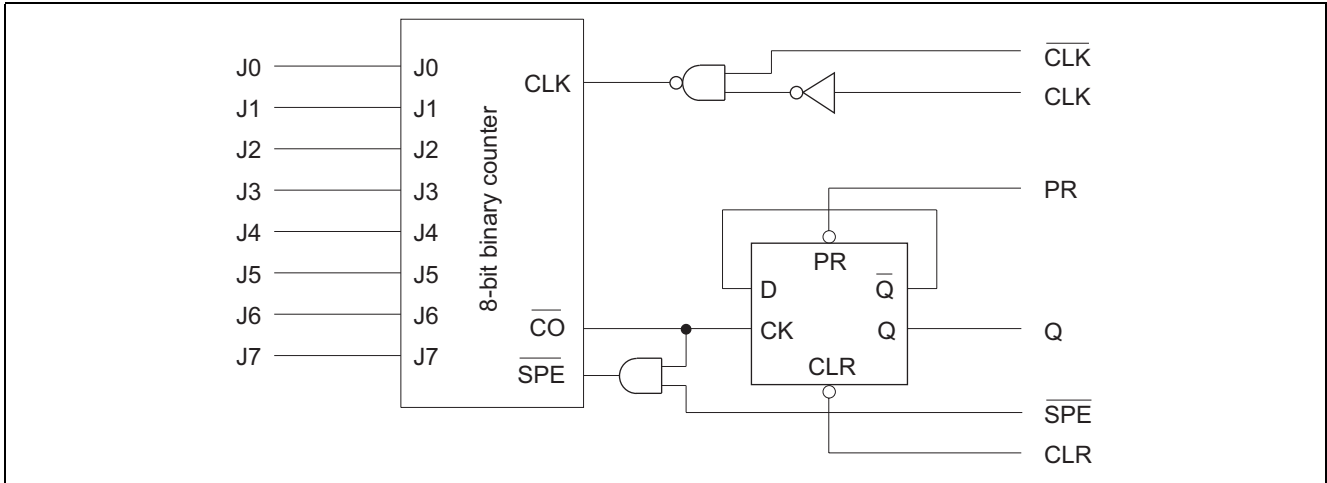
- Notes: 1. The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.
2. All voltage values except for differential input voltage are with respect to network ground terminal.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit	
Supply voltage	V_{CC}	2	—	6	V	
Input/output voltage	$V_{IN/OUT}$	0	—	V_{CC}	V	
Operating temperature	T_{opr}	-40	—	+85	°C	
Input rise/fall time*1	$V_{CC} = 2.5\text{ V}$	t_r, t_f	0	—	1000	ns
	$V_{CC} = 4.5\text{ V}$		0	—	500	
	$V_{CC} = 5.5\text{ V}$		0	—	400	

Note: 1. This item guarantees maximum limit when one input switches.

Logic Diagram



Electrical Characteristics

Item	Symbol	V _{CC}	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
High level input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V	J0 to J7 SPE PR, CLR	CLK, CLK
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
		2.0	1.5	—	—	1.5	—		J0 to J7 SPE PR, CLR	CLK, CLK
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
Low level input voltage	V _{IL}	2.0	—	—	0.5	—	0.5	V	J0 to J7 SPE PR, CLR	CLK, CLK
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
		2.0	—	—	0.5	—	0.5		J0 to J7 SPE PR, CLR	CLK, CLK
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
High level output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20 mA
		4.5	4.4	4.5	—	4.4	—			I _{OH} = -4 mA
		6.0	5.9	6.0	—	5.9	—			I _{OH} = -5.2 mA
		4.5	4.18	4.31	—	4.13	—			
		6.0	5.68	5.80	—	5.63	—			
Low level output voltage	V _{OL}	2.0	—	0.0	0.1	—	0.1	V	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20 mA
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	0.17	0.26	—	0.33			I _{OL} = 4 mA
		6.0	—	0.18	0.26	—	0.33			I _{OL} = 5.2 mA
Input capacitance	I _{IN}	6.0	—	—	±0.1	—	±1.0	mA	V _{IN} = V _{CC} or GND	
Supply current	I _{CC}	6.0	—	—	4.0	—	40.0	mA	V _{IN} = V _{CC} or GND	

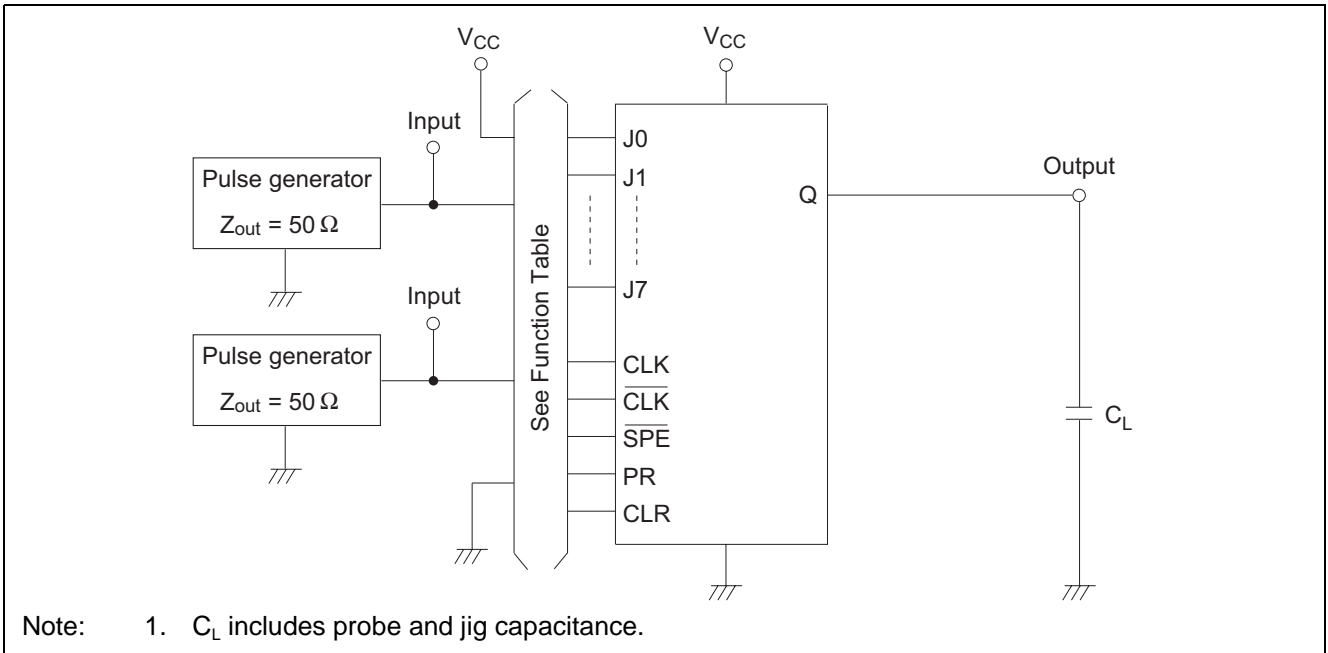
Switching Characteristics ($C_L = 50 \text{ pF}$, $t_r = t_f = 6 \text{ ns}$)

Item	Sym- bol	V_{CC}	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } 85^\circ\text{C}$		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	f_{max}	2.0	—	—	4	—	3	MHz	
		4.5	—	36	20	—	16		
		6.0	—	—	24	—	19		
Output rise/fall time	t_{TLH} t_{THL}	2.0	—	30	75	—	95	ns	
		4.5	—	8	15	—	19		
		6.0	—	7	13	—	16		
Propagation delay time	t_{PLH} t_{PHL}	2.0	—	—	300	—	380		CLK or $\overline{\text{CLK}}$ to Q
		4.5	—	35	60	—	75		
		6.0	—	—	53	—	65		
	t_{PLH} t_{PHL}	2.0	—	—	150	—	185		PR or CLR to Q
		4.5	—	18	30	—	38		
		6.0	—	—	25	—	32		
Pulse width (CLK, $\overline{\text{CLK}}$, PR, CLR)	tw	2.0	80	—	—	100	—	ns	
		4.5	16	—	—	20	—		
		6.0	14	—	—	17	—		
Setup time (Jn - CLK, $\overline{\text{CLK}}$) (SPE, CLK, $\overline{\text{CLK}}$)	ts	2.0	100	—	—	125	—	ns	
		4.5	20	—	—	25	—		
		6.0	17	—	—	21	—		
Hold time (Jn - CLK, $\overline{\text{CLK}}$) (SPE, CLK, $\overline{\text{CLK}}$)	th	2.0	15	—	—	15	—	ns	
		4.5	10	—	—	10	—		
		6.0	5	—	—	5	—		
Input capacitance	C_{IN}	—	—	5	10	—	10	pF	
Power dissipation capacitance*1	C_{PD}	—	—	48	—	—	—	pF	

Note: 1. CPD is equivalent capacitance inside of the IC calculated from the operating current without load (see test circuit). The average operating current without load is calculated according to the expression below.

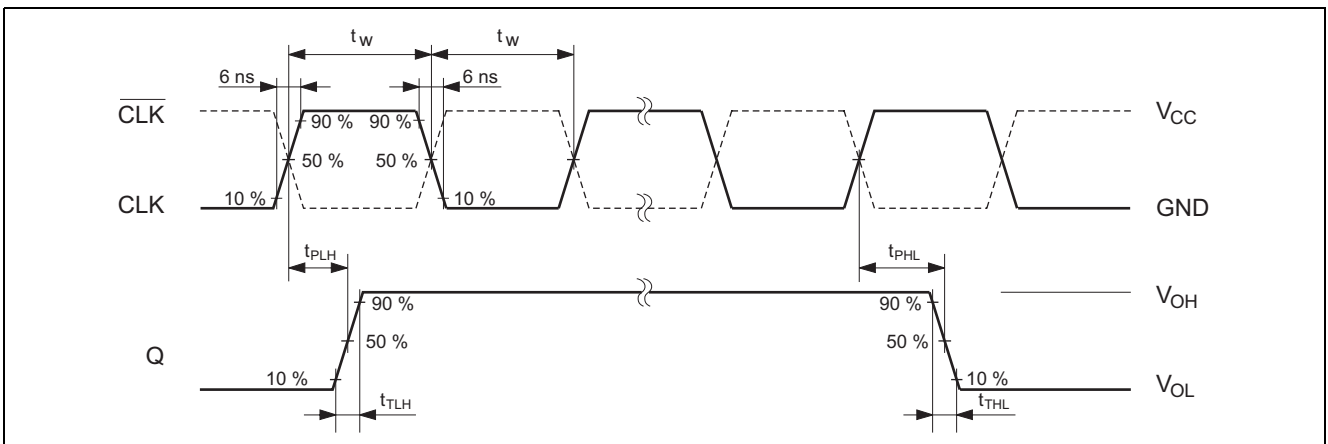
$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

Test Circuit

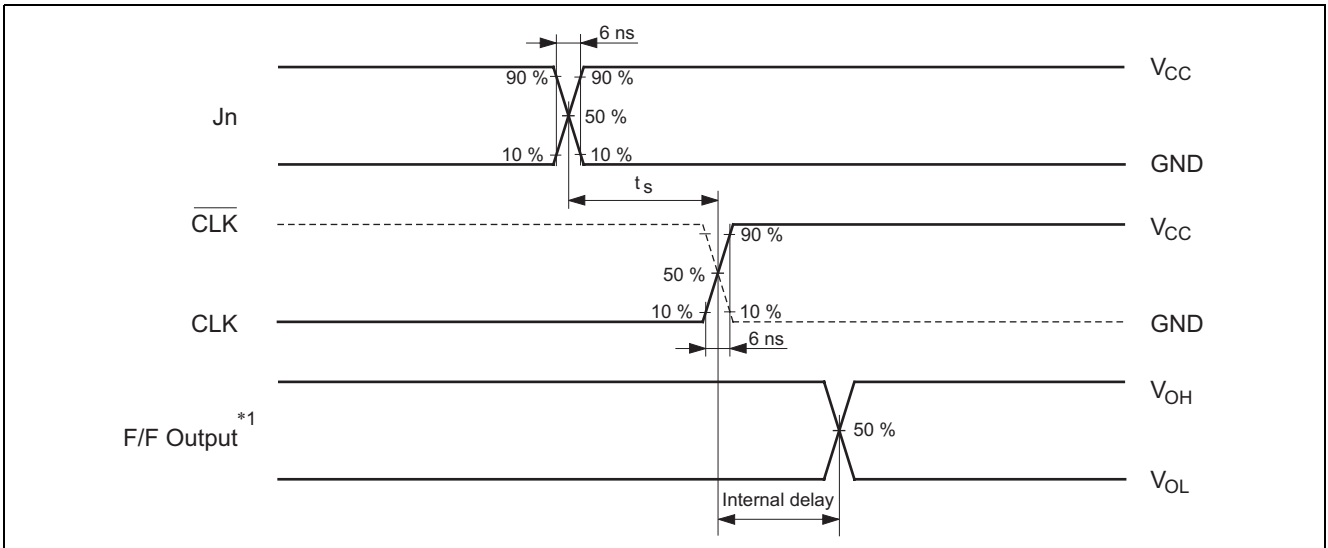


Note: 1. C_L includes probe and jig capacitance.

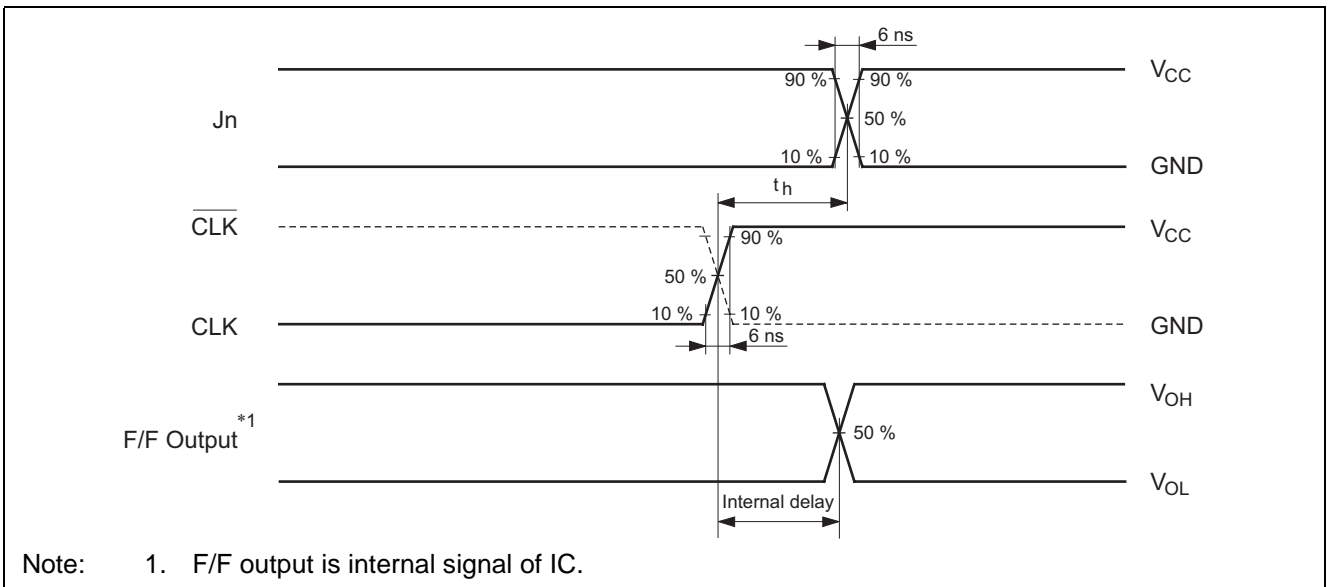
Waveforms – 1



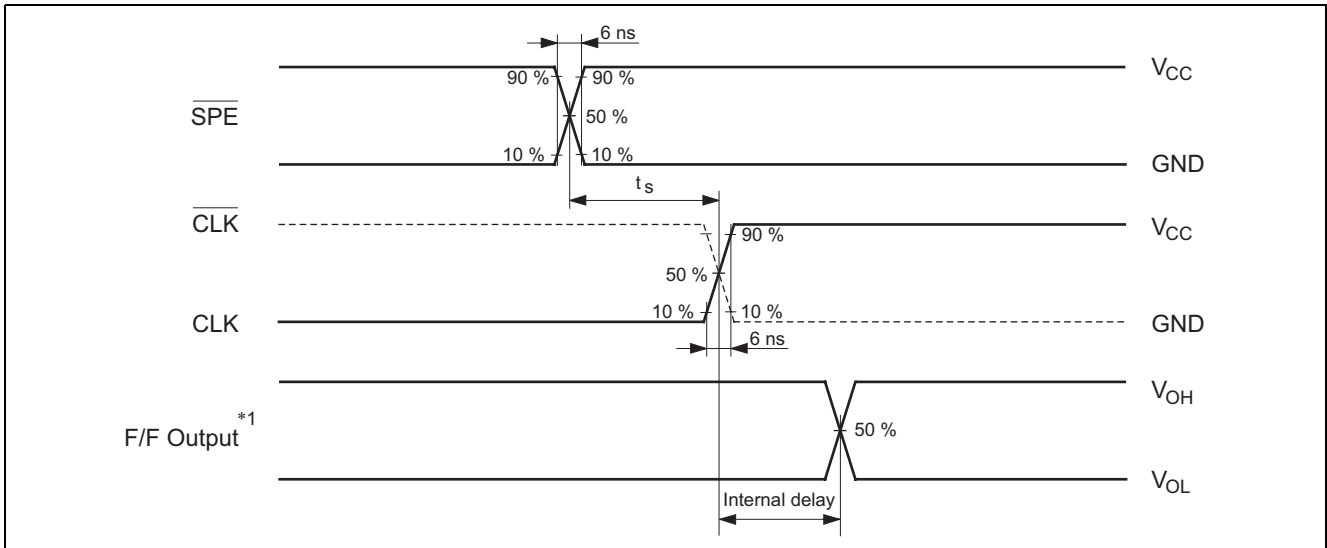
Waveforms – 2



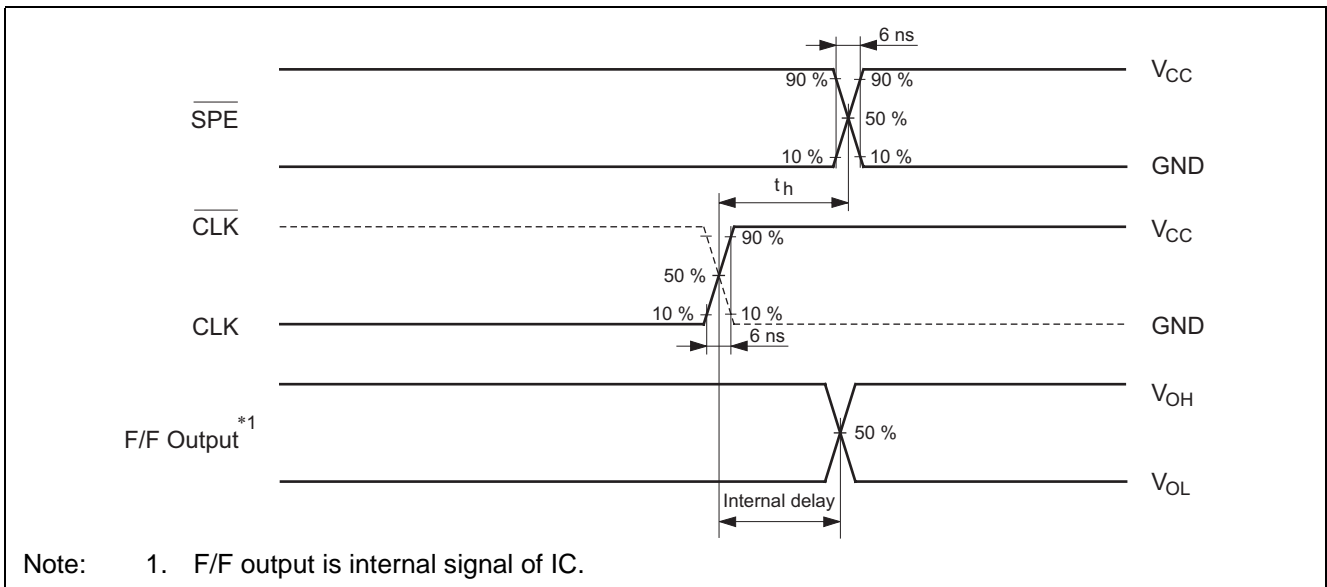
Waveforms – 3



Waveforms – 4

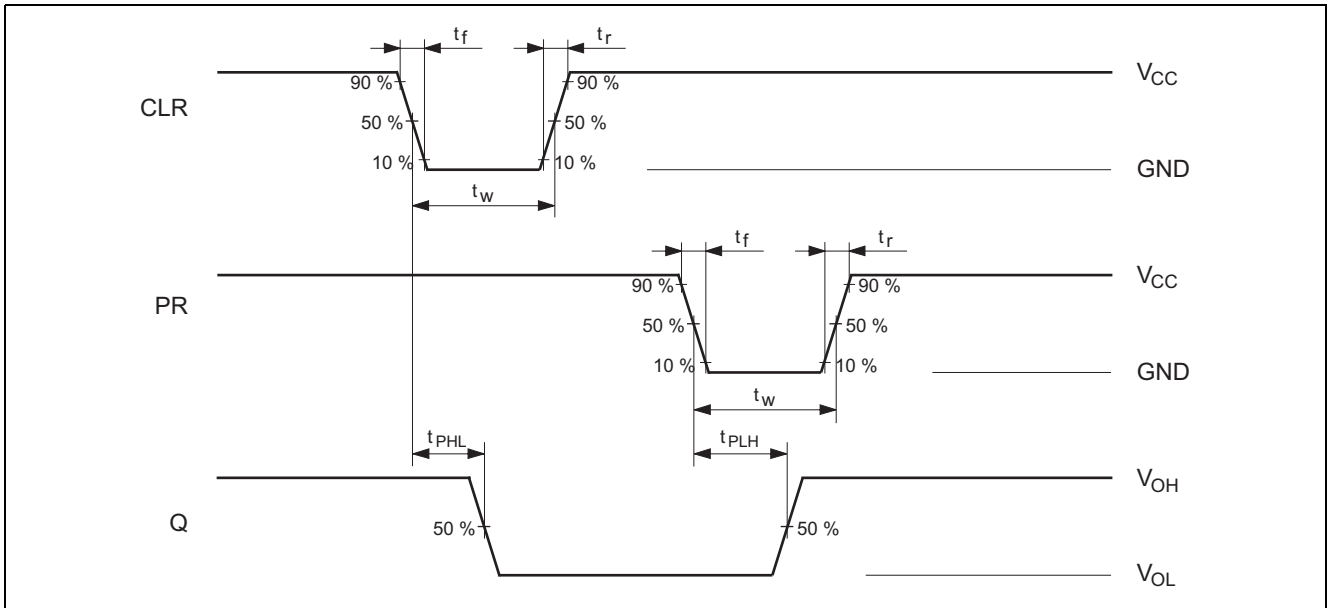


Waveforms – 5

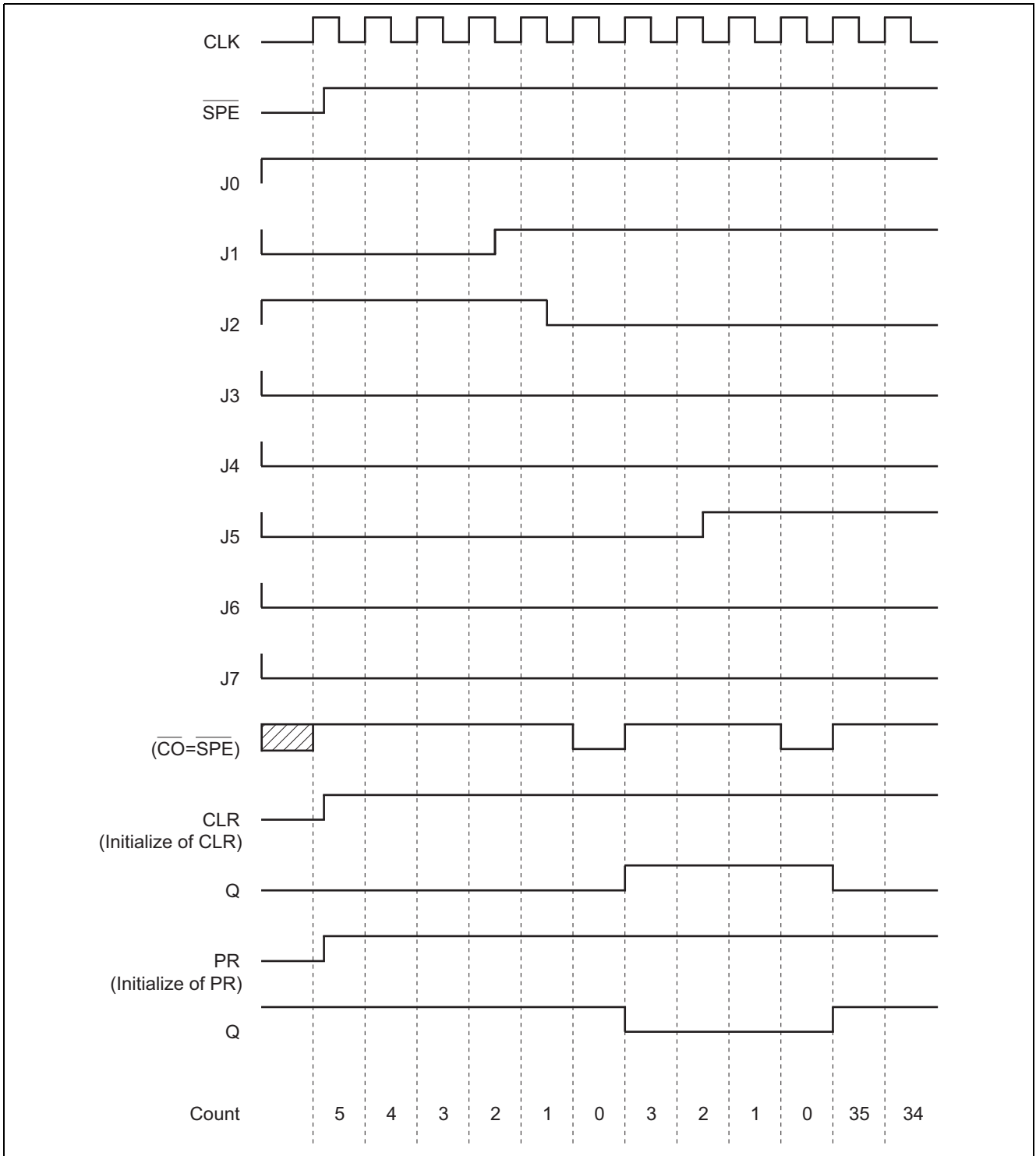


Note: 1. F/F output is internal signal of IC.

Waveforms – 6



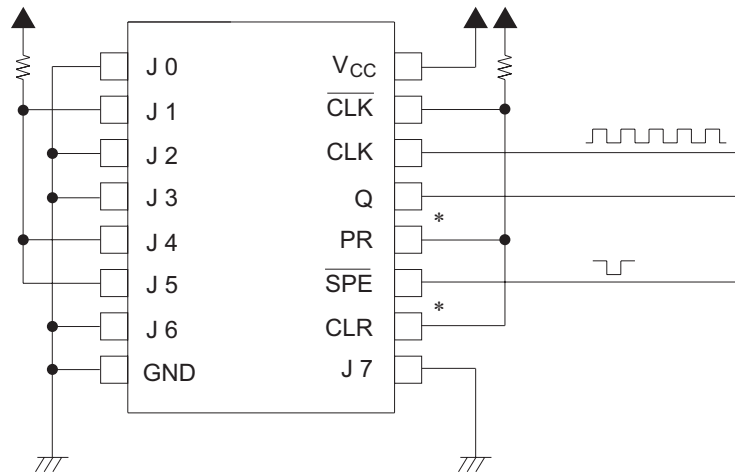
Timing Chart



Example of Application Circuit

AC Signal Generator for STN Type Liquid Crystal Panel

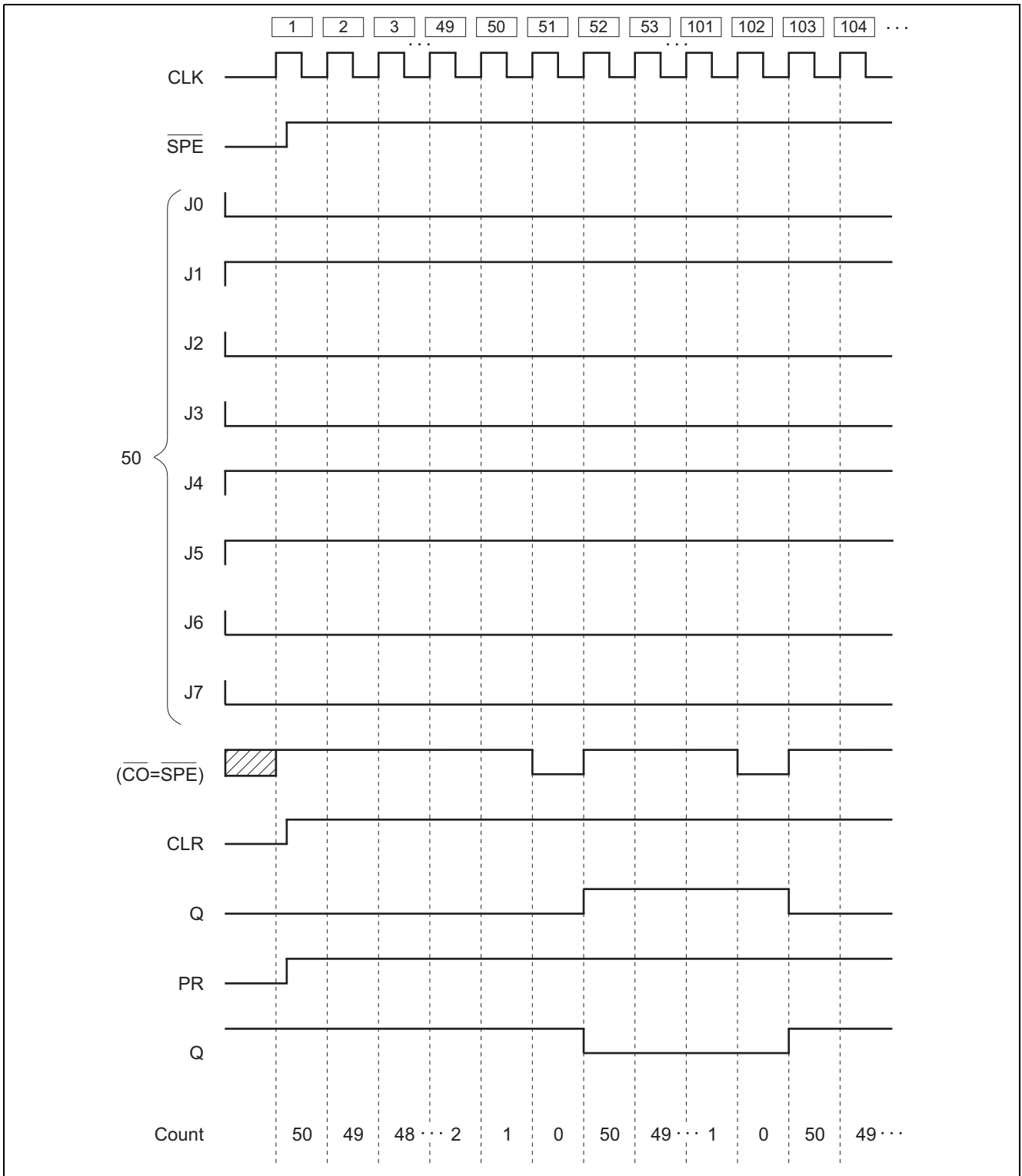
Initialize counter: 50



Note: When initializing output D-F/F apply "L"

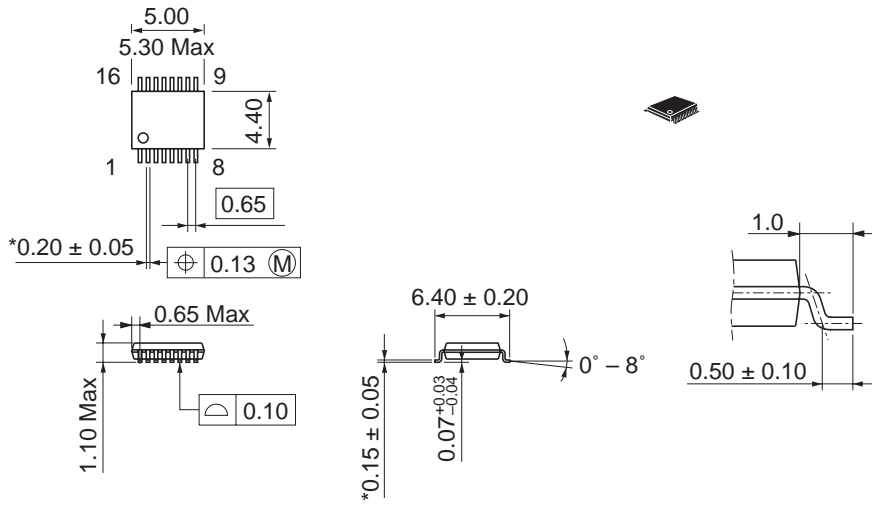
Timing Chart

Example of AC Signal Generator



Package Dimensions

As of January, 2003
Unit: mm



*Ni/Pd/Au plating

Package Code	TTP-16DAV
JEDEC	—
JEITA	—
Mass (reference value)	0.05 g

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
 2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
 3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
The information described here may contain technical inaccuracies or typographical errors.
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (<http://www.renesas.com>).
 4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
 5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
 6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
 7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
 8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.
-



RENESAS SALES OFFICES

<http://www.renesas.com>

Renesas Technology America, Inc.

450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500 Fax: <1> (408) 382-7501

Renesas Technology Europe Limited.

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, United Kingdom
Tel: <44> (1628) 585 100, Fax: <44> (1628) 585 900

Renesas Technology Europe GmbH

Dornacher Str. 3, D-85622 Feldkirchen, Germany
Tel: <49> (89) 380 70 0, Fax: <49> (89) 929 30 11

Renesas Technology Hong Kong Ltd.

7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2375-6836

Renesas Technology Taiwan Co., Ltd.

FL 10, #99, Fu-Hsing N. Rd., Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.

26/F., Ruijin Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.

1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001