

This application note is designed to inform the designer using the DM9008 about crystals use in the oscillator circuit.

The oscillator is controlled by a 20 MHz parallel resonant crystal connected between X1 and X2 or by an external oscillator circuit attached to pin X2 (When X2 is being driven by an external oscillator, X1 must be grounded). The 20 MHz output of the oscillator is divided by 2 to generate the 10 MHz transmit clock for the controller. The oscillator circuit also provides the internal clock signals to the encoding and decoding circuits.

The 20 MHz crystal connection to the DM9008 requires special attention. The IEEE 802.3 standard requires the transmitted signal frequency to be accurate within $\pm 0.01\%$. Stray capacitance can shift the crystal's frequency out of range and cause the transmitted frequency to exceed the $\pm 0.01\%$ tolerance. The frequency marked on the crystal is usually measured with a fixed load capacitance specified in the crystal's data sheet, typically 20pf.

In order to prevent distortion on the transmitted frequency, the total capacitance seen by the crystal should equal the total load capacitance. For a standard parallel setup, as shown in figure 1, the 2 load caps C1 and C2 should equal $2(C1)$ minus any stray capacitances. $2(C1)$ is equal to the specific load capacity acting in series. Thus the trim capacitors required can be calculated as follows:

$$C1 = 2 \times C1 - (Cb1 + Cd1), \text{ where } Cb1 = \text{Board capacitance on X1 and } Cd1 = \text{X1 device capacitance.}$$

$$C2 = 2 \times C2 - (Cb2 + Cd2), \text{ where } Cb2 = \text{Board capacitance on X2 and } Cd2 = \text{X2 device capacitance.}$$

The values of the device capacitance on pins X1 and X2 are in the region of 5pf.

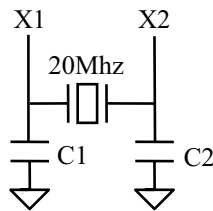


Figure 1

Crystal Specifications

Resonant Frequency	20 MHz
Tolerance	$\pm 0.01\%$ at 25° C
Stability	$\pm 0.0005\%$ through 0° C to 70° C
Type	AT Cut
Circuit	Parallel Resonance
Max. ESR	20Ω
Crystal Load Capacitance	20pf