CS5233-3

500 mA and 1.5 A, 3.3 V Dual Input Linear Regulator with Auxiliary Control

The CS5233–3 provides a glitch–free 3.3 V output from one of three possible supplies, (V_{IN}, V_{SB} and 3.3 V_{AUX}). An on–chip linear regulator powers the output when either V_{IN} or V_{SB} is available. Otherwise AuxDrv turns on an external PFET, which connects the 3.3 V_{AUX} supply to the output. The CS5233–3 is intended to provide power to an ASIC on a PCI Network Interface Card (NIC), and meets Intel's "Instantly Available" power requirements which follow from the Advanced Configuration and Power Interface (ACPI) standards. Other applications include desktop computers, power supplies with multiple input sources, and PCMCIA interface cards.

The CS5233–3 linear regulator provides a fixed 3.3 V output at up to 1.5 A with an overall accuracy of ±2%. The internal NPN–PNP composite pass transistor provides a low dropout voltage and requires less supply current than a straight PNP design. Full protection with both current limit and thermal shutdown is provided. Designed for low reverse current, the IC prevents excessive current from flowing from V_{OUT} to either V_{IN} or ground when the regulator input voltage is lower than the output. The auxiliary drive control feature allows the use of an external PFET to supply power to the output when the regulator supplies are off.

The CS5233–3 regulator is available in two package types: the 5 Lead D^2PAK package (TO–263) and 8 Lead SOIC with 4 Lead Fused (DF8) package. When powered from the V_{IN} source, the D^2PAK is rated for 1.5 A and the 8 Lead SOIC is rated for 500 mA. Both packages are rated for 500 mA when only powered from the V_{SB} source.

Features

- Linear Regulator
  - 3.3 V ± 2% Output Voltage
  - Current Limit
  - Thermal Shutdown with Hysteresis
  - 400 μA Reverse Current
  - ESD Protected
- System Power Management
  - Auxiliary Supply Control
  - "Glitch Free" Transition Between 3 Sources
  - Similar to CS5231–3
- High Output Current Capability
  - 1.5 A D^2PAK
  - 500 mA 8 Lead SOIC DF8
- Internally Fused Leads in SO–8 Package

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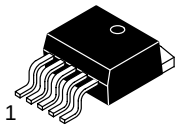
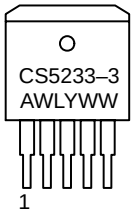


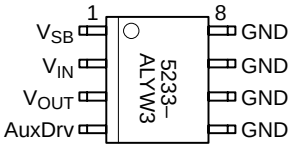
D^2PAK
5–PIN
DP SUFFIX
CASE 936F

SO–8
D SUFFIX
CASE 751

PIN CONNECTIONS AND MARKING DIAGRAMS



Pin 1. V_{SB}
2. V_{IN}
3. GND
4. V_{OUT}
5. AuxDrv



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
CS5233–3GDP5	D^2PAK	50 Units/Rail
CS5233–3GDPR5	D^2PAK	750 Tape & Reel
CS5233–3GDF8	SO–8	95 Units/Rail
CS5233–3GDFR8	SO–8	2500 Tape & Reel

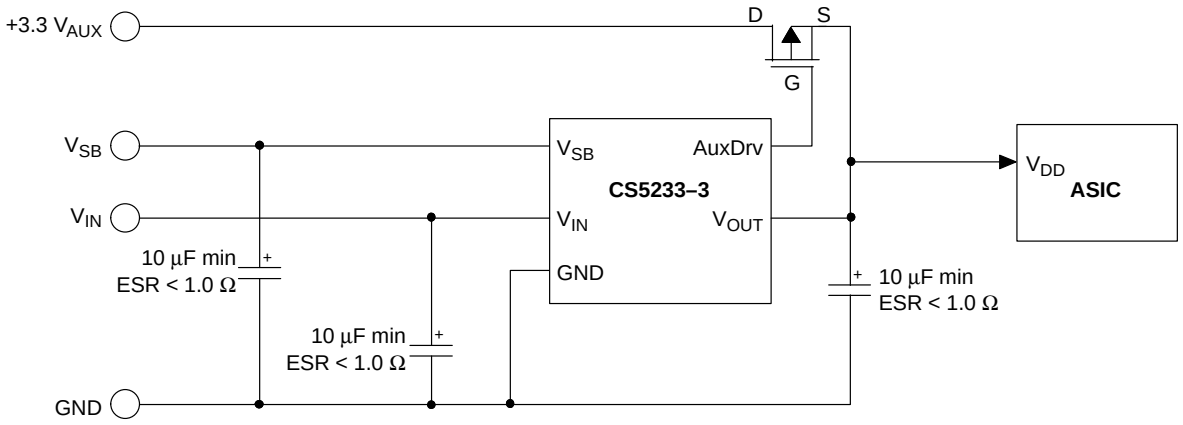


Figure 1. Application Diagram, 5.0 V to 3.3 V Dual Input Regulator with Auxiliary PFET Power Switch

ABSOLUTE MAXIMUM RATINGS*

Rating		Value	Unit
Operating Junction Temperature		150	°C
Lead Temperature Soldering:	Reflow: (SMD styles only) (Note 1.)	230 peak	°C
Storage Temperature Range		–65 to +150	°C
ESD Susceptibility (Human Body Model)		2.0	kV

1. 60 second maximum above 183°C.

*The maximum package power dissipation must be observed.

ABSOLUTE MAXIMUM RATINGS

Pin Name	Pin Symbol	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
IC Power Input (Main)	V_{IN}	6.0 V	–0.3 V	100 mA	Internally Limited
IC Power Input (Standby)	V_{SB}	6.0 V	–0.3 V	100 mA	Internally Limited
Output Voltage	V_{OUT}	6.0 V	–0.3 V	Internally Limited	100 mA
Auxiliary Drive Output	AuxDrv	6.0 V	–0.3 V	10 mA	50 mA
IC Ground	GND	N/A	N/A	N/A	N/A

ELECTRICAL CHARACTERISTICS

($0°C < T_A < 70°C$; $0°C < T_J < 150°C$; $4.75\ V < V_{IN}$; $V_{SB} < 6.0\ V$; $C_{OUT} \geq 10\ \mu F$ with ESR < 1.0 Ω, I_{OUT} = 10 mA; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Linear Regulator					
Output Voltage	10 mA < I_{OUT} < I_{MAX}. Note 2.	3.234 – 2%	3.3	3.366 + 2%	V
Line Regulation	I_{OUT} = 10mA; V_{SOURCE} = 4.75 V to 6.0 V. Note 3.	–	1.0	5.0	mV
Load Regulation	V_{SOURCE} = 5.0 V; I_{OUT} = 10 mA to I_{MAX}. Note 2. Note 3.	–	5.0	15	mV

2. I_{MAX} = 1.5 A for D^2PAK only and with V_{IN} > 4.75 V, otherwise I_{MAX} = 500 mA.
3. Applies to either V_{IN} or V_{SB}.

ELECTRICAL CHARACTERISTICS (continued) ($0°C < T_A < 70°C$; $0°C < T_J < 150°C$; $4.75\ V < V_{IN}$; $V_{SB} < 6.0\ V$; $C_{OUT} \geq 10\ \mu F$ with ESR < 1.0 Ω, I_{OUT} = 10 mA; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Linear Regulator					
Ground Current	I_{OUT} = 10 mA I_{OUT} = 500 mA I_{OUT} = 1.5 A. Note 4.	– – –	2.0 3.0 9.0	3.0 6.0 20	mA mA mA
Reverse Current	V_{SOURCE} = 0 V; V_{OUT} = 3.3 V. Note 4.	–	0.4	1.0	mA
Current Limit V_{IN} Input 8 Lead SOIC 5 Lead D^2PAK	 $0\ V < V_{OUT} < 3.2\ V$ $V_{IN} > 4.25\ V$	 0.55 1.6	 0.8 2.4	 1.3 4.5	 A A
Current Limit V_{SB} Input Either Package	$0\ V < V_{OUT} < 3.2\ V$; $V_{IN} < 4.25\ V$; $V_{SB} > 4.25\ V$	0.55	0.8	1.3	A
Thermal Shutdown	Note 5.	150	180	210	°C
Thermal Shutdown Hysteresis	Note 5.	–	25	–	°C
Auxiliary Drive					
V_{IN} Turn–On Threshold	V_{SB} = 0 V; Ramp V_{IN} up until AuxDrv goes high and regulator turns on	4.35	4.5	4.65	V
V_{IN} Turn–Off Threshold	V_{SB} = 0 V; Ramp V_{IN} down until AuxDrv goes low and regulator turns off	4.25	4.4	4.55	V
V_{SB} Turn–On Threshold	V_{SB} = 0 V; Ramp V_{SB} up until AuxDrv goes high and regulator turns on	4.35	4.5	4.65	V
V_{SB} Turn–Off Threshold	V_{SB} = 0 V; Ramp V_{SV} down until AuxDrv goes low and regulator turns off	4.25	4.4	4.55	V
Threshold Hysteresis	–	75	100	125	mV
AuxDrv Peak Voltage	V_{OUT} = 0 V; $0\ V < V_{SOURCE} < 2.0\ V$. Note 4. V_{OUT} = 0 V; I_{AuxDrv} = 100 μA; $2.0\ V < V_{IN} < 4.25\ V$; $2.0\ V < V_{SB} < 4.25\ V$ V_{OUT} = 3.0 V; I_{AuxDrv} = 100 μA; $0\ V < V_{IN} < 4.25\ V$; $0\ V < V_{SB} < 4.25\ V$	– – –	0.4 0.1 0.1	1.8 0.4 0.4	V V V
AuxDrv High Voltage	V_{IN} or $V_{SB} > 4.65\ V$	3.75	4.0	–	V
AuxDrv Pin Current Limit	V_{AuxDrv} = 1.0 V; V_{SOURCE} = 4.0. Note 4.	0.5	6.0	25	mA
V_{AuxDrv} Turn–Off Response Time	Step V_{SOURCE} from 4.0 V to 5.0 V. Note 4. Note 5.	–	20	40	μs
V_{AuxDrv} Turn–On Response Time	Step V_{SOURCE} from 5.0 V to 4.0 V. Note 4. Note 5.	–	1.0	10	μs
Pull–Up Resistance	V_{IN} = 0 V and $V_{IN} > 4.7\ V$. Note 4. Note 5.	5.0	10	25	kΩ

4. Applies to either V_{IN} or V_{SB}.
5. Guaranteed by design, not 100% production tested.

PACKAGE PIN DESCRIPTION

Package Lead #		Lead Symbol	Function
5 Lead D²PAK	8 Lead SO Narrow		
1	1	V_{SB}	Standby 5.0 V input voltage.
2	2	V_{IN}	5.0 V Main input voltage.
3, Tab	5, 6, 7, 8	GND	Ground and IC substrate connection.
4	3	V_{OUT}	Regulated output voltage.
5	4	AuxDrv	Control voltage for the external PFET switched auxiliary supply. This pin drives low if V_{IN} and V_{SB} are less than 4.4 V (typical), otherwise it is pulled up to the greater of V_{IN} or V_{SB} through an internal diode and 10 kΩ resistor.

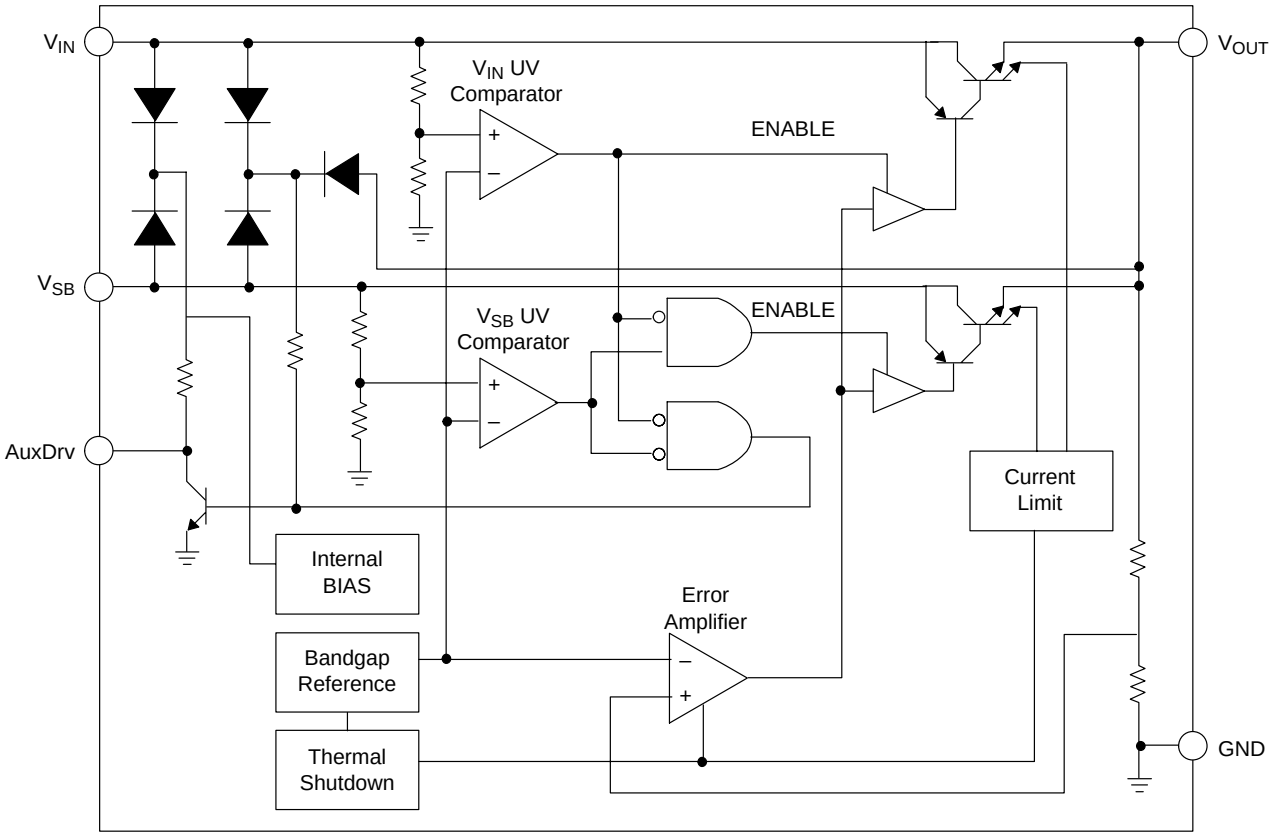


Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

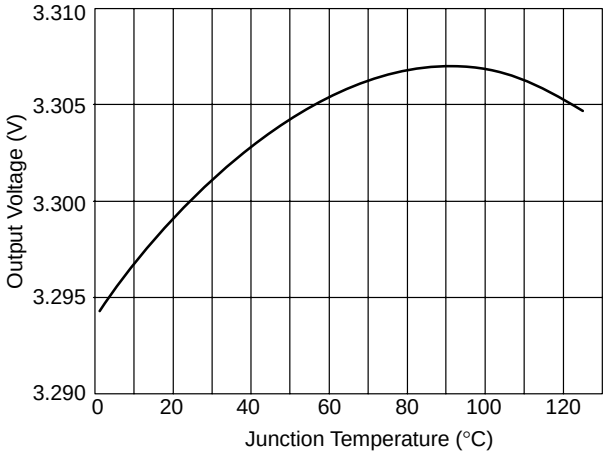


Figure 3. Output Voltage vs. Junction Temperature, Output Voltage when Powered by V_{IN} or V_{SB}

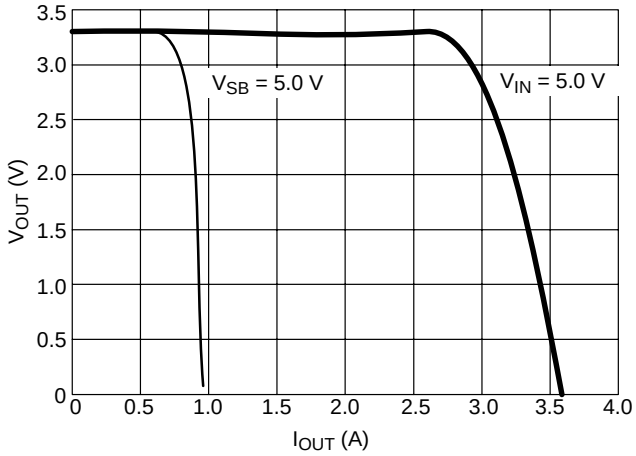


Figure 4. Output Voltage vs. Load Current, V_{SB} Values Taken with V_{IN} = 0 V

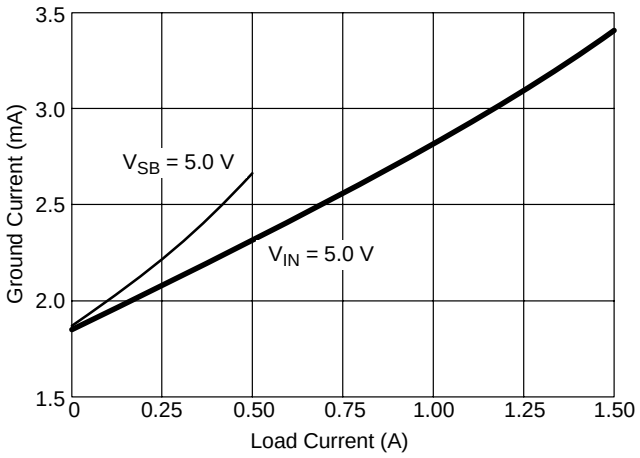


Figure 5. Ground Pin Current vs. Output Current, V_{SB} Data with V_{IN} = 0 V

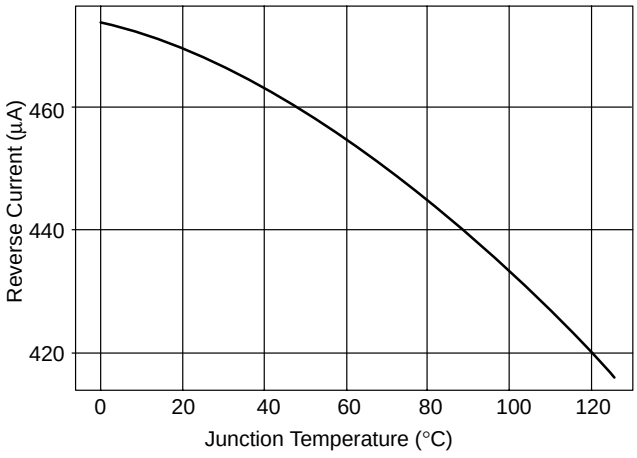


Figure 6. Reverse Current vs. Junction Temperature

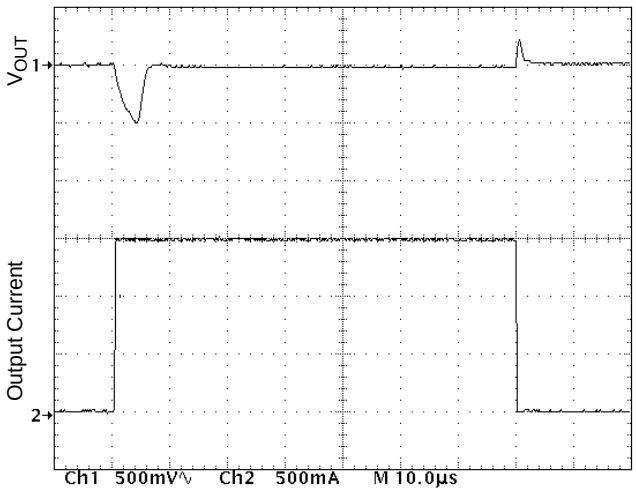


Figure 7. Transient Load Response, Transient Response for 1.5 A Step Load, V_{IN} = 5.0 V, C_{OUT} = 33 μF @ 0.4 Ω ESR

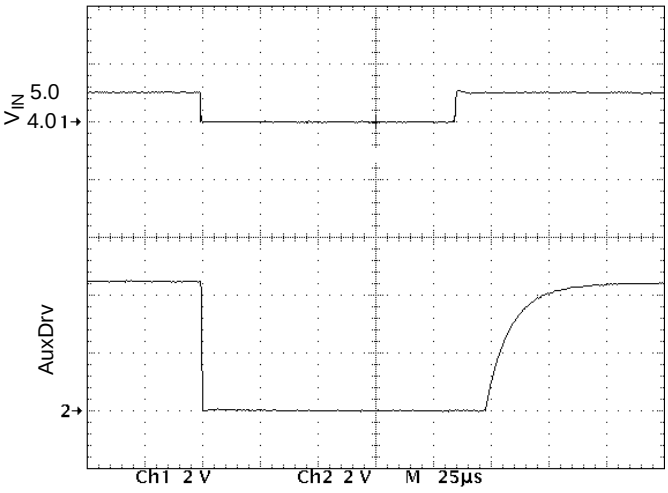


Figure 8. AuxDrv Response Time

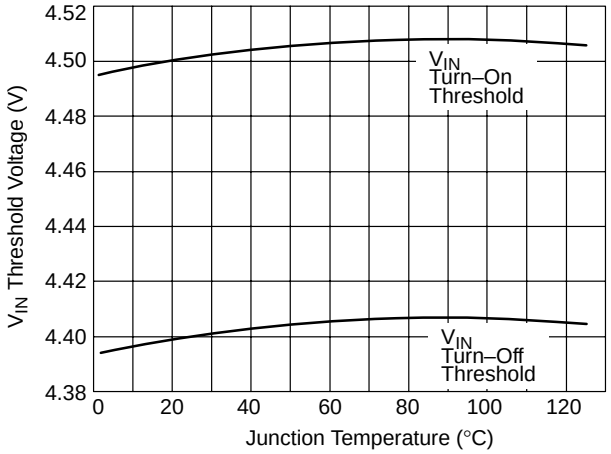


Figure 9. V_{IN} Threshold vs. Junction Temperature, Typical Minimum and Maximum Threshold Voltages to Switch AuxDrv Control

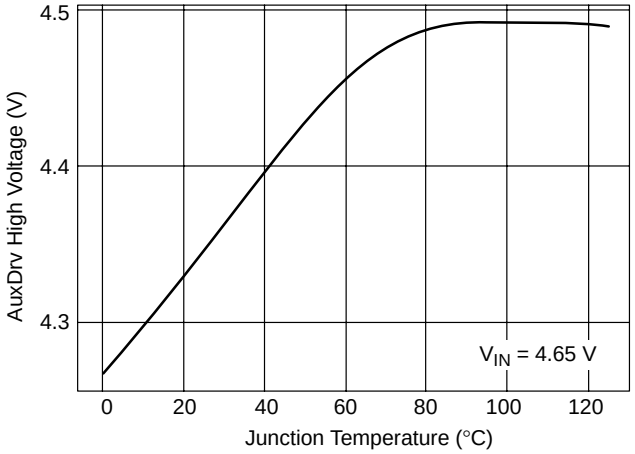


Figure 10. AuxDrv High Voltage vs. Junction Temperature

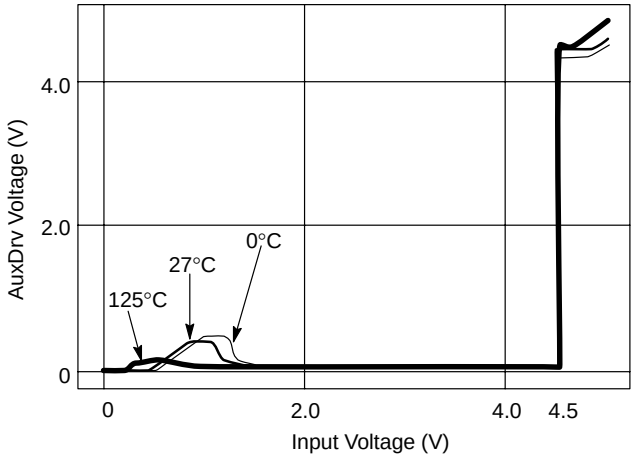


Figure 11. AuxDrv Voltage vs. Input Voltage (V_{SB} or V_{IN}) at Three Temperatures

APPLICATIONS INFORMATION

INPUT AND OUTPUT VOLTAGE MATRIX

Input				Outputs	
V_{IN}	V_{SB}	3.3 V_{AUX}	AuxDrv/5.0 V Detect	V_{OUT}, 5 Lead D^2PAK	V_{OUT}, 8 Lead SOIC
0 V	0 V	0 V	On (low)	0 V	0 V
0 V	0 V	3.3 V	On (low)	3.3 V_{AUX}	3.3 V_{AUX}
0 V	5.0 V	0 V	Off (high)	3.3 V_{REG} @ 500 mA	3.3 V_{REG} @ 500 mA
0 V	5.0 V	3.3 V	Off (high)	3.3 V_{REG} @ 500 mA	3.3 V_{REG} @ 500 mA
5.0 V	0 V	0 V	Off (high)	3.3 V_{REG} @ 1.5 A	3.3 V_{REG} @ 500 mA
5.0 V	0 V	3.3 V	Off (high)	3.3 V_{REG} @ 1.5 A	3.3 V_{REG} @ 500 mA
5.0 V	5.0 V	0 V	Off (high)	3.3 V_{REG} @ 1.5 A	3.3 V_{REG} @ 500 mA
5.0 V	5.0 V	3.3 V	Off (high)	3.3 V_{REG} @ 1.5 A	3.3 V_{REG} @ 500 mA

THEORY OF OPERATION

Linear Regulator

The CS5233–3 is a dual input fixed 3.3 V linear regulator that contains an auxiliary drive control feature. When V_{IN} alone is present, or V_{IN} and V_{SB} are simultaneously present, the CS5233–3 uses the V_{IN} supply to generate the 3.3 V output at currents of up to 1.5 A. When V_{SB} alone is present, the CS5233–3 uses the V_{SB} supply to generate the 3.3 V output at currents of up to 500 mA. The linear regulator is composed of a composite PNP–NPN pass transistor to provide low–voltage dropout capability. An output capacitor greater than 10 μF with equivalent series resistance (ESR) less than 1.0 Ω is required for compensation. More information is provided in the Stability Considerations section.

Auxiliary Drive Feature

The CS5233–3 provides an auxiliary drive feature that allows a load to remain powered even if both supplies to the IC are absent. An external p–channel FET is the only additional component required to implement this function when the auxiliary power supply is available. The PFET gate is connected to the IC's AuxDrv output, the PFET drain is connected to the auxiliary power supply, and the PFET source is connected to the load. The polarity of this connection is very important, since the PFET body diode will be connected between the load and the auxiliary supply. If the PFET is connected with its drain to the load and its source to the supply, the body diode could be forward–biased if the auxiliary supply is not present. This would result in the linear regulator providing current to everything on the auxiliary supply rail.

The AuxDrv (5.0 V detect) output is pulled up to the input voltage through an internal resistor when V_{IN} or V_{SB} are available. If V_{IN} and V_{SB} are not available or both drop below 4.4 V, the AuxDrv output goes low, turning on an external PFET that connects the 3.3 V auxiliary supply to the load. The AuxDrv is low only when neither V_{IN} nor V_{SB} are available.

There is 100 mV of hysteresis (typical) in the circuitry that determines if V_{IN} or V_{SB} are present.

STABILITY CONSIDERATIONS

The output capacitor helps determine three main characteristics of a linear regulator: loop stability, load transient response, and start–up delay. The CS5233–3 is designed to be stable with an output capacitor that has a minimum value of 10 μF and an equivalent series resistance less than 1.0 Ω. To guarantee loop stability, the output capacitor should be located close to the regulator output and ground pins. The load transient response, during the time it takes the regulator to respond, is also determined by the output capacitor. For large changes in load current, the ESR of the output capacitor causes an immediate drop in output voltage given by:

$$\Delta V = \Delta I \times ESR$$

There is then an additional drop in output voltage given by:

$$\Delta V = \Delta I \times T/C$$

where T is the time for the regulation loop to begin to respond, (typically 4.0 μs for the CS5233–3). If tight output regulation is required with fast changing loads, a capacitor network of tantalum and low ESR ceramic capacitors can be added as close to the load as possible, with enough capacitance and a reduced ESR to minimize the voltage change, as determined by the formulas above.

Input Capacitors and the Vin Thresholds

A capacitor placed on the V_{IN} pin will help to improve transient response. During a load transient, the input capacitor serves as a charge "reservoir," providing the

needed extra current until the external power supply can respond. One of the consequences of providing this current is an instantaneous voltage drop at V_{IN} due to capacitor ESR. The magnitude of the voltage change is again the product of the current change and the capacitor ESR.

It is very important to consider the maximum current step that can exist in the system. If the change in current is large enough, it is possible that the instantaneous voltage drop on V_{IN} will exceed the V_{IN} threshold hysteresis, and the IC will enter a mode of operation resembling an oscillation. As the part turns on, the output current I_{OUT} will increase, reaching current limit during initial charging. Increasing I_{OUT} results in a drop at V_{IN} such that the shutdown threshold is reached. The part will turn off, and the load current will decrease. As I_{OUT} decreases, V_{IN} will rise and the part will turn on, starting the cycle all over again. This oscillatory operation is most likely at initial start–up when the output capacitance is not charged, and in cases where the ramp–up of the V_{IN} supply is slow. It may also occur during the power transition when the linear regulator turns on and the PFET turns off. A 20 μs delay exists between turn–on of the regulator and the AuxDrv pin pulling the gate of the PFET high. This delay prevents “chatter” during the power transitions.

If required, using a few capacitors in parallel to increase the bulk charge storage and reduce the ESR should give better performance than using a single input capacitor. Short, straight connections between the power supply and V_{IN} lead along with careful layout of the PC board ground plane will reduce parasitic inductance effects. Wide V_{IN} and V_{OUT} traces will reduce resistive voltage drops.

Choosing the PFET Switch

The choice of the external PFET switch is based on two main considerations. First, the PFET should have a very low turn–on threshold. Choosing a switch transistor with $V_{GS(ON)} \approx 1.0$ V will ensure the PFET will be fully enhanced with only 3.3 V of gate drive voltage. Second, the switch transistor should be chosen to have a low $R_{DS(ON)}$ to minimize the voltage drop due to current flow in the switch. The formula for calculating the maximum allowable on–resistance is

$$R_{DS(ON)MAX} = \frac{V_{AUX(MIN)} - V_{OUT(MIN)}}{1.5 \times I_{OUT(MAX)}}$$

$V_{AUX(MIN)}$ is the minimum value of the auxiliary supply voltage, $V_{OUT(MIN)}$ is the minimum allowable output voltage, $I_{OUT(MAX)}$ is the maximum output current and 1.5 is a “fudge factor” to account for increases in $R_{DS(ON)}$ due to temperature.

Output Voltage Sensing

It is not possible to remotely sense the output voltage of the C5233–3 since the feedback path to the error amplifier is not externally available. It is important to minimize voltage drops due to metal resistance of high current PC board traces. Such voltage drops can occur in both the supply traces and the return traces.

The following board layout practices will help to minimize output voltage errors:

- Always place the linear regulator as close to both load and output capacitors as possible.
- Always use the widest possible traces to connect the linear regulator to the capacitor network and to the load.
- Connect the load to ground through the widest possible traces.
- Connect the IC ground to the load ground trace at the point where it connects to the load.

Current Limit

The CS5233–3 has internal current limit protection. Output current is limited to a typical value of 3.0 A for the D^2PAK using V_{IN} and 800 mA using V_{SB}, even under output short circuit conditions. If the load current drain exceeds the current limit value, the output voltage will be pulled down and will result in an out of regulation condition.

Thermal Shutdown

The CS5233–3 has internal temperature monitoring circuitry. The output is disabled if junction temperature of the IC reaches 180°C. Thermal hysteresis is typically 25°C and allows the IC to recover from a thermal fault without the need for an external reset signal. The monitoring circuitry is located near the composite PNP–NPN output transistor, since this transistor is responsible for most of the on–chip power dissipation. The combination of current limit and thermal shutdown will protect the IC from nearly any fault condition.

Reverse Current Protection

During normal system operation, the auxiliary drive circuitry will maintain voltage on the V_{OUT} pin. IC reliability and system efficiency are improved by limiting the amount of reverse current that flows from V_{OUT} to ground and from V_{OUT} to V_{IN}. Current flows from V_{OUT} to ground through the feedback resistor divider that sets up the output voltage, typically 400 μA. Current flow from V_{OUT} to V_{IN} will be limited to leakage current after the IC shuts down. On–chip RC time constants are such that the output transistor should be turned off well before V_{IN} drops below the V_{OUT} voltage.

Calculating Power Dissipation and Heatsink Requirements

Most linear regulators operate under conditions that result in high on–chip power dissipation. This results in high junction temperatures. Since the IC has a thermal shutdown feature, ensuring the regulator will operate correctly under normal conditions is an important design consideration. Some heatsinking will usually be required.

Thermal characteristics of an IC depend on four parameters: ambient temperature (T_A in °C), power dissipation (P_D in watts), thermal resistance from the die to the ambient air (θ_{JA} in °C per watt) and junction temperature (T_J in °C). The maximum junction temperature is calculated from the formula below:

$$T_{J(MAX)} = T_{A(MAX)} + \theta_{JA} \times P_{D(MAX)}$$

Maximum ambient temperature and power dissipation are determined by the design, while θ_{JA} is dependent on the package manufacturer. The maximum junction temperature for operation of the CS5233–3 within specification is 150°C. The maximum power dissipation of a linear regulator is given as

$$P_{D(MAX)} = (V_{IN(MAX)} - V_{OUT(MIN)}) \times I_{LOAD(MAX)} + V_{IN(MAX)} \times I_{GND(MAX)}$$

where $I_{GND(MAX)}$ is the IC bias current.

It is possible to change the effective value of θ_{JA} by adding a heatsink to the design. A heatsink serves in some manner to raise the effective area of the package, thus improving the flow of heat from the package into the surrounding air. Each material in the path of heat flow has its own characteristic thermal resistance, all measured in °C per watt. The thermal resistances are summed to determine the total thermal resistance between the die junction and air. There are three components of interest: junction–to–case thermal resistance (θ_{JC}), case–to–heatsink thermal resistance (θ_{CS}) and heatsink–to–air thermal resistance (θ_{SA}). The resulting equation for junction–to–air thermal resistance is

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}, \text{ or}$$
$$\theta_{JA} = \theta_{JC} + \theta_{SA} \text{ for } \theta_{CS} = 0$$

The value of θ_{JC} for the CS5233–3 is provided in the Packaging Information section of this data sheet. θ_{CS} can be considered zero, since heat is conducted out of the package by the IC leads and the tab of the D^2PAK package, and since the IC leads and tab are soldered directly to the PC board.

Modification of θ_{SA} is the primary means of thermal management. For surface mount components, this means modifying the amount of trace metal that connects to the IC.

The thermal capacity of PC board traces is dependent on how much copper area is used, if the IC is in direct contact with the metal, whether the metal surface is coated with some type of sealant, and whether there is airflow across the PC board. The chart provided below shows heatsinking capability of a square, single sided copper PC board trace. The area is given in square millimeters, and it is assumed there is no airflow across the PC board.

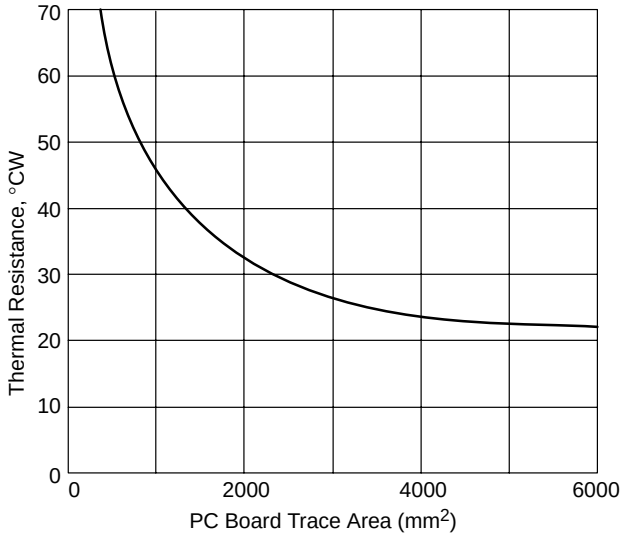
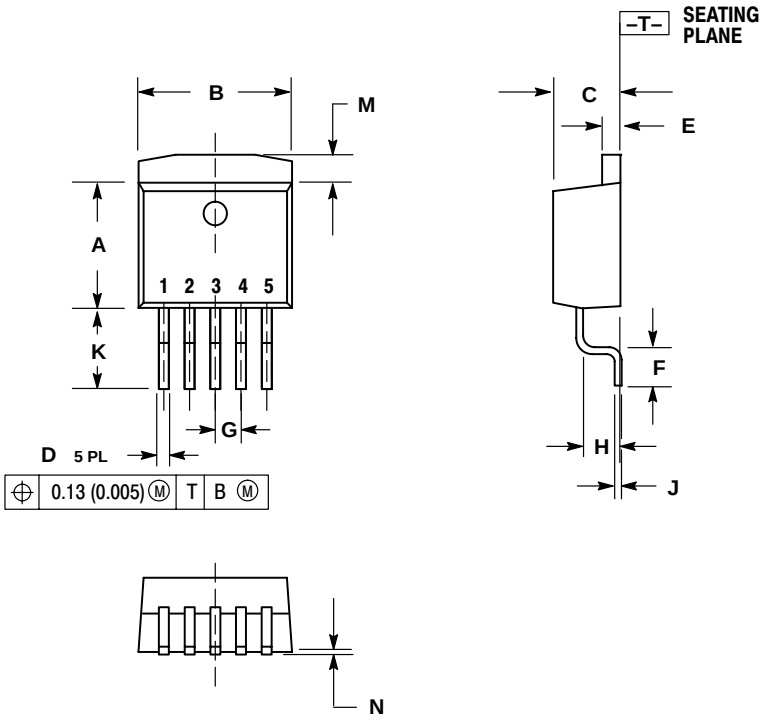


Figure 12. Thermal Resistance Capability of Copper PC Board Metal Traces

PACKAGE DIMENSIONS

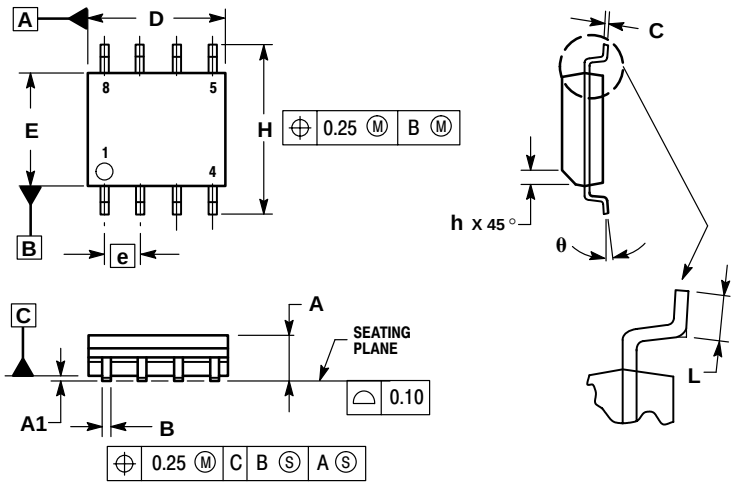
D²PAK
5–PIN
DP SUFFIX
CASE 936F–01
ISSUE O



NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS B AND M.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAX.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.326	0.336	8.28	8.53
B	0.396	0.406	10.05	10.31
C	0.170	0.180	4.31	4.57
D	0.026	0.035	0.66	0.91
E	0.045	0.055	1.14	1.40
F	0.090	0.110	2.29	2.79
G	0.067 BSC		1.70 BSC	
H	0.098	0.108	2.49	2.74
J	0.018	0.025	0.46	0.64
K	0.204	0.214	5.18	5.44
M	0.055	0.066	1.40	1.68
N	0.000	0.004	0.00	0.10

SO–8
DF SUFFIX
CASE 751–06
ISSUE T



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

PACKAGE THERMAL DATA

Parameter		5 Lead D^2PAK	8 Lead SOIC	Unit
$R_{\Theta JC}$	Typical	1.0–4.0	25	°C/W
$R_{\Theta JA}$	Typical	10–50*	110	°C/W

*Depending on thermal properties of substrate. $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$.

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