2.5 GBPS LIMITING AMPLIFIER S3051

FEATURES

- 2 GHz Bandwidth
- 32dB Gain
- Single +5V Power Supply
- Fully Differential Architecture
- 16 pin Glass-Metal Package

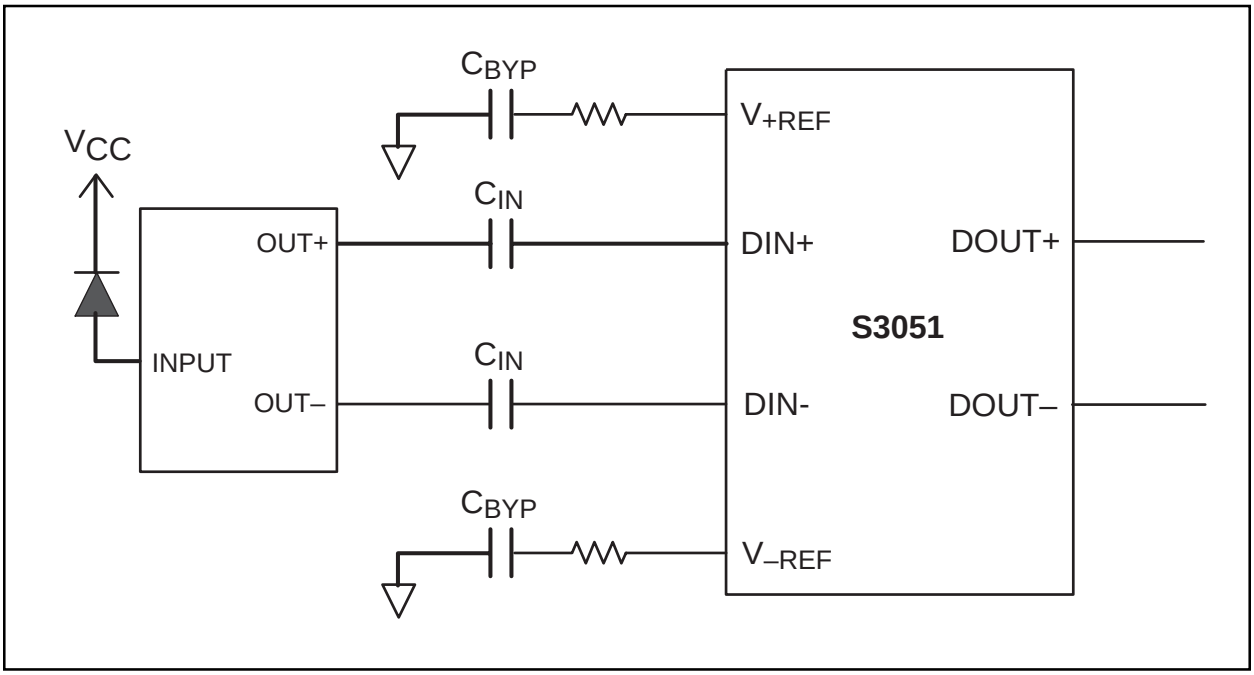
APPLICATIONS

- SONET OC-48
- Fiber Optic Data Links
- High-Speed FM Limiting Amplifier

GENERAL DESCRIPTION

The S3051 limiting amplifier with its high gain and wide bandwidth is ideal for use as a post amplifier in fiber optic receivers with data rates up to 2.5 Gbps. The amplifier's gain is 32dB, and differential signals as small as 12 mVp-p, can be amplified to 900 mVp-p. Figure 1 shows a typical system application.

Figure 1. System Block Diagram



DETAILED DESCRIPTION

The S3051 is an integrated limiting amplifier intended for high-frequency fiber-optic applications. The circuit connects to typical transimpedance amplifiers found within a fiber-optic link. The linear signal output from a transimpedance amplifier can contain significant amounts of noise, and may vary in amplitude over time. The S3051 limiting amplifier quantizes the signal, and outputs a voltage limited waveform over a 38 dB input dynamic range.

At low signal levels, below 12 mVp-p, the circuit behaves as a linear amplifier. At higher levels the device becomes a limiting amplifier.

The referred wideband input noise (160 µVrms) allows for a less than 1E-9 Bit Error Rate for inputs down to 2 mVp-p.

The S3051 is designed to allow adjustment of the DC offset between the DIN+ and DIN– inputs. V_{+REF} can be used as a reference from which the required offset can be subtracted to set the DC bias level at DIN–. Similarly, $V_{–REF}$ can be used to set the DC bias level at DIN+. (See Application Information).

If no adjustment is made to the input DC bias level, two resistors can be connected in a negative feedback configuration in order to cancel any DC offset at the input. This will minimize the pulse width distortion. (See separate S3051 Limiting Amplifier Application document.)

Figure 2. Functional Block Diagram

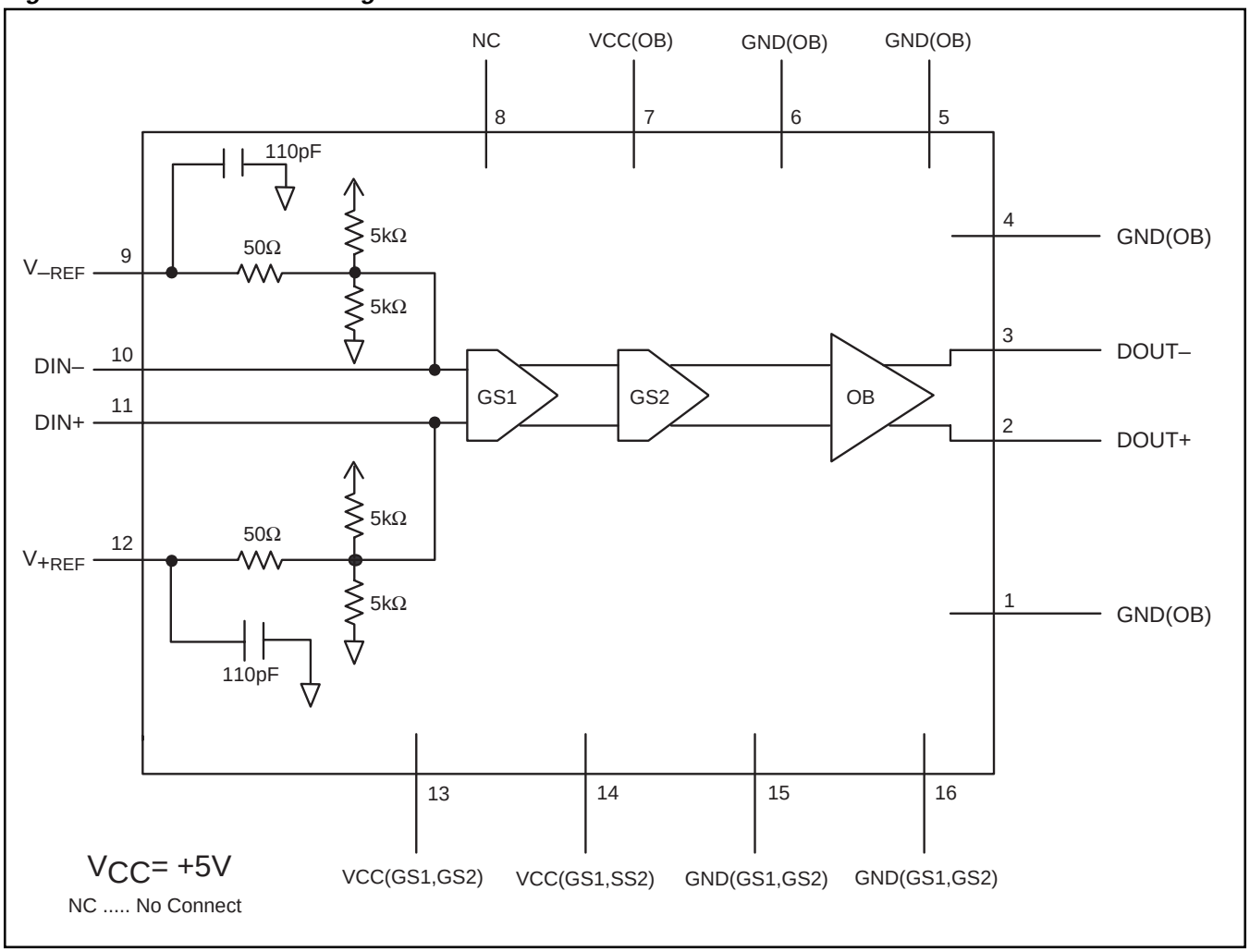
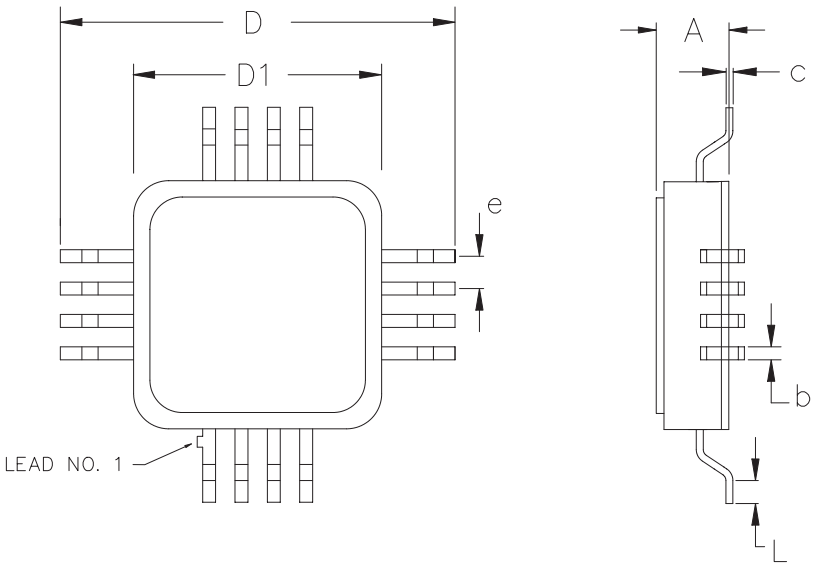


Table 1. S3051 Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
DOUT+	Analog	O	2	Positive data output.
DOUT–	Analog	O	3	Negative data output.
V_{-REF}	DC	O	9	Data Negative reference. Requires up-close external bypassing with a capacitor 0.047µF, or greater, matching the input coupling capacitor. (See Figure 7.)
DIN–	Analog	I	10	Negative data input.
DIN+	Analog	I	11	Positive data input.
V_{+REF}	DC	O	12	Data Positive reference. Requires up-close external bypassing with a capacitor 0.047µF, or greater, matching the input coupling capacitor. (See Figure 7.)
VCC	+5V	S	7, 13, 14	Positive supply.
GND	OV	S	1, 4, 5, 6, 15, 16	Negative supply.
NC			8	No connect.

Figure 3. S3051 16-Pin Glass-Metal Package



Sym.	INCHES	
	MIN.	MAX.
A		.060
D	.361	.371
D1	.220	.230
b	.010	.014
e	.030 BSC.	
c	.004	.006
L	.015	.025

Thermal Management

Device	Max Power	Θja
S3051	750 mW	60˚ C/W

Figure 4. S3051 Pinout (Top View)

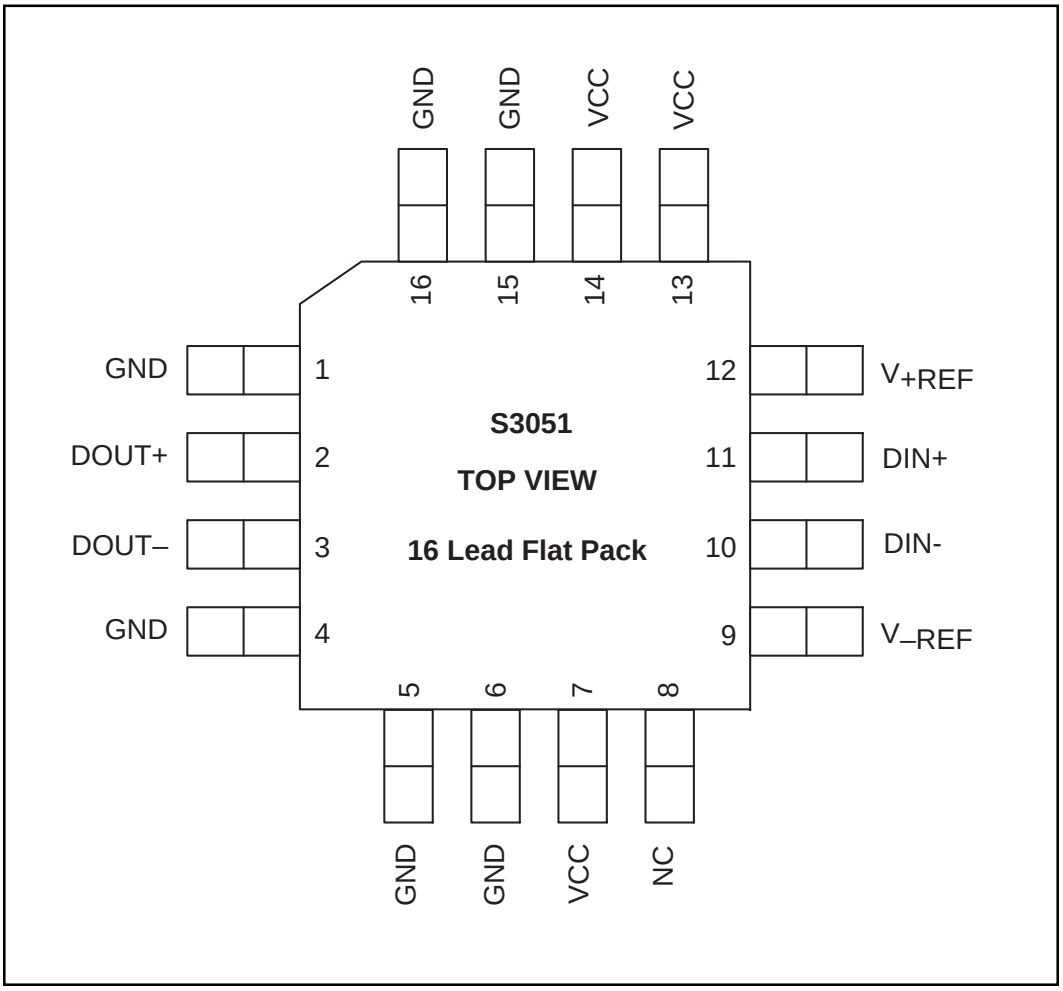


Table 2. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Ambient Temperature Under Bias	–40		+85	˚C
Junction Temperature Under Bias	–10		+130	˚C
Voltage on V_{CC} with respect to GND	4.75	5.0	5.25	V

Table 3. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Storage Temperature Range	–55		+175	˚C
Processing Temperature			+400	˚C
Power Supply V_{CC} with respect to GND			6.0	V
Input Voltage (DIN+, DIN–)			6.0	V
DOUT+, DOUT– (with 50Ω load)	2.5		V_{CC} +0.3	V
ESD Sensitivity [1]	Under 500			V

1. Human body model.

Table 4. AC Electrical Characteristics

(V_{CC} = 5V ± 5%, T_A = –40˚C to +85˚C)

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{ID} = (V_{IN+})-(V_{IN-})	Voltage Range (Over which output is limited)	12		1000	mVp-p	Peak-to-peak, differential (See Figure 5.)
A_D	Differential Gain	32		48	dB	V_{ID} = 8mVp-p
V_N	Differential Input Noise			160 3.58	µV nV/√Hz	Input referred noise = RMS output noise/low frequency gain, 7 kHz–2 GHz
PWD	Pulse Width Distortion			0.1	UI	Input is 2.488 Gbps 2^{23}-1 PRBS, V_{ID} = 12mVp-p and 1000mVp-p note 1
t_R, t_F	Output Edge Speed (20%–80%)		100	165	ps	V_{ID} = 12mVp-p
V_{OD} = (V_{OUT+})-(V_{OUT-})	Differential Output Voltage Swing	550	900		mVpp	Peak-to-peak, differential, 50Ω line termination. (See Figure 6.)
BW_H	Upper Small-Signal Bandwidth	1.6	2		GHz	
BW_L	Low Frequency Cut-off		2		kHz	Input coupling and bypassing as in Figure 7.
S11	Input Reflection Coefficient			–15	dB	200 kHz–2 GHz, 50Ω line termination.
S12	Isolation			–45	dB	200 kHz–2 GHz, 50Ω line termination.
S22	Output Reflection Coefficent			–15	dB	200 kHz–2 GHz, 50Ω line termination.

Note 1. Input offset calibrated out at V_{ID} = 15mV.

Table 5. DC Electrical Characteristics

(V_{CC} = 5V ± 5%, T_A = –40˚C to +85˚C)

Parameters	Description	Min	Typ	Max	Units	Comments
I_{CC}	Power Supply Current		75	100	mA	
V_{DIN}	Input Bias Voltage		V_{CC}/2		V	
V_{OFFSET}	Miximum Input (DIN+, DIN–) Offset Adjust			V_{DIN} ±300	mV	
V_{OL}	Output LOW Voltage	V_{CC} –0.95		V_{CC} –0.5	V	
V_{OH}	Output HIGH Voltage	V_{CC} –0.5		V_{CC}	V	

Figure 5. Input Voltage

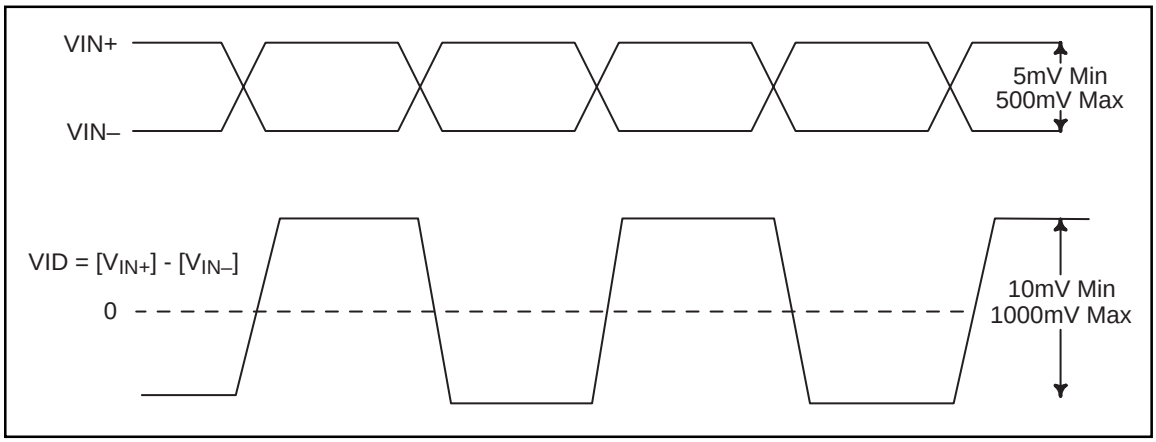
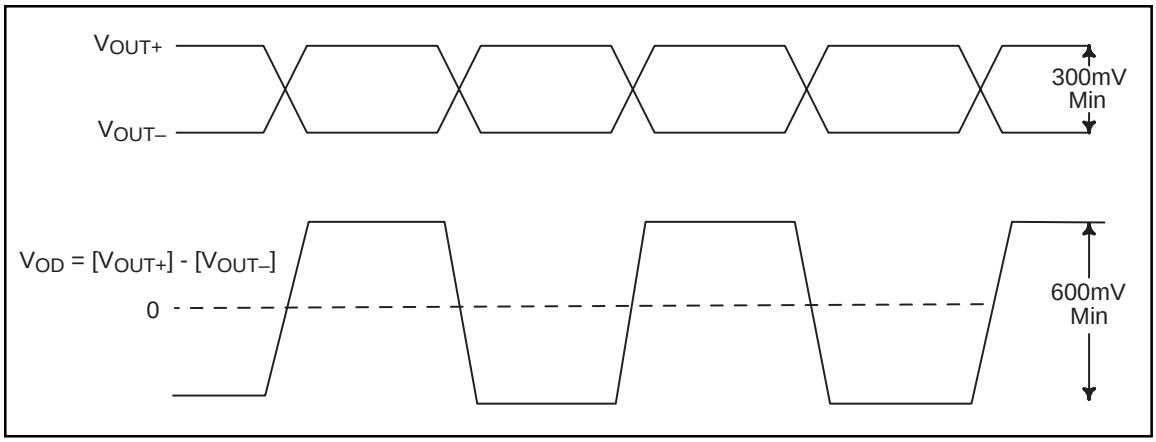


Figure 6. Output Voltage

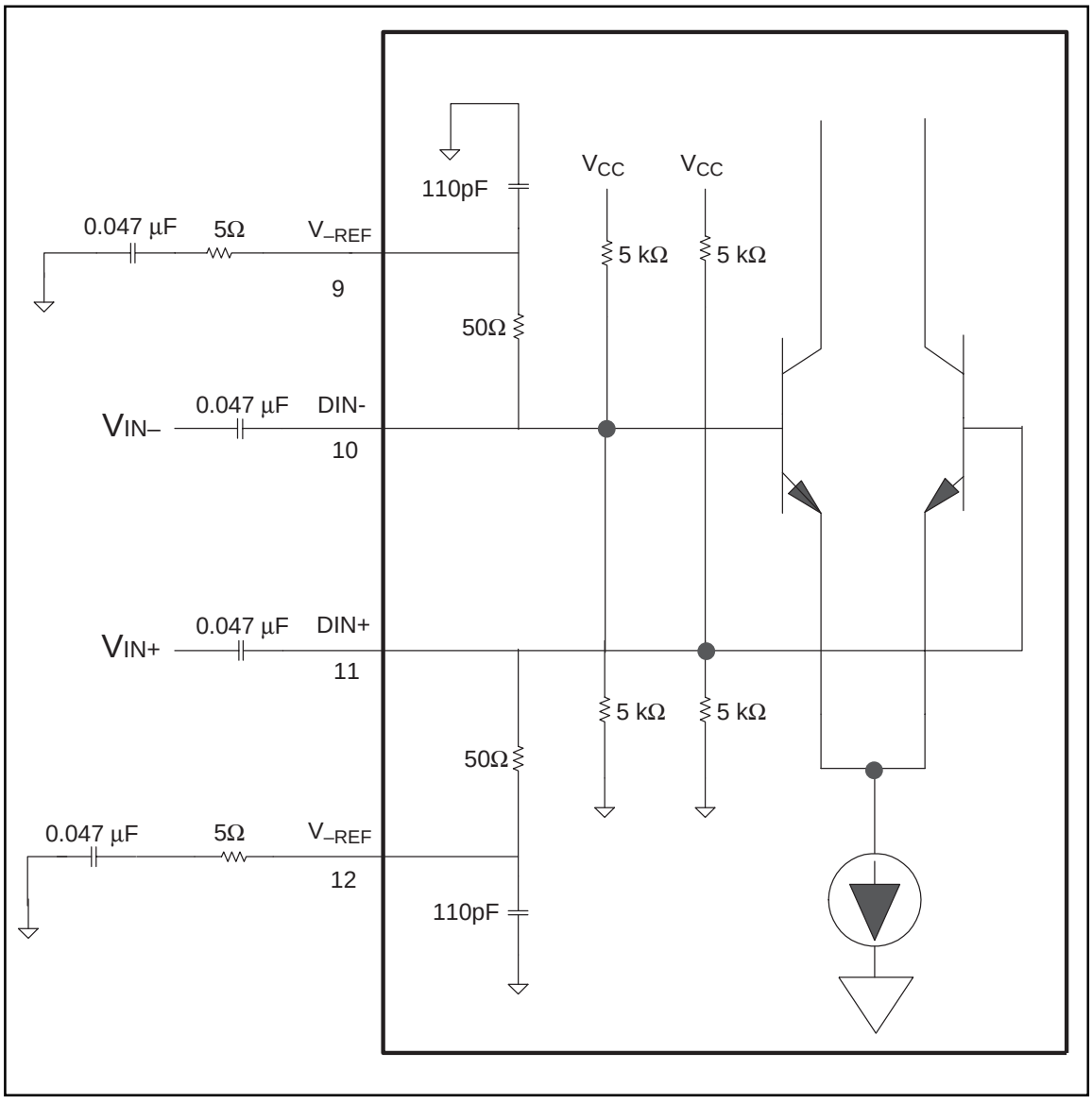


APPLICATIONS INFORMATION

Connecting to the Input of S3051

The equivalent input circuit of S3051 is shown in Figure 7. Both DC biasing and 50 Ohm input line termination have been implemented internally.

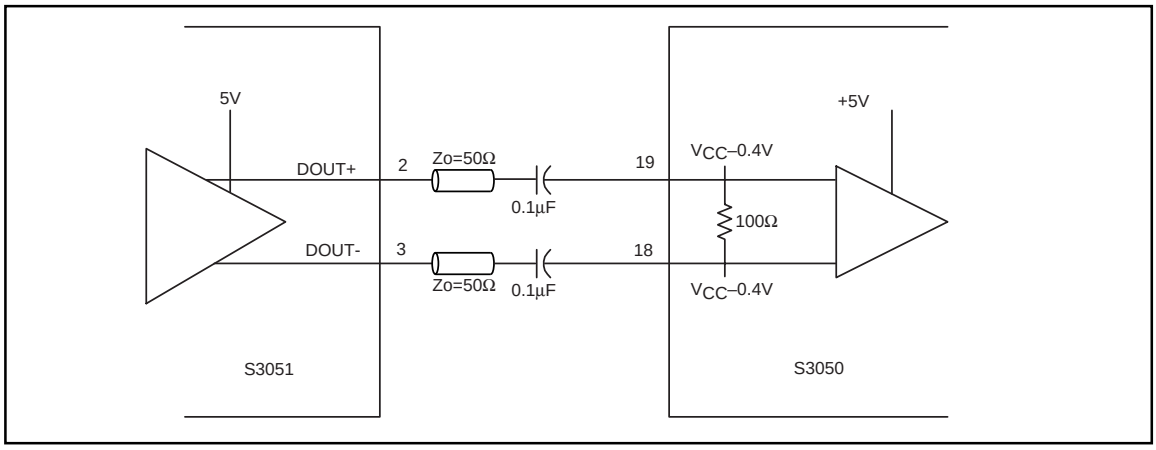
Figure 7. S3051 Equivalent Input Circuit



Connecting to the Output of S3051

The output of the S3051 does not require any external termination.

Figure 8. Output Termination



Adjusting Input DC Offset

The DC bias level at DIN– and DIN+ can be adjusted by inserting a Difference Amplifier function, as shown in Figures 9 and 10.

Figure 9. Adjusting the DC Bias Level at DIN–

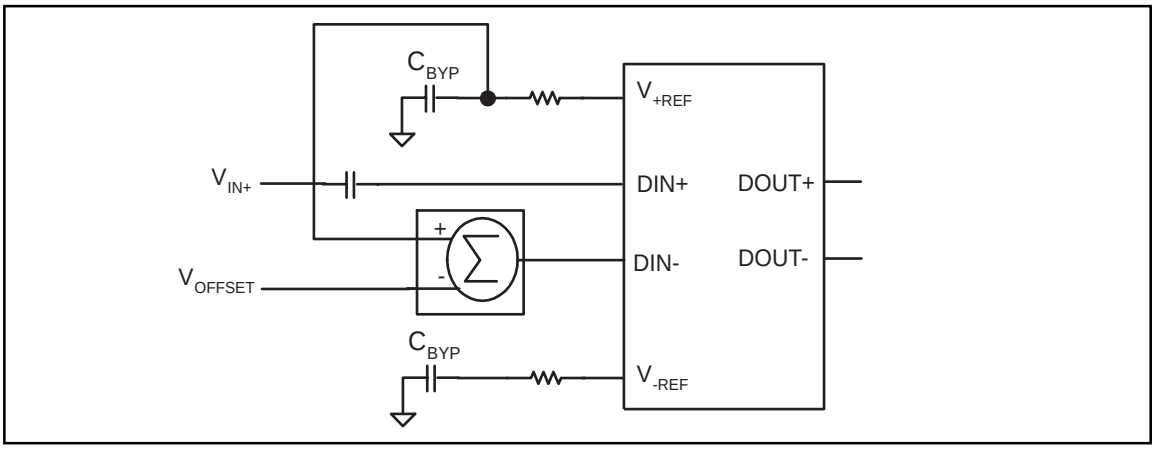
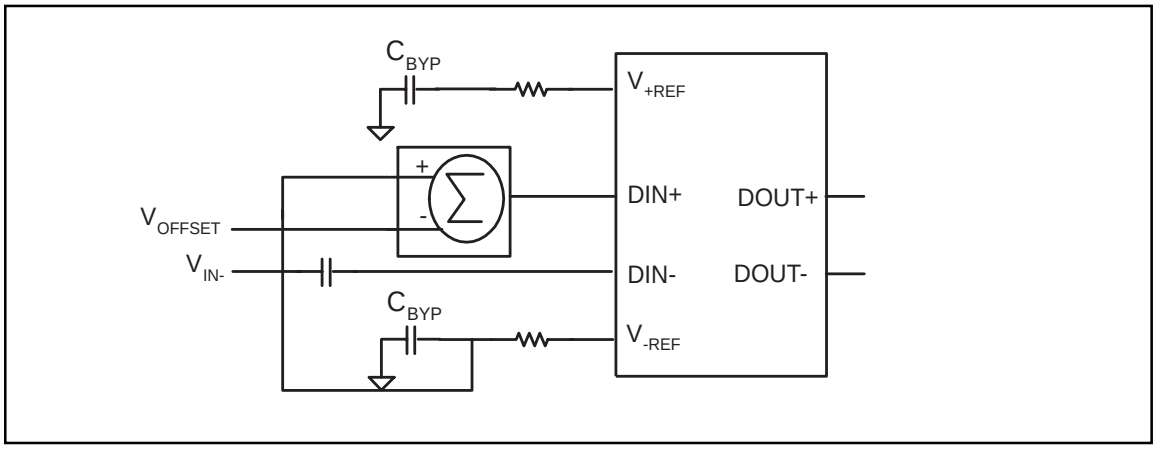


Figure 10. Adjusting the DC Bias Level at DIN+



Typical Operating Characteristics

Figure 11. Vcc Supply Current vs. Temperature

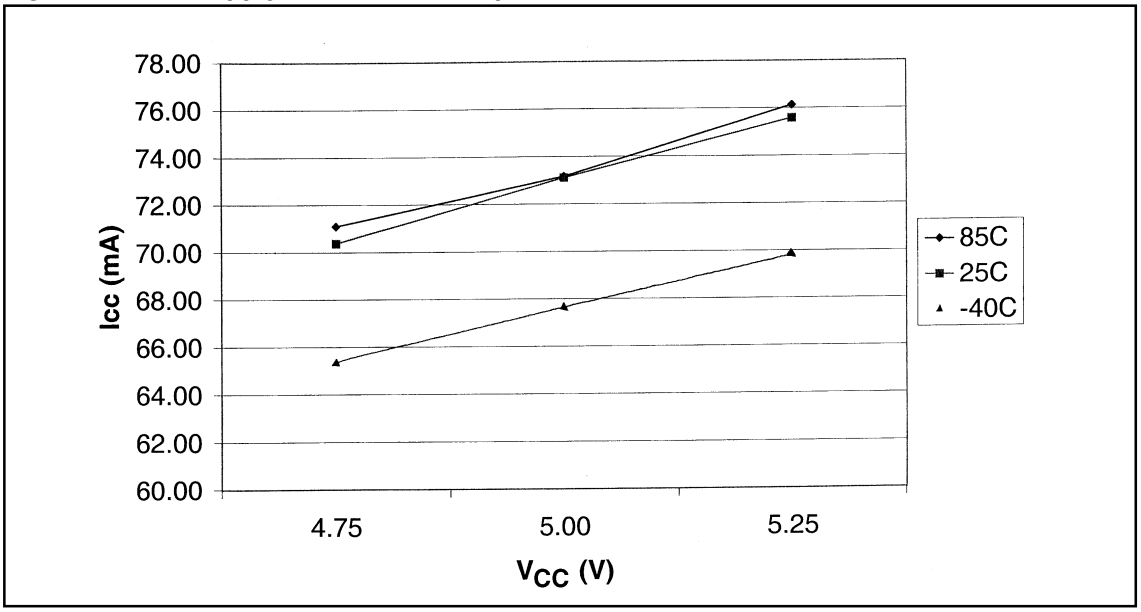


Figure 12. Frequency Response

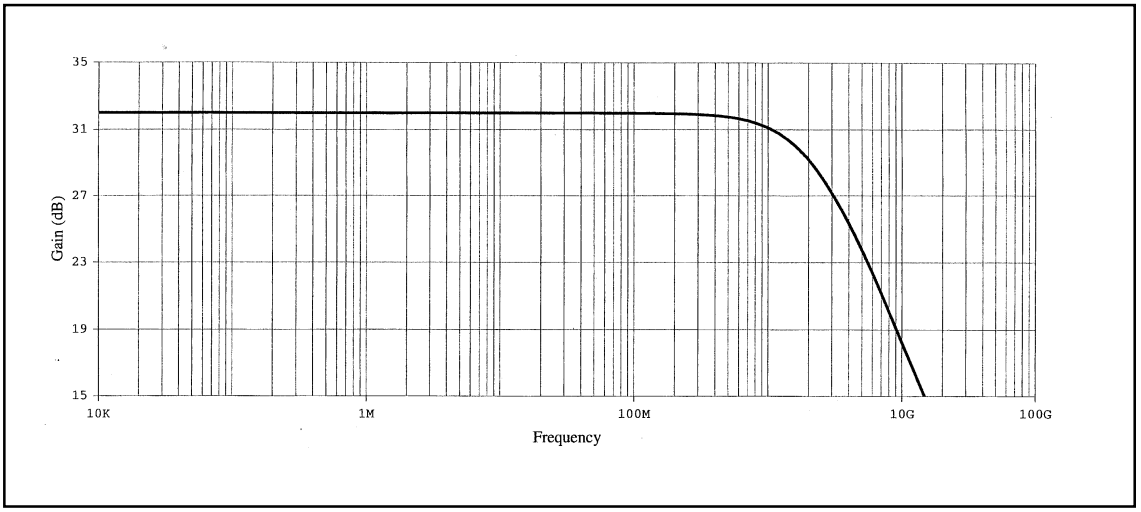


Figure 13. Eye Pattern @V_{ID} = 12mV

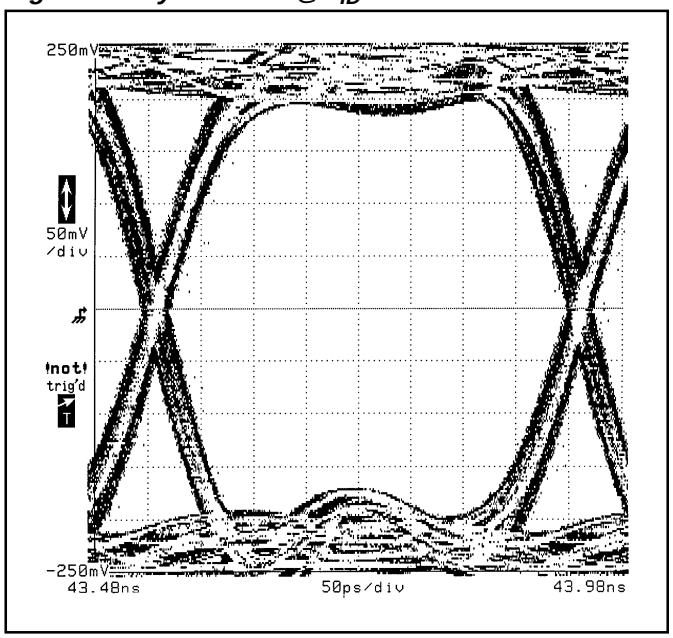


Figure 14. Eye Pattern @V_{ID} = 1000mV

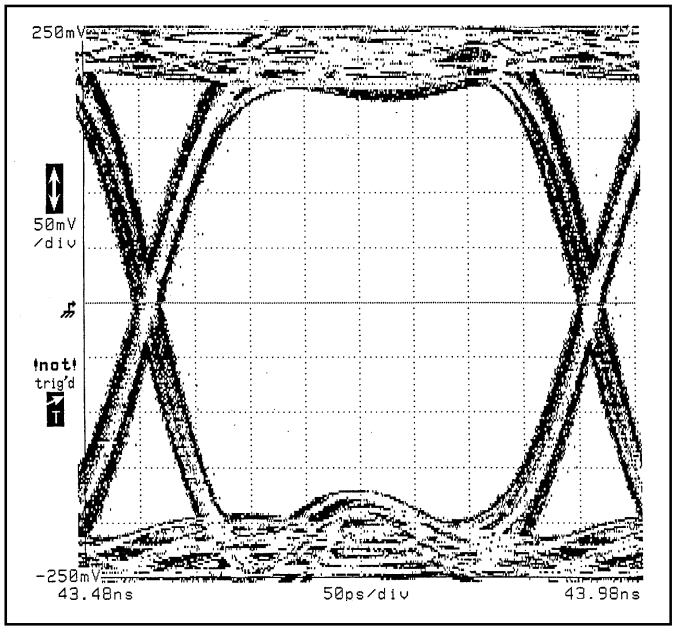
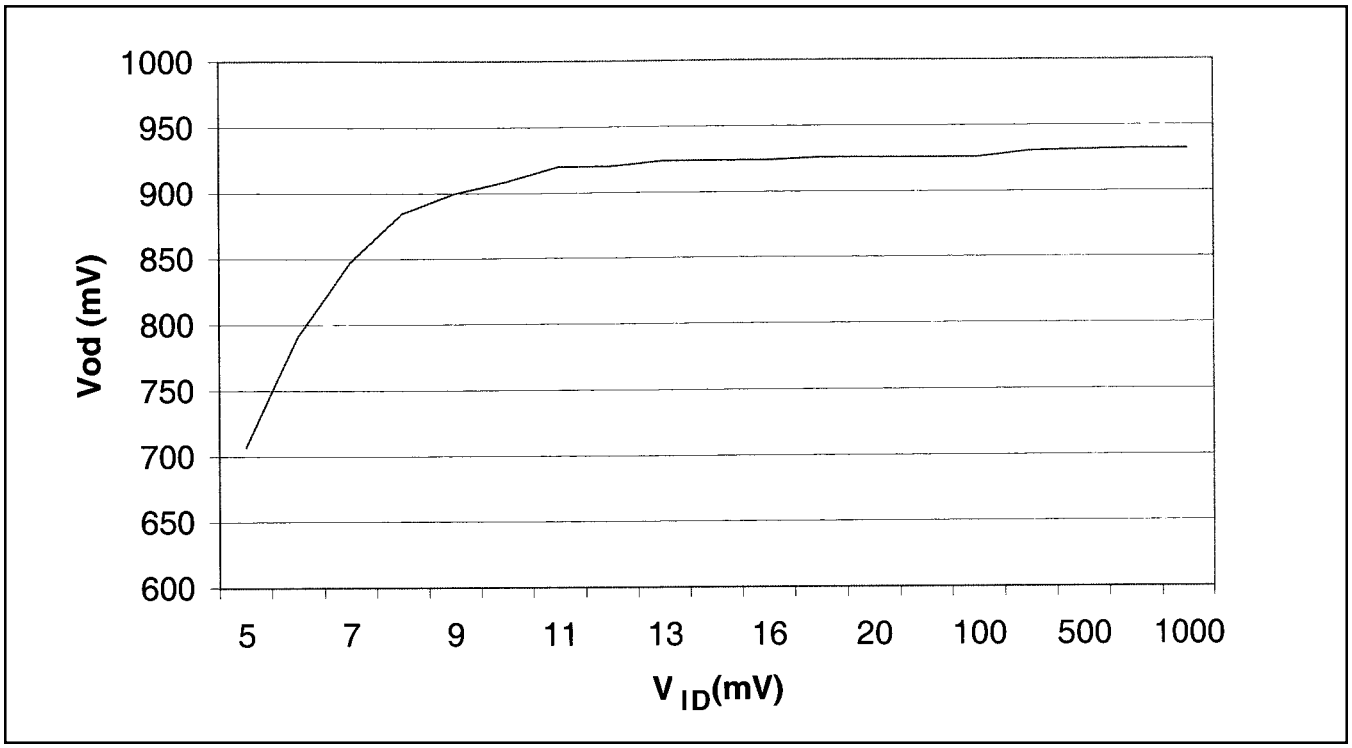
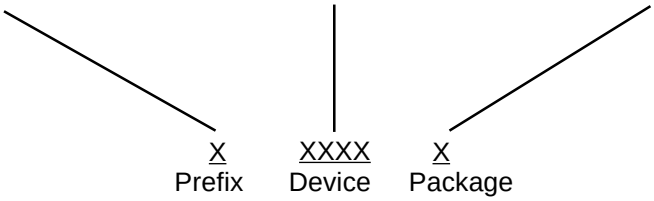


Figure 15. Input Voltage vs. Output Voltage



Ordering Information

PREFIX	DEVICE	PACKAGE
S – Integrated Circuit	3051	A – 16 Lead Flat Pack



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