PM5344

SPTX

SONET/SDH PATH TERMINATING TRANSCEIVER TELECOM

DATA SHEET

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1 FEATURES

- Monolithic SONET/SDH Path Terminating Transceiver that terminates the path overhead of one or three STS-1 (AU3) paths or a single STS-3c (AU4) path.
- Maps one or three STS-1 (AU3) payloads or a single STS-3c (AU4) payload to system timing reference, accommodating plesiochronous timing offsets between the references through pointer processing.
- Operates at 19.44 MHz or 6.48 MHz, processing a duplex 19.44 Mbyte/s or 6.48 Mbyte/s data stream.
- Supports line loopback from line side receive stream to transmit stream and diagnostic loopback from ADD bus interface to DROP bus interface.
- Operates in conjunction with the PM5343 STXC, or with the PM5312 STTX and PM5318 SIPO to form a complete physical interface up to photonics.
- Provides a generic 8-bit microprocessor bus interface for configuration, control, and status monitoring.
- Low power, +5 Volt, CMOS technology, TTL compatible inputs and outputs.
- 160 pin plastic quad flat pack (PQFP) package.

1.1 The receiver section:

- Operates in STS-3 (AU3) or STS-3c (AU4) mode.
- Accepts a byte serial line side multiplex of three STS-1 (AU3) streams or a single STS-3c (AU4) stream, interprets the STS (AU) pointer bytes (H1, H2, and H3), and extracts the synchronous payload envelope(s) and inserts the synchronous payload envelope(s) into a bus referenced to system timing, using pointer processing.
- Extracts and processes the three STS-1 (AU3) path overhead streams or the single STS-3c (AU4) path overhead stream.
- Detects loss of pointer (LOP).
- Detects loss of tributary multiframe (LOM).
- Detects path alarm indication signal (AIS).

- Detects path FERF alarm.
- Extracts and serializes the entire path overhead from the three STS-1 (AU3) or single STS-3c (AU4) stream. Identifies the positions of the path overhead bytes in the serialized streams.
- Extracts the path signal label (C2) byte into an internal register and detects for path signal label unstable and for signal label mismatch with the expected signal label that is downloaded by the microprocessor.
- Extracts the 64 byte or 16 byte path trace (J1) message into an internal register bank.
- Detects for unstable path trace message and mismatch with the expected path trace message that is downloaded by the microprocessor.
- Detects received path BIP-8 and counts received path BIP-8 errors for performance monitoring purposes. Path BIP-8 errors are also available on an output pin. BIP-8 errors are selectable to be treated on a bit basis or block basis.
- Counts received path far end block errors (FEBEs) for performance monitoring purposes.
- Extracts the three STS-1 (AU3) payloads or single STS-3c (AU4) payload and presents it on a byte serial bus.
- Supports Telecombus interfaces by indicating the location of the STS identification byte (C1), the path trace byte(s) (J1), the first tributary overhead byte(s) (V1), and all synchronous payload envelope bytes in the byte serial stream. Also generates bus parity.
- Accomodates phase and frequency differences between the receive stream and the DROP bus via pointer adjustments in the DROP bus.
- Supports tandem connection origination applications by sourcing a new tandem path maintenance byte (Z5) reporting the received BIP-8 errors and the data link message and correcting subsequent path BIP-8 bytes (B3) to reflect the change in Z5.
- Supports tandem connection termination applications by accumulating the incoming error count (IEC) and extracting the tandem connection data link carried in the tandem path maintenance byte (Z5).

- Maintains existing pointer value during incoming signal failures in tandem path terminating mode.

- Maintains the existing tributary multiframe sequence on the H4 byte until a new phase alignment has been verified.

- Provides a "Telecombus" line side receive interface when path termination is done by an upstream device.

- Provides a serial alarm port communication of FEBE and path FERF alarms to the transmit stream in the returning direction.

1.2 The transmitter section:

- Operates in STS-1 (AU3) or STS-3c (AU4) mode.

- Accepts a byte serial multiplex of three STS-1 (AU3) streams or an STS-3c (AU4) stream, extracts the synchronous payload envelope(s) and inserts the synchronous payload envelope(s) with a generated pointer into the transmit system, using pointer processing.

- Supports system side "Telecombus" interfaces by accepting indications of the location of the STS identification byte (C1), the path trace byte(s) (J1), the first tributary overhead byte(s) (V1), and all synchronous payload envelope bytes in the byte serial stream.

- Provides line side "Telecombus" interface on the transmit stream indicating the location of the STS identification byte (C1), the path trace byte(s) (J1), the first tributary overhead byte(s) (V1), and all synchronous payload envelope bytes.

- Accomodates phase and frequency differences between the ADD bus and the transmit stream via pointer adjustments in the transmit stream.

- Optionally inserts STS path alarm indication signal (AIS).

- Optionally inserts STS path FERF alarm.

- Inserts the path overhead bytes in the three STS-1 (AU3) or single STS-3c (AU4) stream. The path overhead bytes may be sourced from internal registers or from bit serial path overhead input streams. Path overhead insertion may also be disabled.

- Optionally calculates and inserts path BIP-8 error detection codes.

- Optionally inserts the path FEBE count into the path status byte (G1) based on BIP-8 errors detected in the receive path.
- Inserts the path signal label (C2) byte from an internal register.
- Inserts the 64 byte or 16 byte path trace (J1) message from an internal register bank.
- Errors may be inserted in the path BIP8 byte (B3) for diagnostic purposes.
- Optionally inserts all-ones payload data for unequipped operations.
- Optionally generates cyclical tributary multiframe pattern.
- Supports in-band error reporting of BIP-8 and path alarms in the path status byte (G1).

2 APPLICATIONS

- SONET/SDH Add Drop Multiplexers
- SONET/SDH Terminal Multiplexers
- SONET/SDH Cross Connects
- SONET/SDH Tandem Path Termination Equipment
- SONET/SDH Test Equipment

3 REFERENCES

1. American National Standard for Telecommunications - Digital Hierarchy - Optical Interface Rates and Formats Specification, ANSI T1.105-1988.

2. American National Standard for Telecommunications - Layer 1 In-Service Digital Transmission Performance Monitoring, T1X1.3/93-005R1, April 1993.

3. Bell Communications Research - SONET Transport Systems: Common Generic Criteria, TR-TSY-000253, Issue 2, December 1991.

4. CCITT Study Group XVIII - Report R 105, Geneva, 9 - 19 June 1992.

5. CCITT Recommendation G781M, 13 October, 1992.

6. ETSI DE/TM1015, "Generic Functional Requirement for SDH Transmission Equipment", Version 0.4, February 1993.

7. CCITT Study Group XVII - Contribution D2166 - "Tandem Connection / Tandem Connection Bundle Maintenance - Working Solution", June 1992.

4 APPLICATION EXAMPLES

The following two examples show the SPTX used in typical SONET/SDH network equipment applications. In the first example, the SPTX is paired with the PM5343 STXC 155 Mbit/s Section and Line overhead terminating transceiver to provide a complete 155 Mbit/s SONET STS-3 or STS-3c/SDH STM-1 interface. In the second example, four SPTX chips are used in conjunction with the PM5312 STTX 622 Mbit/s Section and Line overhead terminating transceiver to provide a complete 622 Mbit/s SONET STS-12/SDH STM-4 interface. In both cases external clock recovery and synthesis is available from a number of commercial sources (additional information is available from PMC).

Figure 1 - 155 Mbit/s STS-3/STM-1 Add-Drop or Terminal Mux Interface

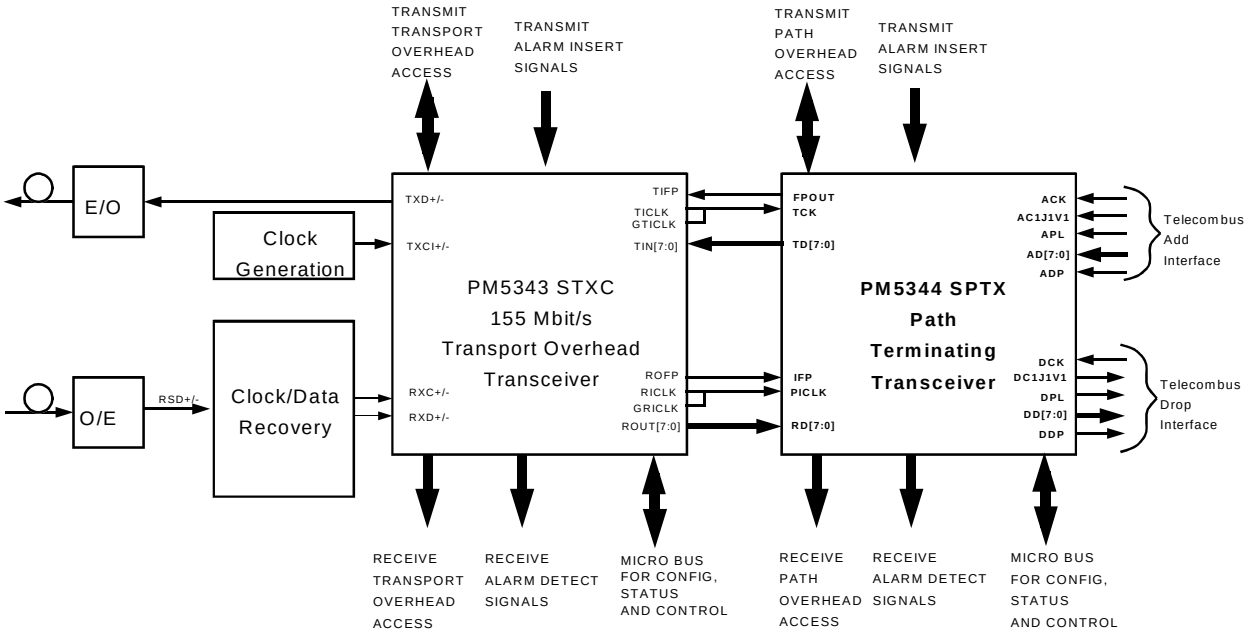
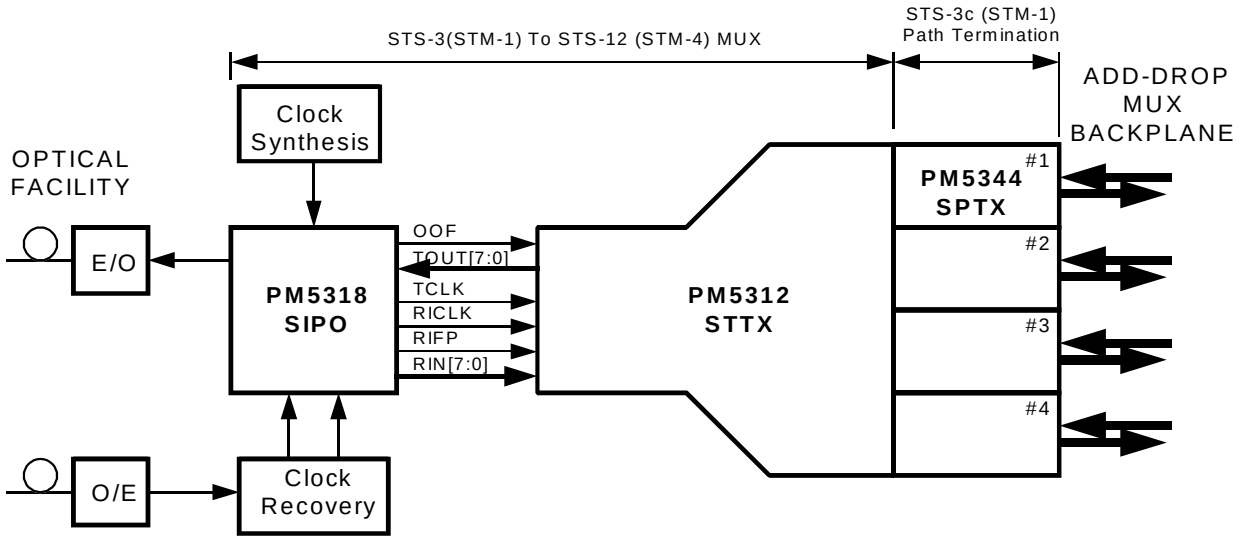
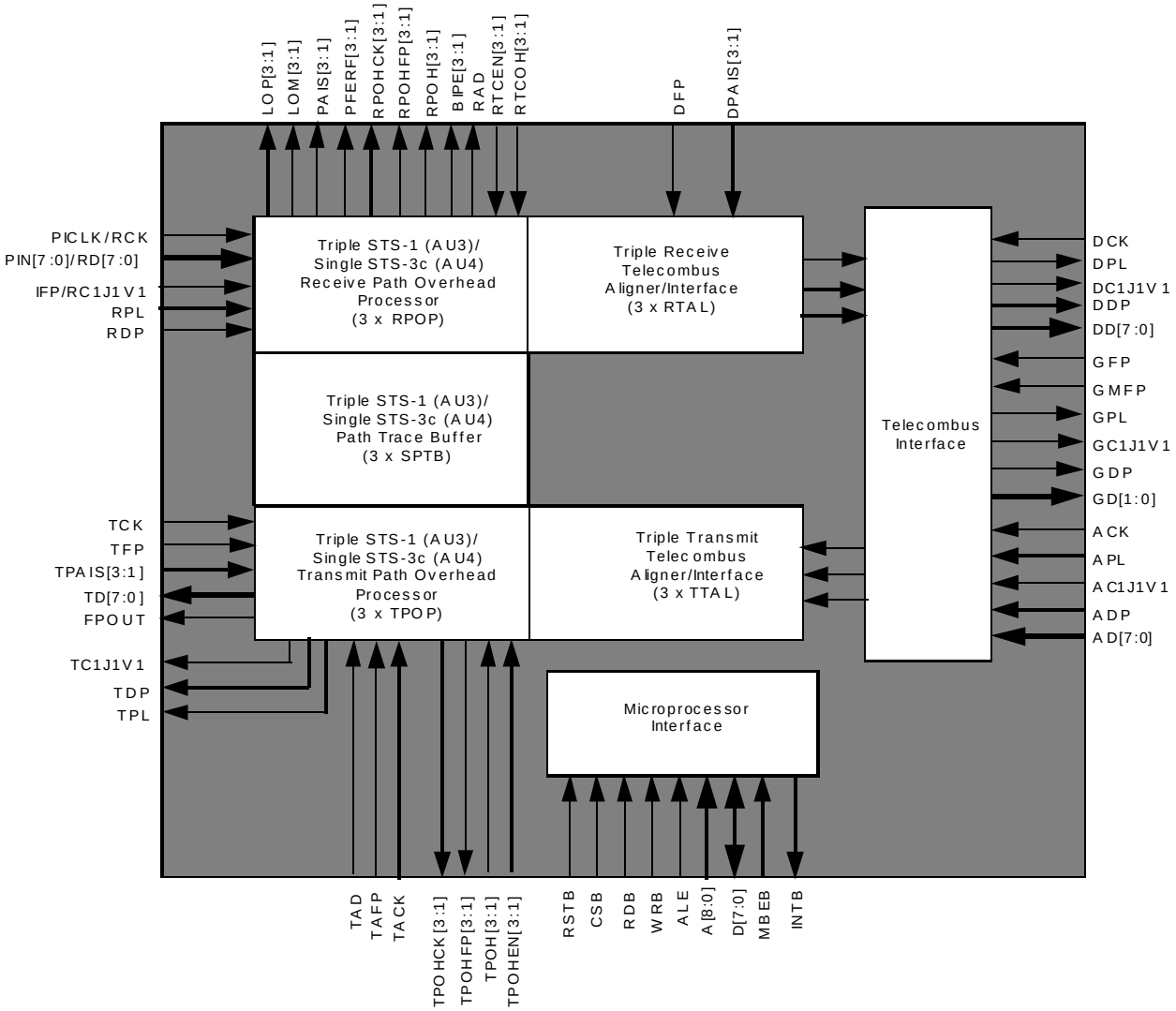


Figure 2 - 622 Mbit/s STS-12/STM-4 Add-Drop Multiplexer Aggregate Interface



5 BLOCK DIAGRAM



6 DESCRIPTION

The PM5344 SPTX SONET/SDH Path Terminating Transceiver is a monolithic integrated circuit that implements payload alignment and path termination for three STS-1 (AU3) paths or a single STS-3c (AU4) path, mapping these payloads onto a Telecombus-like system backplane.

The SPTX operates in conjunction with the PM5343 STXC SONET/SDH Transport Terminating Transceiver to form a complete system for terminating section, line, and path overhead of a SONET STS-3 (SDH STM-1) or SONET STS-1 electrical interface. Four SPTX devices operate in conjunction with the PM5712 SLIM SONET/SDH Line Interface Module to form a complete system for terminating section, line, and path overhead of a SONET STS-12 (SDH STM-4) electrical interface.

The SPTX provides receive path termination for a SONET STS-1, STS-3 or STS-3c stream, or equivalently, an AU3 or an SDH STM-1 stream carrying three AU3s or one AU4. The SPTX interprets the received payload pointers (H1, H2) and extracts the synchronous payload envelope (virtual container). The extracted SPE (VC) is placed on a Telecombus DROP bus. Frequency offsets (e.g., due to plesiochronous network boundaries, or the loss of a primary reference timing source) and phase differences (due to normal network operation) between the received data stream and the DROP bus are accommodated by pointer adjustments in the DROP bus. In addition to its basic processing of the received SONET/SDH overhead, the SPTX provides convenient access to all overhead bytes, which are extracted and serialized on lower rate interfaces, allowing additional external processing of overhead, if desired.

The SPTX provides transmit path origination for a SONET STS-1, STS-3 or STS-3c stream, or equivalently, an AU3 or an SDH STM-1 stream carrying three AU3s or one AU4. The SPTX generates the transmit payload pointers (H1, H2) and inserts the synchronous payload envelope (virtual container) from a Telecombus ADD bus into the transmit stream. Frequency offsets (e.g., due to plesiochronous network boundaries, or the loss of a primary reference timing source) and phase differences (due to normal network operation) between the transmit data stream and the ADD bus are accommodated by pointer adjustments in the transmit stream. In addition to its basic processing of the transmit SONET/SDH overhead, the SPTX provides convenient access to all overhead bytes, which are inserted serially on lower rate interfaces, allowing additional external sourcing of overhead, if desired. The SPTX also supports the insertion of a large variety of errors into the transmit stream, such as bit interleaved parity errors, and inverted NDF flags, which are useful for system

diagnostics and tester applications.The SPTX supports in-band error reporting where the path status byte (G1) inserted in the DROP bus reflects the number of BIP-8 errors detected and the path FERF status. The SPTX can be programmed to pass the path status byte on the ADD bus through unmodified. This feature allows the transmit path processor to be located remotely to the receive processor without having to incur the cost of routing an alarm port.

The SPTX supports tandem connection termination applications where the tandem connection maintenance byte (Z5) carries the incoming BIP-8 error count, a tandem data link, and a path AIS code. The incoming error count is accumulated and the receive data link is serialized for external processing. A new data link can be inserted from a low speed serial input. An incoming signal failure alarm (ISF) is used to convey path AIS in place of all-ones in the pointer (H1, H2).

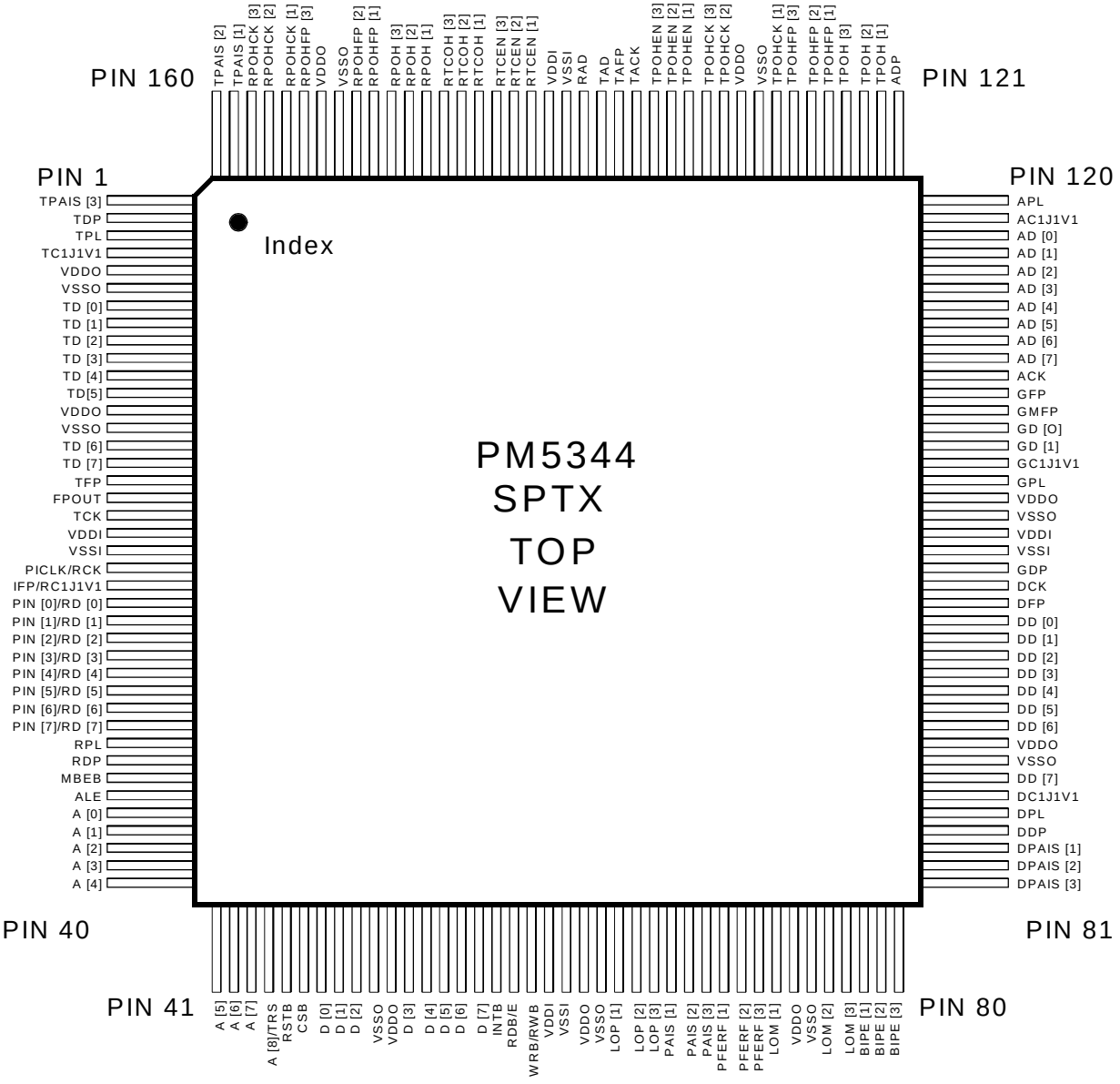
The SPTX maintains a large number of statistics for performance monitoring purposes. BIP-8 errors, and tandem path incoming error counts are accumulated. In addition, the SPTX is selectable to accumulate positive and negative pointer justifications that it receives or justifications that it generates on the DROP bus. It also accumulates positive and negative pointer justifications in the transmit stream. Excessive justifications may be indicative of clock synchronization failures.

In STS-3c, STS-3 (AU4, three AU3s) applications, no auxiliary high speed clocks are required as the SPTX operates from a set of plesiochronous 19.44 MHz clocks. In STS-1 (single AU3) applications, the SPTX operates from a set of plesiochronous 6.48 MHz clocks. The SPTX is configured, controlled and monitored via a generic 8-bit microprocessor bus interface.

The SPTX is implemented in low power, +5 Volt, CMOS technology. It has TTL compatible inputs and outputs and is packaged in a 160 pin PQFP package.

7 PIN DIAGRAM

The SPTX is packaged in an 160 pin PQFP package having a body size of 28 mm by 28 mm and a pin pitch of 0.65 mm.



8 PIN DESCRIPTION

Table 1 - Pin Description

Pin Name	Type	Pin No.	Function
PICLK /	Input	22	The parallel input clock (PICLK) provides timing for sampling the receive SONET/SDH stream, PIN[7:0] when external path termination is disabled. PICLK is nominally a 19.44 MHz or 6.48 MHz, 50% duty cycle clock. Inputs PIN[7:0] and IFP are sampled on the rising edge of PICLK. Inputs RPL and RDP are ignored. Outputs LOP[3:1], PAIS[3:1], and PFERF[3:1] are updated on the rising edge of PICLK.
RCK			The RECEIVE bus clock (RCK) provides timing for the RECEIVE bus interface when external path termination is enabled. RCK is nominally a 19.44 MHz or 6.48 MHz, 50% duty cycle clock. Outputs LOP[3:1], LOM[3:1], PAIS[3:1], PFERF[3:1], BIPE[3:1], RAD, RPOH[3:1], RPOHFP[3:1], are RPOHCLK[3:1] are inactive. Inputs RTCEN[3:1] and RTCOH[3:1] are ignored. Inputs RD[7:0], RC1J1V1, RPL, and RDP are sampled on the rising edge of RCK.
PIN[7] PIN[6] PIN[5] PIN[4] PIN[3] PIN[2] PIN[1] PIN[0] /	Input	31 30 29 28 27 26 25 24	The parallel receive data bus (PIN[7:0]) carries the SONET/SDH frame in byte serial format when external path termination is disabled. PIN[7] is the most significant bit (corresponding to bit 1 of each serial word, the first bit transmitted). PIN[0] is the least significant bit (corresponding to bit 8 of each serial word, the last bit transmitted). PIN[7:0] is sampled on the rising edge of PICLK.
RD[7] RD[6] RD[5] RD[4] RD[3] RD[2] RD[1] RD[0]			The RECEIVE bus data (RD[7:0]) carries the SONET/SDH frame in byte serial format when external path termination is enabled. RD[7] is the most significant bit (corresponding to bit 1 of each serial word, the first bit transmitted). RD[0] is the least significant bit (corresponding to bit 8 of each serial word, the last bit transmitted). RD[7:0] is sampled on the rising edge of RCK.

Pin Name	Type	Pin No.	Function
IFP / RC1J1V1	Input	23	The active high framing position signal (IFP) indicates when the first byte of the synchronous payload envelope (SPE byte 1 of STS-1 #1) is available on the PIN[7:0] bus when external path termination is disabled. Note that IFP has a fixed relationship to the SONET/SDH frame; the start of the SPE is determined by the STS (AU) pointer and may change relative to IFP. IFP is sampled on the rising edge of PICLK. The receive composite timing signal (RC1J1V1) indicates the frame, payload and tributary multiframe boundaries on the RECEIVE bus when external path termination is enabled. RC1J1V1 pulses high with the RECEIVE bus payload active signal (RPL) set low to mark the first STS-1 identification byte or equivalently the STM identification byte. RC1J1V1 pulses high with RPL set high to mark the path trace byte (J1). Optionally, the RC1J1V1 signal pulses high with RPL set high on the V1 byte to indicate tributary multiframe boundaries. RC1J1V1 is sampled on the rising edge of RCK.
RPL	Input	32	The RECEIVE bus payload active signal (RPL) indicates when RD[7:0] is carrying a payload byte. It is set high during path overhead and payload bytes and low during transport overhead bytes. RPL is set high during the H3 byte to indicate a negative pointer justification event and set low during the byte following H3 to indicate a positive pointer justification event. RPL is ignored when external path termination is disabled. RPL is sampled on the rising edge of RCK.
RDP	Input	33	The RECEIVE bus data parity signal (RDP) indicates the parity of the RECEIVE bus signals. The RECEIVE data bus (RD[7:0]) is always included in parity calculations. Internal register bits controls the inclusion of the RPL and RC1J1V1 signals in parity calculations and the sense (odd/even) of the parity. RDP is ignored when external path termination is disabled. RDP is sampled on the rising edge of RCK.
RPOHCK[3] RPOHCK[2] RPOHCK[1]	Output	158 157 156	The receive path overhead clocks (RPOHCK[3:1]) provide timing to process the BIPE[3:1] signals, to insert tandem path incoming error count and data link, and to sample the extracted path overhead for the corresponding STS-1 (AU3) stream. RPOHCK[3:1] are nominally 576 kHz clocks. In STS-3c (AU4) mode or STS-1 mode, only RPOHCK[1] is active. RTCEN[3:1], and RTCOH[3:1] are sampled on the rising edge of the corresponding RPOHCK signal. BIPE[3:1], RPOH[3:1] and RPOHFP[3:1] are updated on the falling edge of the corresponding RPOHCK signal. RPOHCK[1] provides timing for the serial receive alarm indication port (RAD), which is updated on the falling edge of RPOHCK[1]. RPOHCK[3:1] are inactive when external path termination is enabled.

Pin Name	Type	Pin No.	Function
RPOH[3] RPOH[2] RPOH[1]	Output	150 149 148	The receive path overhead data signals (RPOH[3:1]) contain the path overhead bytes (J1, B3, C2, G1, F2, H4, Z3, Z4, and Z5) extracted from the path overhead of the corresponding STS-1 (AU3) stream. In STS-3c (AU4) mode or STS-1 mode, only RPOH[1] is active. Each RPOH signal is updated on the falling edge of the corresponding RPOHCK signal. RPOH[3:1] are inactive when external path termination is enabled.
RPOHFP[3] RPOHFP[2] RPOHFP[1]	Output	155 152 151	The receive path overhead frame position signals (RPOHFP[3:1]) may be used to locate the individual path overhead bits in the path overhead data stream for the corresponding STS-1 (AU3) stream. Each RPOHFP[3:1] signal is logic 1 when bit 1 (the most significant bit) of the path trace byte (J1) is present in the corresponding RPOH stream. In STS-3c (AU4) mode or STS-1 mode, only RPOHFP[1] is active. Each RPOHFP signal is updated on the falling edge of the corresponding RPOHCK signal. RPOHFP[1] may be used to located the BIP error count and path FERF indication bits on the receive alarm port data signal (RAD). RPOHFP[1] is logic 1 when the first of eight BIP error positions from the first STS-1 (AU3) or the STS-3c (AU4) stream is present on the receive alarm data signal (RAD). RPOHFP[3:1] are inactive when external path termination is enabled.
RTCEN[3] RTCEN[2] RTCEN[1]	Input	144 143 142	The receive tandem connection overhead insert enable signals (RTCEN[3:1]) control the insertion of incoming error count and data link in the tandem connection maintenance byte (Z5), on a bit-by-bit basis. When RTCEN is set high, the data on the corresponding RTCOH stream is inserted into the associated bit in the Z5 byte. RTCEN has significance only during the the J1 byte positions in the RPOHCK clock sequence and is ignored at all other times. In STS-3c (AU4) mode or STS-1 mode, only RTCEN[1] is significant. RTCEN is sampled on the rising edge of the corresponding RPOHCK signal. RTCEN[3:1] are ignored when external path termination is enabled.
RTCOH[3] RTCOH[2] RTCOH[1]	Input	147 146 145	The receive tandem connection overhead data signals (RTCOH[3:1]) contain the incoming error count and data link message to be inserted into the tandem connection maintenance byte (Z5). When RTCEN is set high, the values sampled on RTCOH is inserted into the Z5 byte. When RTCEN is set low, the IEC field of Z5 reports the incoming path BIP error count and the data link field is set to all ones. In STS-3c (AU4) mode or STS-1 mode, only RTCEN[1] is significant. RTCOH is sampled on the rising edge of the corresponding RPOHCK signal. RTCOH[3:1] are ignored when external path termination is enabled.

Pin Name	Type	Pin No.	Function
BIPE[3] BIPE[2] BIPE[1]	Output	80 79 78	The bit interleaved parity error signals (BIPE[3:1]) signal is set high for one RPOHCK period for each path BIP-8 error detected (up to eight per frame) or once if any of the BIP-8 bits are in error depending on whether BIP-8 errors are treated on a bit or block basis. Path BIP-8 errors are detected by comparing the extracted path BIP-8 byte (B3) with the computed BIP-8 for the previous frame. In STS-3c (AU4) mode or STS-1 mode, only BIP[1] is active. BIPE[3:1] is updated on the falling edge of RPOHCK. BIPE[3:1] are inactive when external path termination is enabled.
RAD	Output	139	The receive alarm port data signal (RAD) contains the path BIP error count and the path FERF status of the three receive STS-1 (AU3) streams or the single STS-3c (AU4) stream. RAD is updated on the falling edge of RPOHCK[1]. RAD is inactive when external path termination is enabled.
LOP[3] LOP[2] LOP[1]	Output	66 65 64	The loss of pointer signals (LOP[3:1]) indicate the loss of pointer state in the associated SONET/SDH stream. LOP is set high when invalid STS pointers are received in eight consecutive frames, or if eight consecutive enabled NDFs are detected in the corresponding STS-1 (AU3) stream. The loss of pointer state is exited (LOP set low) when the same valid STS pointer, with disabled NDF, is detected for three consecutive frames. In STS-3c (AU4) mode, only LOP[1] is active and loss of pointer state (LOP[1]) depends only on the first of three H1, H2 bytes; the value of the concatenation indicators do not affect LOP[1] signal. In STS-1 mode, only LOP[1] is active. LOP[3:1] are updated on the rising edge of PICLK. LOP[3:1] are inactive when external path termination is enabled.
PAIS[3] PAIS[2] PAIS[1]	Output	69 68 67	The path alarm indication signals (PAIS[3:1]) indicate the STS path AIS state associated with the SONET/SDH stream. PAIS is set high when an all ones pattern is observed in the STS-1 pointer bytes (H1, and H2) for three consecutive frames in the corresponding STS-1 (AU3) stream. Path AIS is removed when the same valid pointer with normal NDF is detected for three consecutive frames or a single valid pointer with NDF set is received. In STS-3c (AU4) mode, only PAIS[1] is active and depends only on the first of three H1, H2 bytes; the value of the concatenation indicators do not affect PAIS[1]. In STS-1 mode, only PAIS[1] is active. PAIS[3:1] are updated on the rising edge of PICLK. PAIS[3:1] are inactive when external path termination is enabled.
PFERF[3] PFERF[2] PFERF[1]	Output	72 71 70	The path far end receive failure signals (PFERF[3:1]) indicate the STS path FERF state associated with the SONET/SDH stream. PFERF is set high when the path FERF alarm bit (bit 5) of the STS path status (G1) byte is set high for five consecutive frames. STS path FERF is removed when bit 5 of the G1 byte is set low for five consecutive frames. In STS-3c (AU4) mode and STS-1 mode, only PFERF[1] is active. PFERF[3:1] are updated on the rising edge of PICLK. PFERF[3:1] are inactive when external path termination is enabled.

Pin Name	Type	Pin No.	Function
LOM[3] LOM[2] LOM[1]	Output	77 76 73	The loss of multiframe signals (LOM[3:1]) indicate the tributary multiframe synchronization status associated with the SONET/SDH stream. LOM is set low when a correct sequence has been detected for four consecutive frames. LOM is set high if a correct four frame sequence is not detected in eight frames. In STS-3c (AU4) mode and STS-1 mode, only LOM[1] is active. LOM[3:1] are updated on the rising edge of PICLK. LOM[3:1] are inactive when external path termination is enabled.
DCK	Input	98	The DROP bus clock (DCK) provides timing for the DROP bus interface. DCK is nominally a 19.44 MHz or 6.48 MHz, 50% duty cycle clock. Frequency offsets between PICLK/RCK and DCK are accommodated by pointer justification events on the DROP bus. DFP is sampled on the rising edge of DCK. Outputs DPL, DC1J1V1, DDP and DD[7:0] are updated on the rising edge of DCK.
DFP	Input	97	The active high DROP bus reference frame position signal (DFP) indicates when the first byte of the synchronous payload envelope (SPE byte 1 of STS-1 #1) is available on the DD[7:0] bus. Note that DFP has a fixed relationship to the SONET/SDH frame; the start of the SPE is determined by the STS (AU) pointer and may change relative to DFP. DFP is sampled on the rising edge of DCK.
DPAIS[3:1]	Input	81 82 83	The active high DROP bus path alarm indication signals (DPAIS[3:1]) controls the insertion of path AIS in the DROP bus DD[7:0]. A high level on DPAIS forces the insertion of the all ones pattern into the complete SPE, and the payload pointer bytes (H1, H2, and H3). DROP bus path AIS insertion can also be inserted via register access or in response to ISF code in terminating tandem connection termination equipment applications. In STS-3c (AU4) mode or STS-1 mode, only DPAIS[1] is significant. DPAIS[3:1] is sampled on the rising edge of DCK.
DD[7] DD[6] DD[5] DD[4] DD[3] DD[2] DD[1] DD[0]	Output	87 90 91 92 93 94 95 96	The DROP bus data (DD[7:0]) contains the SONET/SDH receive payload data. The transport overhead bytes, with the exception of the H1, H2 pointer bytes, are set to zeros. The fixed stuff columns in a tributary mapped SPE (VC) may also be optionally set to zero or NPI. DD[7] is the most significant bit (corresponding to bit 1 of each serial word, the first bit transmitted). DD[0] is the least significant bit (corresponding to bit 8 of each serial word, the last bit transmitted). DD[7:0] is updated on the rising edge of DCK.
DPL	Output	85	The active high DROP bus payload active signal (DPL) indicates when the DD[7:0] is carrying a payload byte. It is set high during path overhead and payload bytes and low during transport overhead bytes. DPL is set high during the H3 byte to indicate a negative pointer justification event and set low during the byte following H3 to indicate a positive pointer justification event. DPL is updated on the rising edge of DCK.

Pin Name	Type	Pin No.	Function
DC1J1V1	Output	86	The DROP bus composite timing signal (DC1J1V1) indicates the frame, payload and tributary multiframe boundaries on the DROP data bus DD[7:0]. DC1J1V1 pulses high with the DROP bus payload active signal (DPL) set low to mark the first STS-1 Identification byte or equivalently the STM identification byte (C1). DC1J1V1 pulses high with DPL set high to mark the path trace byte (J1). Optionally, the DC1J1V1 signal pulses high on the V1 byte to indicate tributary multiframe boundaries. DC1J1V1 is updated on the rising edge of DCK.
DDP	Output	84	The DROP bus data parity signal (DDP) indicates the parity of the DROP bus signals. The DROP data bus (DD[7:0]) is always included in parity calculations. The internal register bits control the inclusion of the DPL and DC1J1V1 signals in parity calculation and the sense (odd/even) of the parity. DDP is updated on the rising edge of DCK.
ACK	Input	110	The ADD bus clock (ACK) provides timing for the ADD bus and the GENERATED bus interfaces. ACK is nominally a 19.44 MHz or 6.48 MHz, 50% duty cycle clock. Inputs AD[7:0], APL, AC1J1V1, GFP and GMFP are sampled on the rising edge of ACK. Outputs GPL, GC1J1V1, and GD[1:0] are updated on the rising edge of ACK.
AD[7] AD[6] AD[5] AD[4] AD[3] AD[2] AD[1] AD[0]	Input	111 112 113 114 115 116 117 118	The ADD bus data (AD[7:0]) contains the SONET/SDH transmit payload data. The transport overhead bytes, including the H1, H2 pointer bytes, are ignored. The phase relation of the SPE (VC) to the transport frame is determined by the ADD bus composite timing signal (AC1J1V1). AD[7] is the most significant bit (corresponding to bit 1 of each serial word, the first bit transmitted). AD[0] is the least significant bit (corresponding to bit 8 of each serial word, the last bit transmitted). AD[7:0] is sampled on the rising edge of ACK.
APL	Input	120	The ADD bus payload active signal (APL) indicates when AD[7:0] is carrying a payload byte. It is set high during path overhead and payload bytes and low during transport overhead bytes. APL is set high during the H3 byte to indicate a negative pointer justification event and set low during the byte following H3 to indicate a positive pointer justification event. APL is sampled on the rising edge of ACK.
AC1J1V1	Input	119	The ADD bus composite timing signal (AC1J1V1) identifies the frame, payload and tributary multiframe boundaries on the ADD data bus AD[7:0]. AC1J1V1 pulses high with the ADD bus payload active signal (APL) set low to mark the first STS-1 Identification byte or equivalently the STM identification byte (C1). AC1J1V1 pulses high with APL set high to mark the path trace byte (J1). The AC1J1V1 signal pulses high on the V1 byte to indicate tributary multiframe boundaries. AC1J1V1 is sampled on the rising edge of ACK.

Pin Name	Type	Pin No.	Function
ADP	Input	121	The ADD bus data parity signal (ADP) indicates the parity of the ADD bus signals. The ADD data bus (AD[7:0]) is always included in parity calculations. Internal register bits controls the inclusion of the APL and AC1J1V1 signals in parity calculations and the sense (odd/even) of the parity. ADP is sampled on the rising edge of ACK.
GFP	Input	109	The active high GENERATED bus reference frame position signal (GFP) indicates when the first byte of the synchronous payload envelope (SPE byte 1 of STS-1 #1) is available on the GD[1:0] bus. Note that GFP has a fixed relationship to the SONET/SDH frame; the start of the SPE is determined by the STS (AU) pointer and may change relative to GFP. GFP is sampled on the rising edge of ACK.
GMFP	Input	108	The active high GENERATED reference multiframe position signal (GMFP) is used to align the SONET/SDH tributary multiframe boundary on the GENERATED bus. GMFP should be brought high for a single ACK period every 9720 ACK cycles, or multiples thereof. GMFP may be tied low if such synchronization is not required. A pulse on GMFP realigns the GENERATED bus to be the first of four frames in the multiframe. I.e., the frame containing the V1 bytes. In STS-1 mode, GMFP is sampled one ACK cycle after the J1 indication on GC1J1V1. In STS-3/3c modes, GMFP is sampled three ACK cycles after the J1 indication. GMFP is ignored at other byte positions. GMFP is sampled on the rising edge of ACK.
GD[1] GD[0]	Output	106 107	The GENERATED bus data (GD[1:0]) contains cyclical multiframe count carried in the H4 byte. The sequence is initialized to 'b01 by a high pulse on GMFP, and increments at the byte following J1. GD[1:0] is updated on the rising edge of ACK.
GPL	Output	104	The GENERATED bus payload active signal (GPL) indicates when GD[1:0] is carrying a payload byte. GPL distinguishes between payload and transport overhead timeslots in the GENERATED bus. Since the GENERATED bus is expected to have fixed timing relationship with the ADD bus, access modules may use GPL to locate payload timeslots in the ADD bus. GPL is updated on the rising edge of ACK.
GC1J1V1	Output	105	The GENERATED bus composite timing signal (GC1J1V1) identifies the frame, payload and tributary multiframe boundaries on the GENERATED data bus GD[1:0]. GC1J1V1 pulses high with the GENERATED bus payload active signal (GPL) set low to mark the first STS-1 Identification byte or equivalently the STM identification byte (C1). GC1J1V1 pulses high with GPL set high to mark the path trace byte (J1). The GC1J1V1 signal pulses high on the V1 byte to indicate tributary multiframe boundaries. Since the GENERATED bus is expected to have fixed timing relationship with the ADD bus, access modules may use GC1J1V1 to located the frame, payload and tributary multiframe boundaries on the ADD bus. GC1J1V1 is updated on the rising edge of ACK.

Pin Name	Type	Pin No.	Function
GDP	Output	99	The GENERATED bus data parity signal (GDP) indicates the parity of the GENERATED bus signals. The GENERATED data bus (GD[1:0]) is always included in parity calculations. The internal register bits control the inclusion of the GPL and GC1J1V1 signals in parity calculation and the sense (odd/even) of the parity. GDP is updated on the rising edge of ACK.
TCK	Input	19	The transmit reference clock (TCK) provides timing for SPTX transmit functions. TCK is nominally a 19.44 MHz or 6.48 MHz, 50% duty cycle clock. Frequency offsets between TCK and ACK are accommodated by pointer justification events on the transmit data stream. Inputs TFP, TPAIS[3:1] and TPFERF[3:1] are sampled on the rising edge of TCK. Outputs TD[7:0], TPL, TDP, TC1J1V1 and FPOUT are updated on the rising edge of TCK, while TPOHCLK[3:1] is updated on the falling edge of TCK.
TFP	Input	17	The active high transmit reference frame position (TFP) is used to align the SONET/SDH transport frame generated by the SPTX device to a system reference. TFP indicates when the first byte of the synchronous payload envelope (SPE byte 1 of STS-1 #1) is available on the TD[7:0] bus. TFP should be brought high for a single TCK period every 2430 TCK cycles, or multiples thereof. TFP may be tied low if such synchronization is not required. TFP is sampled on the rising edge of TCK.
TD[7] TD[6] TD[5] TD[4] TD[3] TD[2] TD[1] TD[0]	Output	16 15 12 11 10 9 8 7	The TRANSMIT bus data (TD[7:0]) carries the SONET/SDH frame in byte serial format. The transport overhead bytes, with the exception of H1, H2 pointer bytes, are set to zero. The fixed stuff columns in a tributary based SPE (VC) may be optionally set to zero or NPI. TD[7] is the most significant bit (corresponding to bit 1 of each serial word, the first bit transmitted). TD[0] is the least significant bit (corresponding to bit 8 of each serial word, the last bit transmitted). TD[7:0] is updated on the rising edge of TCK.
TPL	Output	3	The TRANSMIT bus payload active signal (TPL) indicates when TD[7:0] is carrying a payload byte. It is set high during path overhead and payload bytes and low during transport overhead bytes. TPL is set high during the H3 byte to indicate a negative pointer justification event and set low during the byte following H3 to indicate a positive pointer justification event. TPL is updated on the rising edge of TCK.
TC1J1V1	Output	4	The TRANSMIT bus composite timing signal (TC1J1V1) identifies the frame, payload and tributary multiframe boundaries on the TRANSMIT data bus TD[7:0]. TC1J1V1 pulses high with the TRANSMIT bus payload active signal (TPL) set low to mark the first STS-1 Identification byte or equivalently the STM identification byte (C1). TC1J1V1 pulses high with TPL set high to mark the path trace byte (J1). The TC1J1V1 signal pulses high on the V1 byte to indicate tributary multiframe boundaries. TC1J1V1 is updated on the rising edge of TCK.

Pin Name	Type	Pin No.	Function
TDP	Output	2	The TRANSMIT bus parity signal (TDP) indicates the parity of the TRANSMIT bus signals. The TRANSMIT data bus (TD[7:0]) is always included in parity calculations. The internal register bits control the inclusion of the TPL and TC1J1V1 signals in parity calculation and the sense (odd/even) of the parity. TDP is updated on the rising edge of TCK.
TPAIS[3] TPAIS[2] TPAIS[1]	Input	1 160 159	The active high transmit path alarm indication signals (TPAIS[3:1]) controls the insertion of path AIS in the TRANSMIT bus TD[7:0]. A high level on TPAIS forces the insertion of the all ones pattern into the complete SPE, and the payload pointer bytes (H1, H2, and H3). Transmit path AIS insertion can also be inserted via register access or in response to ISF code in terminating tandem connection termination equipment applications. In STS-3c (AU4) mode or STS-1 mode, only TPAIS[1] is significant. TPAIS[3:1] is sampled on the rising edge of TCK.
TPOH[3] TPOH[2] TPOH[1]	Input	124 123 122	The path overhead data signals (TPOH[3:1])... signal contains the path overhead bytes (J1, C2, G1, F2, Z3, Z4, and Z5) and error mask (B3 and H4) which may be inserted, or used to insert multiframe sequence bit errors into the path overhead byte positions in the TRANSMIT bus TD[7:0]. Insertion is controlled by the corresponding TPOHEN input, or by bits in internal registers. In STS-3c (AU4) mode or STS-1 mode, only TPOH[1] is significant. Each TPOH input is sampled on the rising edge of the corresponding TPOHCK output.
TPOHEN[3] TPOHEN[2] TPOHEN[1]	Input	135 134 133	The transmit path overhead insert enable signals (TPOHEN[3:1]), together with internal register bits, control the source of the path overhead data which is inserted in the TRANSMIT bus TD[7:0]. While TPOHEN is high, values sampled on the TPOH input are inserted into the corresponding path overhead bit position (for the J1, C2, G1, F2, Z3, Z4, and Z5 bytes). While TPOHEN is low, values obtained from internal registers are inserted into these path overhead bit positions. A high level on TPOHEN during the B3 bit positions enables an error mask. While the error mask is enabled, a high level on input TPOH causes the corresponding B3 bit position to be inverted. A low level on TPOH allows the corresponding bit position to pass through the SPTX uncorrupted. In STS-3c (AU4) mode or STS-1 mode, only TPOHEN[1] is significant. Each TPOHEN input is sampled on the rising edge of the corresponding TPOHCK output.
TPOHCK[3] TPOHCK[2] TPOHCK[1]	Output	132 131 128	The transmit path overhead clocks (TPOHCK[3:1]) provide timing to update the corresponding path overhead stream, TPOH. In STS-3c (AU4) mode, TPOHCK[1] is a 576kHz clock and TPOHCK[3:2] are inactive. TPOH and TPOHEN are sampled on the rising edge of the corresponding TPOHCLK.
TPOHFP[3] TPOHFP[2] TPOHFP[1]	Output	127 126 125	The path overhead frame position signals (TPOHFP[3:1]) may be used to locate the individual path overhead bits in the overhead data stream, TPOH. TPOHFP is logic 1 when bit 1 (the most significant bit) of the Path Trace byte (J1) is present in the TPOH stream. In STS-3c (AU4) mode or STS-1 mode, only TPOHFP[1] is active. Each TPOHFP output is updated on the falling edge of the corresponding TPOHCK output.

Pin Name	Type	Pin No.	Function
FPOUT	Output	18	The frame pulse output signal (FPOUT) marks the first SPE byte in the TRANSMIT bus TD[7:0] (the byte after the last C1 byte). The transmit frame alignment of peer SPTX devices may be synchronized by connecting the FPOUT signal of the master to the transmit frame pulse input (TFP) of all the SPTX devices in the set. FPOUT is updated on the rising edge of TCK.
TAD	Input	138	The transmit alarm port data signal (TAD) contains the path FEBE error count and the path FERF status of the three associated receive STS-1 (AU3) streams or the single STS-3c (AU4) stream. TAD is sampled on the rising edge of TACK.
TAFP	Input	137	The transmit alarm port frame pulse signal (TAFP) marks the first bit of the transmit alarm message in each SONET (SDH) frame. TAFP is pulsed high to mark the first FEBE bit location of the first STS-1 (AU3) stream or the first FEBE bit location of the single STS-3c (AU4) stream. TAFP is sampled on the rising edge of TACK.
TACK	Input	136	The transmit alarm port clock (TACK) provides timing for transmit alarm port. TACK is nominally a 576 kHz clock. Inputs TAD and TAFP are sampled on the rising edge of TACK.
CSB	Input	46	The active low chip select (CSB) signal is low during SPTX register accesses.
RDB E	Input	58	The active low read enable (RDB) signal is low during SPTX register read accesses. The SPTX drives the D[7:0] bus with the contents of the addressed register while RDB and CSB are low. The active high external access signal (E) is set high during SPTX register access while in Motorola bus mode.
WRB RWB	Input	59	The active low write strobe (WRB) signal is low during a SPTX register write accesses. The D[7:0] bus contents are clocked into the addressed register on the rising WRB edge while CSB is low. The read/write select signal (RWB) selects between SPTX register read and write accesses while in Motorola bus mode. The SPTX drives the data bus D[7:0] with the contests of the addressed register while CSB is low and RWB and E are high. The contents of D[7:0] are clocked into the addressed register on the falling E edge while CSB and RWB are low.
D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7]	I/O	47 48 49 52 53 54 55 56	The bidirectional data bus D[7:0] is used during SPTX register read and write accesses.

Pin Name	Type	Pin No.	Function
A[0] A[1] A[2] A[3] A[4] A[5] A[6] A[7] A[8]/TRS	Input	36 37 38 39 40 41 42 43 44	The address bus A[8:0] selects specific registers during SPTX register accesses. The test register select (TRS) signal selects between normal and test mode register accesses. TRS is high during test mode register accesses, and is low during normal mode register accesses. TRS has an integral pull down resistor.
RSTB	Input	45	The active low reset (RSTB) signal provides an asynchronous SPTX reset. RSTB is a Schmitt triggered input with an integral pull up resistor.
ALE	Input	35	The address latch enable (ALE) is active high and latches the address bus A[8:0] when low. When ALE is high, the internal address latches are transparent. It allows the SPTX to interface to a multiplexed address/data bus. ALE has an integral pull up resistor.
MBEB	Input	34	The active low Motorola bus enable (MBEB) signal configures the SPTX for Motorola bus mode where the RDB/E signal functions as E, and the WRB/RWB signal functions as RWB. When MBEB is high, the SPTX is configured for Intel bus mode where the RDB/E signal functions as RDB. The MBEB input has an integral pull up resistor.
INTB	OD Output	57	The active low interrupt (INTB) signal goes low when a SPTX interrupt source is active, and that source is unmasked. The SPTX may be enabled to report several alarms or events via interrupts. Examples are changes in the loss of pointer state, changes in the path AIS state, changes in the path FERF state, changes in the path status, path BIP-8 error events, FEBE events, pointer adjustment events and pointer error events. INTB returns high when the interrupt is acknowledged via an appropriate register access. INTB is an open drain output.
VDDI1 VDDI2 VDDI3 VDDI4	Power	20 60 101 141	The core power (VDDI1 - VDDI4) pins should be connected to a well decoupled +5 V DC in common with VDDO.
VSSI1 VSSI2 VSSI3 VSSI4	Ground	21 61 100 140	The core ground (VSSI1 - VSSI4) pins should be connected to GND in common with VSSO.

Pin Name	Type	Pin No.	Function
VDDO1	Power	5	The pad ring power (VDDO1 - VDDO9) pins should be connected to a well decoupled +5 V DC in common with VDDI.
VDDO2		13	
VDDO3		51	
VDDO4		62	
VDDO5		74	
VDDO6		89	
VDDO7		103	
VDDO8		130	
VDDO9		154	
VSSO1	Ground	6	The pad ring ground (VSSO1 - VSSO9) pins should be connected to GND in common with VSSI.
VSSO2		14	
VSSO3		50	
VSSO4		63	
VSSO5		75	
VSSO6		88	
VSSO7		102	
VSSO8		129	
VSSO9		153	

Notes on Pin Description:

1. All SPTX inputs and bidirectionals present minimum capacitive loading and operate at TTL logic levels.

2. All SPTX digital outputs and bidirectionals have 2 mA drive capability, except the INTB open drain output and D[7:0] bidirectionals, which have 4 mA drive capability. All outputs use slew rate limited pads.

3. The VSSO and VSSI ground pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage the SPTX.

4. The VDDO and VDDI power pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage the SPTX.

9 FUNCTIONAL DESCRIPTION

9.1 Receive Path Overhead Processor

The Receive Path Overhead Processor (RPOP) provides pointer interpretation, extraction of path overhead, extraction of the synchronous payload envelope (virtual container), and path level alarm and performance monitoring. In tandem path origination mode, RPOP generates an IEC based on its received path BIP-8 errors and inserts the tandem path data link. In tandem path termination mode, RPOP accumulates incoming error counts (IEC) and extracts the tandem connection data link. Optionally, the RPOP will overwrite the fixed stuff columns in a tributary mapped SPE (VC) with zeros or null pointer indications in the NPI bytes.

Diagnostic loopback of the SPTX can be enabled to connect the RPOP receive data stream to the TRANSMIT bus interface of the Transmit Telecombus Aligner block.

9.1.1 Pointer Interpreter

The Pointer Interpreter Block interprets the incoming pointer (H1, H2) as specified in the references. The pointer value is used to determine the location of the path overhead (the J1 byte) in the incoming STS-3c (AU4) or STS-1 (AU3) stream. The algorithm can be modelled by a finite state machine. Within the pointer interpretation algorithm three states are defined (as shown in Figure 3):

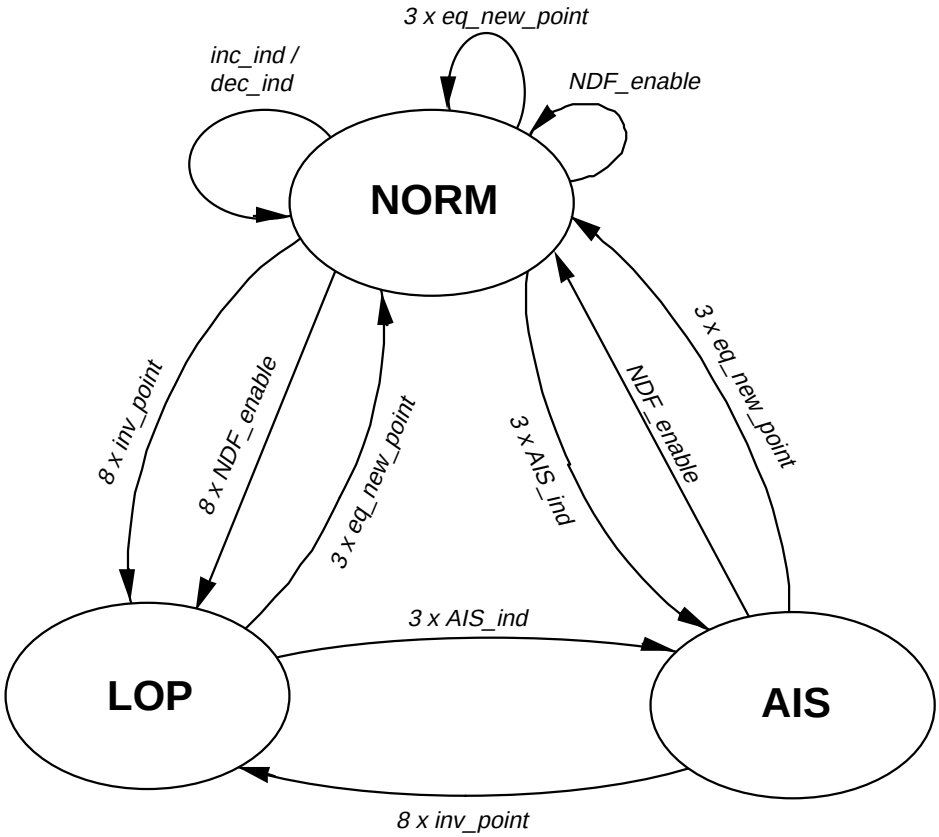
NORM_state (NORM)

AIS_state (AIS)

LOP_state (LOP)

The transition between states will be consecutive events (indications), e.g., three consecutive AIS indications to go from the NORM_state to the AIS_state. The kind and number of consecutive indications activating a transition is chosen such that the behaviour is stable and insensitive to low BER. The only transition on a single event is the one from the AIS_state to the NORM_state after receiving a NDF enabled with a valid pointer value. It should be noted that, since the algorithm only contains transitions based on consecutive indications, this implies that, for example, non-consecutively received invalid indications do not activate the transitions to the LOP_state.

Figure 3 - Pointer Interpretation State Diagram



The following events (indications) are defined

norm_point : disabled NDF + ss + offset value equal to active offset

NDF_enable: enabled NDF + ss + offset value in range of 0 to 782

AIS_ind: H1 = 'hFF, H2 = 'hFF

inc_ind: disabled NDF + ss + majority of I bits inverted + no majority of D bits inverted + previous NDF_enable, inc_ind dec_ind more than 3 frames ago

dec_ind: disabled NDF + ss + majority of D bits inverted + no of I bits inverted + previous NDF_enable, inc_ind dec_ind more than 3 frames ago

inv_point:	not any of above (i.e., not norm_point, and not NDF_enable, and not AIS_ind, and not inc_ind and not dec_ind)
new_point:	disabled_NDF + ss + offset value in range of 0 to 782 but not equal to active offset
inc_req:	disabled NDF + ss + majority of I bits inverted + no majority of D bits inverted
dec_req:	disabled NDF + ss + majority of D bits inverted + no majority of I bits inverted
Note 1.-	active offset is defined as the accepted current phase of the SPE (VC) in the NORM_state and is undefined in the other states.
Note 2 -	enabled NDF is defined as the following bit patterns: 1001, 0001, 1101, 1011, 1000.
Note 3 -	disabled NDF is defined as the following bit patterns: 0110, 1110, 0010, 0100, 0111.
Note 4 -	the remaining six NDF codes (0000, 0011, 0101, 1010, 1100, 1111) result in an inv_point indication.
Note 5 -	ss bits are unspecified in SONET and has bit pattern 10 in SDH
Note 6 -	the use of ss bits in definition of indications may be optionally disabled.
Note 7 -	the requirement for previous NDF_enable, inc_ind or dec_ind be more than 3 frames ago may be optionally disabled.
Note 8 -	new_point is also an inv_point.
Note 9 -	LOP is not declared if all the following conditions exist: the received pointer is out of range (>782), the received pointer is static,

the received pointer can be interpreted, according to voting on the I and D bits, as a positive or negative justification indication,

after making the requested justification, the received pointer continues to be interpretable as a pointer justification.

When the received pointer returns to an in-range value, the SPTX will interpret it correctly.

Note 10 - LOP will exit at the third frame of a three frame sequence consisting of one frame with NDF enabled followed by two frames with NDF disabled, if all three pointers have the same legal value.

The transitions indicated in the state diagram are defined as follows:

inc_ind/dec_ind: offset adjustment (increment or decrement indication)

3 x eq_new_point: three consecutive equal new_point indications

NDF_enable: single NDF_enable indication

3 x AIS_ind: three consecutive AIS indications

8 x inv_point: eight consecutive inv_point indications

8 x NDF_enable eight consecutive NDF_enable indications

Note 1 - the transitions from NORM_state to NORM_state do not represent state changes but imply offset changes.

Note 2 - 3 x new_point takes precedence over 8 x inv_point.

Note 3 - all three offset values received in 3 x eq_new_point must be identical.

Note 4 - "consecutive event counters" are reset to zero on a change of state except for consecutive NDF count.

The Pointer Interpreter Block detects loss of pointer (LOP) in the incoming STS-1 or STS3c stream. LOP is declared on entry to the LOP_state as a result of eight consecutive invalid pointers or eight consecutive NDF enabled indications. Path AIS is inserted in the DROP bus when LOP is declared. The alarm condition is reported in the receive alarm port and is optionally returned to the source node

by signalling the corresponding Transmit Path Overhead Processor in the local SPTX to insert a path FERF indication. Alternatively, if in-band error reporting is enabled, the path FERF bit in DROP bus G1 byte is set to indicate the LOP alarm to the TPOP is a remote SPTX. Path AIS is optionally inserted in the drop bus when LOP is declared.

The Pointer Interpreter Block detects path AIS in the incoming STS-1 or STS-3c stream. PAIS is declared on entry to the AIS_state after three consecutive AIS indications. Path AIS is inserted in the DROP bus when AIS is declared. The alarm condition reported in the receive alarm port and is optionally returned to the source node by signalling the corresponding Transmit Path Overhead Processor in the local SPTX to insert a path FERF indication. Alternatively, if in-band error reporting is enabled, the path FERF bit in DROP bus G1 byte is set to indicate the LOP alarm to the TPOP is a remote SPTX.

Invalid pointer indications (inv_point), invalid NDF codes, new pointer indications (new_point), discontinuous change of pointer alignment, and illegal pointer changes are also detected and reported by the Pointer Interpreter block via register bits. An invalid NDF code is any NDF code that does not match the NDF enabled or NDF disabled definitions. The third occurrence of equal new_point indications (3 x eq_new_point) is reported as a discontinuous change of pointer alignment event (DISCOPA) instead of a new pointer event and the active offset is updated with the receive pointer value. An illegal pointer change is defined as a inc_ind or dec_ind indication that occurs within three frames of the previous inc_ind, dec_ind or NDF_enable indications. Illegal pointer changes may be optionally disabled via register bits.

The active offset value is used to extract the path overhead from the incoming stream and can be read from an internal register.

9.1.2 Multiframe Framer

The multiframe alignment sequence in the path overhead H4 byte is monitored for the bit patterns of 00, 01, 10, 11 in the two least significant bits. If an unexpected value is detected, the primary multiframe will be kept, and a second multiframe process will, in parallel, check for a phase shift. The primary process will enter out of multiframe state (OOM). A new multiframe alignment is chosen, and OOM state is exited when four consecutive correct multiframe patterns are detected. Loss of multiframe (LOM) is declared after residing in the OOM state for eight frames without re-alignment. A new multiframe alignment is chosen, and LOM state is exited when four consecutive correct multiframe patterns are detected.

A spurious LOM alarm can occur if there is a change in the H4 phase and a bit error occurs in frames 5-8 (where frame 1 is the first frame with the new H4 alignment).

9.1.3 SPE Timing

The SPE Timing Block provides SPE timing information to the Error Monitor and the Extract blocks. The block contains a free running timeslot counter that is initialized by a J1 byte identifier (which identifies the first byte of the SPE). Control signals are provided to the Error Monitor and the Extract blocks to identify the Path Overhead bytes.

9.1.4 Error Monitor

The Error Monitor Block contains three 16-bit counters that are used to accumulate path BIP-8 errors (B3), far end block errors (FEBE), and tandem path incoming error counts (IEC). The contents of the counters may be transferred to holding registers, and the counters reset under microprocessor control.

Path BIP-8 errors are detected by comparing the path BIP-8 byte (B3) extracted from the current frame, to the path BIP-8 computed for the previous frame. BIP-8 errors are selectable to be counted as bit errors or as block errors via register bits. When in-band error reporting is enabled, the error count is inserted into the path status byte (G1) of the DROP bus.

FEBEs are detected by extracting the 4-bit FEBE field from the path status byte (G1). The legal range for the 4-bit field is between 0000 and 1000, representing zero to eight errors. Any other value is interpreted as zero errors.

Path FERF alarm is detected by extracting bit 5 of the path status byte. The PFERF signal is set high when bit 5 is set high for five consecutive frames. PFERF is set low when bit 5 is low for five consecutive frames.

IECs are detected by extracting the 4-bit IEC field from the tandem path maintenance byte (Z5). The legal range for the 4-bit field is between 0000 and 1000, representing zero to eight errors. Any other value is interpreted as zero errors.

9.1.5 Path Overhead Extract

The Path Overhead Extract Block uses timing information from the SPE Timing block to extract, serialize and output the Path Overhead bytes on output RPOH.

Output RPOHFP is provided to identify the most significant bit of the path trace byte (J1) on RPOH. The path overhead clock, RPOHCK is nominally a 576 kHz clock. RPOH and RPOHFP are updated with timing aligned to RPOHCLK.

9.1.6 Tandem Connection Originate

The Tandem Connection Originate block updates the path BIP byte (B3) and the tandem connection maintenance byte (Z5) on the DROP bus when RPOP originates a tandem connection. Incoming BIP-8 errors are counted and encoded in the incoming error count field of the Z5 byte. The tandem connection data link is placed into the data link field of the Z5 byte. The B3 byte is updated to reflect the changes made to the Z5 byte. When LOP or path AIS alarms are declared, the incoming error count field of the Z5 byte is set to indicate incoming signal failure (ISF = 'b1111). The H1, H2 pointer bytes are frozen to the previous active offset. Path overhead and payload bytes are set to all ones. The tandem connection data link remains active and the path BIP-8 byte remains valid.

9.1.7 Receive Alarm Port

Received path BIP errors and defect indications (RDI) are communicated to the transmit path overhead processor (TPOP) in a remote SPTX via the receive alarm port. The port carries the count of received path BIP errors. Insertion of path AIS in the DROP bus is reported in the alarm port and will trigger the remote TPOP to signal path FERF in the transmit stream.

9.2 Receive Path Trace Buffer

The receive portion of the SONET Path Trace Buffer (SPTB) captures the received path trace identifier message (J1 bytes) into microprocessor readable registers. It contains two pages of trace message memory. One is designated the capture page and the other the expected page. Path trace identifier data bytes from the receive stream are written into the capture page. The expected identifier message is downloaded by the microprocessor into the expected page. On receipt of a trace identifier byte, it is written into next location in the capture page. The received byte is compared with the data from the previous message in the capture page. An identifier message is accepted if it is received unchanged three times, or optionally, five times. The accepted message is then compared with the expected message. If enabled, an interrupt is generated when the accepted message changes from matching to mismatching the expected message and vice versa. If the current message differs from the previous message the unstable counter is incremented by one. When the unstable count reaches eight, the received message is declared unstable. The received message is declared stable and the unstable counter reset, when the received

message passes the persistency criterion (three or five identical receptions) for being accepted. An interrupt may be optionally generated on entry to and exit from the unstable state. Optionally, path AIS may be inserted in the DROP bus when the receive message is in the mismatched or unstable state.

The length of the path trace identifier message is selectable between 16 bytes and 64 bytes. When programmed for 16 byte messages, the SPTB synchronizes to the byte with the most significant bit set to high and places the byte at the first location in the capture page. When programmed for 64 byte messages, the SPTB synchronizes to the trailing carriage return (CR = 0DH), line feed (LF = 0AH) sequence and places the next byte at the head of the capture page. This enables the path trace message to be appropriately aligned for interpretation by the microprocessor. Synchronization may be disabled, in which case, the memory acts as a circular buffer.

The path signal label (PSL) found in the path overhead byte (C2) is processed. An incoming PSL is accepted when it is received unchanged for five consecutive frames. The accepted PSL is compared with the provisioned value. The PSL match/mismatch state is determined as follows:

Table 2 - Path Signal Label Match/Mismatch

Expected PSL	Accepted PSL	PSLM State
00	00	Match
00	01	Mismatch
00	X ≠ 00	Mismatch
01	00	Mismatch
01	01	Match
01	X ≠ 01	Match
X ≠ 00, 01	00	Mismatch
X ≠ 00, 01	01	Match
X ≠ 00, 01	X	Match
X ≠ 00, 01	Y	Mismatch

Each time an incoming PSL differs from the one in the previous frame, the PSL unstable counter is incremented. Thus, a single bit error in the PSL in a sequence of constant PSL values will cause the counter to increment twice, once on the errored PSL and again on the first error-free PSL. The incoming PSL is

considered unstable, when the counter reaches five. The counter is cleared when the same PSL is received for five consecutive frames.

9.3 Receive Telecombus Aligner

The Receive Telecombus Aligner (RTAL) block takes the payload data from an STS-1 (AU3 or TUG3) stream from the Receive Path Overhead Processor and inserts it in a Telecombus DROP bus. It aligns the frame of the received STS-1 (AU3) stream to the frame of the DROP bus. In an STS-3c (AU4) system, the first STS-1 (TUG3) in a STS-3c (AU4) stream is processed by an RTAL in master mode controlling two RTALs in slave mode. The alignment is accomplished by recalculating the STS (AU) payload pointer value based on the offset between the transport overhead of the receive stream and that of the DROP bus.

Frequency offsets (e.g., due to plesiochronous network boundaries, or the loss of a primary reference timing source) and phase differences (due to normal network operation) between the receive data stream and the DROP bus are accommodated by pointer adjustments in the DROP bus. DROP bus pointer justification events are indicated and are accumulated in the Performance Monitor (PMON) block. Large differences between the number and type of received pointer justification events as indicated by the RPOP block, and pointer justification events generated by the RTAL block may indicate network synchronization failure.

When the RPOP block detect a loss of multiframe, the RTAL may optionally insert all ones in the tributary portion of the SPE. The path overhead column and the fixed stuff columns are unaffected.

The RTAL may optionally insert the tributary multiframe sequence and clear the fixed stuff columns. The tributary multiframe sequence is a four byte pattern ('hFC, 'hFD, 'hFE, 'hFF) applied to the H4 byte. The H4 byte of the frame containing the tributary V1 bytes is set to 'hFD. The fixed stuff columns of a synchronous payload envelope (virtual container) may optionally be over-written all-zeros in the fixed stuff bytes.

9.3.1 Elastic Store

The Elastic Store block perform rate adaptation between the receive data stream and the DROP bus. The entire received payload, including path overhead bytes, is written into in a first-in-first-out (FIFO) buffer at the receive byte rate. Each FIFO word stores a payload data byte and a one bit tag labelling the J1 byte. Receive pointer justifications are accommodated by writing into the FIFO during the negative stuff opportunity byte or by not writing during the positive stuff

opportunity byte. Data is read out of the FIFO in the Elastic Store block at the DROP bus rate by the Pointer Generator block. Analogously, pointer justifications on the DROP bus are accommodated by reading from the FIFO during the negative stuff opportunity byte or by not reading during the positive stuff opportunity byte. The Elastic Store block may be optionally by-passed if the DROP bus is synchronous to receive stream.

The FIFO read and write addresses are monitored. Pointer justification requests will be made to the Pointer Generator block based on the proximity of the addresses relative to programmable thresholds. The Pointer Generator block schedules a pointer increment event if the FIFO depth is below the lower threshold and a pointer decrement event of the depth is above the upper threshold. FIFO underflow and overflow events are detected and path AIS is optionally inserted in the DROP bus for three frames to alert downstream elements of data corruption.

9.3.2 Pointer Generator

The Pointer Generator Block generates the DROP bus pointer (H1, H2) as specified in the references. The pointer value is used to determine the location of the path overhead (the J1 byte) in the DROP bus STS-3 (AU4) or STS-1 (AU3) stream. The algorithm can be modelled by a finite state machine. Within the pointer generator algorithm, five states are defined (as shown in Figure 4):

NORM_state (NORM)

AIS_state (AIS)

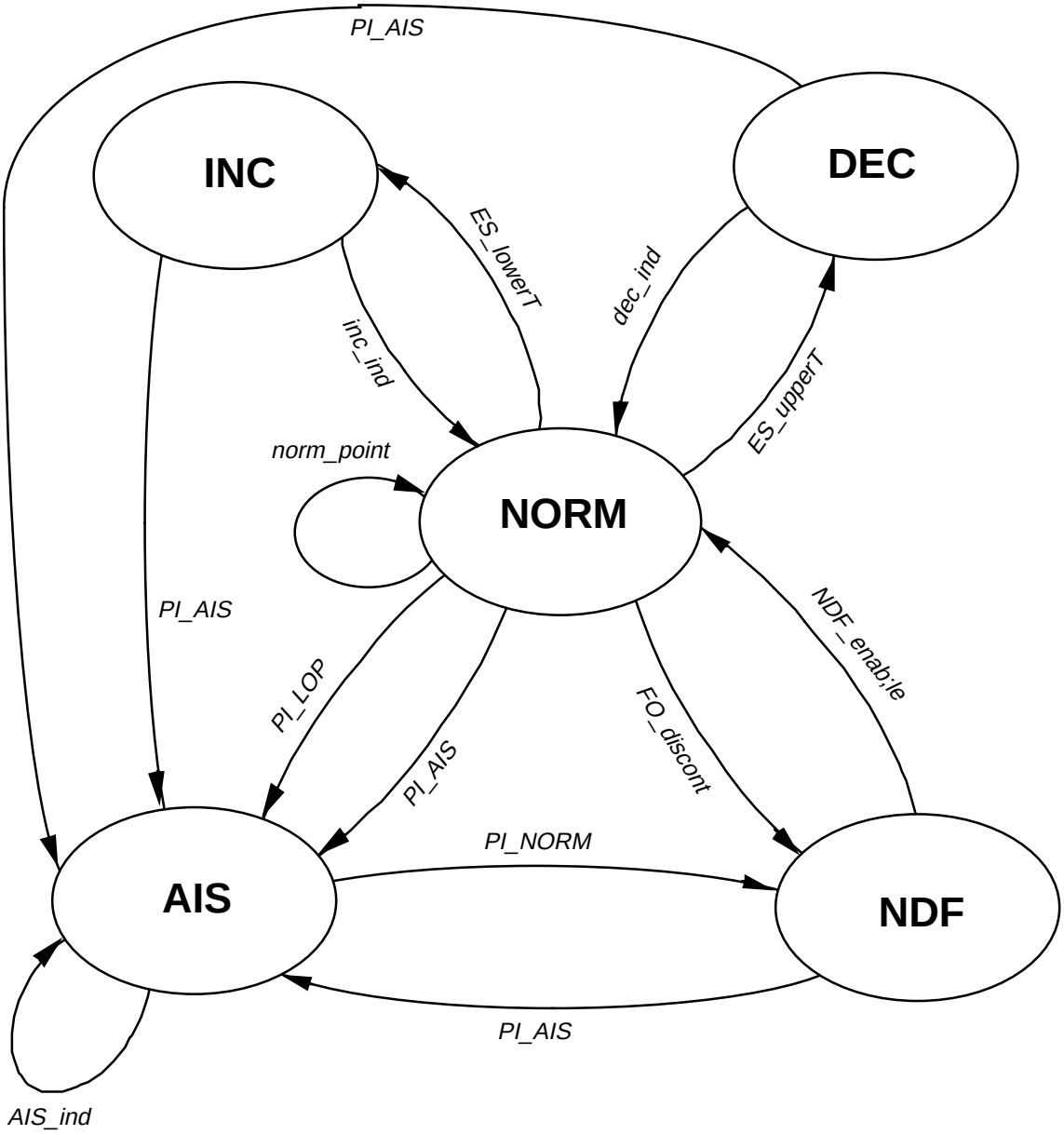
NDF_state (NDF)

INC_state (INC)

DEC_state (DEC)

The transition from the NORM to the INC, DEC, and NDF states are initiated by events in the Elastic Store (ES) block. The transition to/from the AIS state are controlled by the pointer interpreter (PI) in the Receive Path Overhead Processor block. The transitions from INC, DEC, and NDF states to the NORM state occur autonomously with the generation of special pointer pattens.

Figure 4 - Pointer Generation State Diagram



The following events, indicated in the state diagram (Figure 2), are defined:

ES_lowerT: ES filling is below the lower threshold + previous inc_ind, dec_ind or NDF_enable more than three frames ago.

ES_upperT: ES filling is above the upper threshold + previous inc_ind, dec_ind or NDF_enable more than three frames ago.

FO_discont: frame offset discontinuity

PI_AIS: PI in AIS state

PI_LOP: PI in LOP state

PI_NORM: PI in NORM state

Note 1 - A frame offset discontinuity occurs if an incoming NDF enabled isreceived, or if an ES overflow/underflow occurred.

The autonomous transitions indicated in the state diagram are defined as follows:

inc_ind: transmit the pointer with NDF disabled and inverted I bits, transmit a stuff byte in the byte after H3, increment active offset.

dec_ind: transmit the pointer with NDF disabled and inverted D bits, transmit a data byte in the H3 byte, decrement active offset.

NDF_enable: accept new offset as active offset, transmit the pointer withNDF enabled and new offset.

norm_point: transmit the pointer with NDF disabled and active offset.

AIS_ind: active offset is undefined, transmit an all-1's pointer and payload.

Note 1 - active offset is defined as the phase of the SPE (VC).

Note 2 - the ss bits are undefined in SONET, and has bit pattern 10 in SDH

Note 3 - enabled NDF is defined as the bit pattern 1001.

Note 4 - disabled NDF is defined as the bit pattern 0110.

9.3.3 Tandem Connection Alarm

When terminating a tandem connection, the Tandem Connection Alarm block converts Incoming Signal Failure code (ISF) in the tandem connection maintenance byte (Z5) to path AIS in the DROP bus. The ISF code can be optionally filtered so that path AIS is only inserted after detecting ISF in three consecutive frames. Similarly, path AIS is removed after three consecutive frames where ISF is not present. When filtering is disabled, path AIS is

immediately inserted on detection on ISF and removed on detection of inactive ISF code.

9.4 Transmit Path Overhead Processor

The Transmit Path Overhead Processor (TPOP) provides transport frame alignment generation, path overhead insertion, insertion of the synchronous payload envelope, insertion of path level alarm signals and path BIP-8 (B3) insertion. Path overhead insertion is disabled at intermediate tandem connection nodes.

9.4.1 BIP-8 Calculate

The BIP-8 Calculate Block performs a path bit interleaved parity calculation on the SPE (VC) of the outgoing STS-1 (AU3) or STS-3c (AU4) stream. The fixed stuff columns in the VC3 format may be optionally excluded from BIP calculations. The resulting parity byte is inserted in the path BIP-8 (B3) byte position of the subsequent frame. BIP-8 errors may be continuously inserted under register control for diagnostic purposes.

9.4.2 FEBE Calculate

The FEBE Calculate Block accumulates far end block errors on a per frame basis, and inserts the accumulated value (up to maximum value of eight) in the FEBE bit positions of the path status (G1) byte. The FEBE information is derived from path BIP-8 errors detected by the Receive Path Overhead Processor, RPOP. The asynchronous nature of these signals implies that more than eight FEBE events may be accumulated between transmit G1 bytes. If more than eight receive Path BIP-8 errors are accumulated between transmit G1 bytes, the accumulation counter is decremented by eight, and the remaining FEBEs are transmitted at the next opportunity. Alternatively, path FEBE can be accumulated from FEBE error counts reported on the transmit alarm port when the local SPTX is paired with a receive section of a remote SPTX. Far end block errors may be inserted under register control for diagnostic purposes. Optionally, FEBE insertion may be disabled and the incoming G1 byte passes through unchanged to support applications where the received path processing does not reside in the local SPTX.

9.4.3 Transmit Alarm Port

Received path BIP errors and defect indications (RDI) from Receive Path Overhead Processors (RPOP) in a remote SPTX is communicated to the local

SPTX via the transmit alarm port. When the port is enabled, BIP error counts and defect indications are inserted in the FEBE and path FERF positions of the path status byte in the transmit stream.

9.4.4 Path Overhead Insert

The Path Overhead Insert Block provides a bit serial path overhead interface to the TPOP. Any, or all of the path overhead bytes may be sourced from, or modified by the bit serial path overhead stream, TPOH. The individual bits of each path overhead byte are shifted in using the TPOHCLK output. The TPOHFP output is provided to identify when the most significant bit of the Path Trace byte is expected on TPOH. The state of the TPOHEN input, together with an internal register, determines whether the data sampled on TPOH, or the default path overhead byte values are inserted in each STS-1 (AU3) or STS-3c (AU4) stream. For example, a high level on TPOHEN during the path label (C2) bit positions causes the eight values shifted in on TPOH to be inserted in the C2 byte position in the transmit stream. A low level on TPOHEN during the path signal label bit positions causes the default value ('h01) to be inserted. The path trace byte is optionally sourced from the Transmit Path Trace Buffer block.

During the B3 and H4 byte positions in the TPOH stream, a high level on TPOHEN enables an error insertion mask. While the error mask is enabled, a high level on input TPOH causes the corresponding bit in the B3 or H4 byte to be inverted. A low level on TPOH causes the corresponding bit in the B3 or H4 byte to be processed normally without corruption.

9.4.5 SPE Multiplexer

The SPE Multiplexer Block multiplexes the payload pointer bytes, the SPE stream, and the path overhead bytes into the transmit stream. When in-band error reporting is enabled, the FEBE and path FERF bits of the path status (G1) byte has already been formed by the corresponding Receive Path Overhead Processor and is transmitted unchanged.

9.4.6 GENERATED Bus Controller

The GENERATED Bus Controller block provides timing on the GENERATED bus of the SPTX. It controls the GC1J1V1 and GPL signals to indicate the position of the STS (STM) frame and the SPE (VC) within the frame. Downstream access modules may then generate AC1J1V1 and APL based upon this alignment. The phase of the synchronous payload envelope (virtual container) in the GENERATED bus transport frame is indicated by separation of the GC1J1V1

pulse marking the J1 byte from the pulse marking the C1 byte. The relative position of the pulses may be changed by:

1. Discontinuous STS (AU) pointer offsets may be generated by accessing internal SPTX registers If a valid value (i.e., 0 • pointer value • 782) is written to the appropriated SPTX register, the GC1J1V1 pulse indicating J1 will immediately jump to the corresponding byte position. If a value greater than 782 is transferred, the J1 indication pulse remains in its present byte position.

2. Positive pointer movements may be generated by accessing internal SPTX registers. The GPL signal is set low during the positive stuff opportunity byte position, and the GC1J1V1 pulse indicating J1 will be delayed one byte position. Positive pointer movements may be inserted once per frame.

3. Negative pointer movements may be generated by accessing internal SPTX registers. The GPL signal is set high during the negative stuff opportunity byte position (H3), and the GC1J1V1 pulse indicating J1 will be advanced one byte position. Negative pointer movements may be inserted once per frame.

The GENERATED Bus Controller block can be configured to ensure that no positive or negative stuffs occur within three frames of the last pointer event . Discontinuous pointer offset events can still occur in any frame. Positive and negative pointer justifications are provided primarily for diagnostic purposes.

9.5 Transmit Telecombus Aligner

The Transmit Telecombus Aligner (TTAL) block takes the STS-1 SPE (VC3) data from the ADD bus and aligns it to the frame of the transmit stream. In an STS-3c (AU4) system, the first STS-1 (first third of VC4) in the stream is processed by an TTAL in master mode controlling two TTALs in slave mode. The alignment is accomplished by recalculating the STS (AU) payload pointer value based on the offset between the transport overhead of the ADD bus and the transmit stream.

Frequency offsets (e.g., due to plesiochronous network boundaries, or the loss of a primary reference timing source) and phase differences (due to normal network operation) between the ADD and the transmit stream are accommodated by pointer adjustments in the transmit stream.

The TTAL may optionally insert the tributary multiframe sequence and clear the fixed stuff columns. The tributary multiframe sequence is a four byte pattern ('hFC, 'hFD, 'hFE, 'hFF) applied to the H4 byte. The H4 byte of the frame containing the tributary V1 bytes is set to 'hFD. The fixed stuff columns of a

synchronous payload envelope (virtual container) may optionally be over-written with all-zeros in the fixed stuff bytes.

9.5.1 Elastic Store

The Elastic Store block perform rate adaptation between the ADD bus and the transmit stream. The entire ADD bus payload, including path overhead bytes, is written into in a first-in-first-out (FIFO) buffer at the ADD bus byte rate. Each FIFO word stores a payload data byte and a one bit tag labelling the J1 byte. ADD bus pointer justifications are accommodated by writing into the FIFO during the negative stuff opportunity byte or by not writing during the positive stuff opportunity byte. Data is read out of the FIFO in the Elastic Store block at the transmit stream rate by the Pointer Generator block. Analogously, pointer justifications on the transmit stream are accommodated by reading from the FIFO during the negative stuff opportunity byte or by not reading during the positive stuff opportunity byte. The Elastic Store block may be optionally by-passed if the transmit stream is synchronous to ADD bus.

The FIFO read and write addresses are monitored. Pointer justification requests are made to the Pointer Generator block based on the proximity of the addresses relative to programmable thresholds. The Pointer Generator block schedules a pointer increment event if the FIFO depth is below the lower threshold and a pointer decrement event if the depth is above the upper threshold. FIFO underflow and overflow events are detected and path AIS is inserted in the transmit stream for three frames to alert downstream elements of data corruption.

9.5.2 Pointer Generator

The Pointer Generator Block generates the transmit stream pointer (H1, H2) as specified in the references. The pointer value is used to determine the location of the path overhead (the J1 byte) in the transmit STS-3 (AU4) or STS-1 (AU3) stream. The algorithm is identical to that described in the Receive Telecombus Interface block (Figure 4).

9.5.3 Tandem Connection Alarm

In terminating tandem connection termination equipment applications, the Tandem Connection Alarm block converts Incoming Signal Failure code (ISF) in the tandem connection maintenance byte (Z5) to path AIS in the transmit stream. The ISF code can be optionally filtered so that path AIS is only inserted after detecting ISF in three consecutive frames. Similarly, path AIS is removed after three consecutive frames where ISF is not present. When filtering is disabled,

path AIS is immediately inserted on detection of ISF and removed on detection of inactive ISF code.

9.6 Transmit Path Trace Buffer

The transmit portion of the SONET Path Trace Buffer (SPTB) sources the path trace identifier message (J1) for the Transmit Overhead Processor block. The length of the trace message is selectable between 16 bytes and 64 bytes. The SPTB contains one page of transmit trace identifier message memory. Identifier message data bytes are written by the microprocessor into the message buffer and delivered serially to the Transmit Overhead Processor block for insertion in the transmit stream. When the microprocessor is updating the transmit page buffer, SPTB may be programmed to transmit null characters to prevent transmission of partial messages.

9.7 Telecombus Interface

The Telecombus Interface block converts signals defined in the Telecombus standard to those useable by TSBs. It performs multiplexing and demultiplexing functions in STS-3 (AU3) mode to deliver and collect data at STS-1 rate from the three Receive Telecombus Aligner and Transmit Transport Overhead Processors to the STS-3 line rate. To accommodate unequipped application on the ADD bus, the Telecombus Interface block may be programmed to set the ADD bus SPE bytes to all ones. When line loopback is enabled, the Telecombus Interface block replaces the data received on the ADD bus by the data placed on the DROP bus.

9.8 Microprocessor Interface

The microprocessor interface block provides normal and test mode registers, and the logic required to connect to the microprocessor interface. The normal mode registers are required for normal operation, and test mode registers are used to enhance the testability of the SPTX. The register set is accessed as follows:

9.9 Register Memory Map

Table 3 - Register Memory Map

Address	Register
00H	SPTX Master Configuration
01H	SPTX Master Alarm Configuration

Address	Register
02H	SPTX Master Parity Configuration
03H	SPTX Master Reset and Identity
04H	SPTX Master Interrupt Status #1
05H	SPTX Master Interrupt Status #2
06H	SPTX Master Transmit Control
07H	SPTX Master Loopback, ADD Bus Control
08H	SPTX Input Signal Activity Monitor, Accumulation Trigger
09H-0FH	Reserved
10H	RPOP #1, Status and Control
11H	RPOP #1, Alarm Interrupt Status
12H	RPOP #1, Pointer Interrupt Status
13H	RPOP #1, Alarm Interrupt Enable
14H	RPOP #1, Pointer Interrupt Enable
15H	RPOP #1, Pointer LSB
16H	RPOP #1, Pointer MSB
17H	RPOP #1, Path Signal Label
18H	RPOP #1, Path BIP-8 Count LSB
19H	RPOP #1, Path BIP-8 Count MSB
1AH	RPOP #1, Path FEBE Count LSB
1BH	RPOP #1, Path FEBE Count MSB
1CH	RPOP #1, Tributary Multiframe Status and Control
1DH	RPOP #1, Tandem Connection and Ring Control
1EH	RPOP #1, Tandem Connection IEC Count LSB
1FH	RPOP #1, Tandem Connection IEC Count MSB
20H-23H	Reserved
24H	PMON #1, Receive Positive Pointer Justification Count
25H	PMON #1, Receive Negative Pointer Justification Count
26H	PMON #1, Transmit Positive Pointer Justification Count

Address	Register
27H	PMON #1, Transmit Negative Pointer Justification Count
28H	RTAL #1, Control
29H	RTAL #1, Interrupt Status and Control
2AH	RTAL #1, Alarm and DiagnosticControl
2BH	Reserved
2CH- 2FH	Reserved
30H	TPOP #1, Control
31H	TPOP #1, Payload Pointer Control
32H	TPOP #1, Source Control
33H	TPOP #1, Current Pointer LSB
34H	TPOP #1, Current Pointer MSB
35H	TPOP #1, Payload Pointer LSB
36H	TPOP #1, Payload Pointer MSB
37H	TPOP #1, Path Trace
38H	TPOP #1, Path Signal Label
39H	TPOP #1, Path Status
3AH	TPOP #1, Path User Channel
3BH	TPOP #1, Path Growth 1
3CH	TPOP #1, Path Growth 2
3DH	TPOP #1, Path Growth 3
3EH	TPOP #1, Concatenation LSB
3FH	TPOP #1, Concatenation MSB
40H	TTAL #1, Control
41H	TTAL #1, Interrupt Status and Control
42H	TTAL #1, Alarm and Diagnostic Control
43H	Reserved
44H-47H	Reserved
48H	SPTB #1, Control

Address	Register
49H	SPTB #1, Status
4AH	SPTB #1, Indirect Address
4BH	SPTB #1, Indirect Data
4CH	SPTB #1, Expected Path Signal Label
4DH	SPTB #1, Path Signal Label Status
4EH-4FH	Reserved
50H-5FH	RPOP #2 Registers
60H-67H	PMON #2 Registers
68H-6BH	RTAL #2 Registers
6CH-6FH	Reserved
70H-7FH	TPOP #2 Registers
80H-83H	TTAL #2 Registers
84H-87H	Reserved
88H-8FH	SPTB #2 Registers
90H-9FH	RPOP #3 Registers
A0H-A7H	PMON #3 Registers
A8H-ABH	RTAL #3 Registers
ACH-AFH	Reserved
B0H-BFH	TPOP #3 Registers
C0H-C3H	TTAL #3 Registers
C4H-C7H	Reserved
C8H-CFH	SPTB #3 Registers
D0H-FFH	Reserved
100H	Master Test
101H-1FFH	Reserved for Test

For all register accesses, CSB must be low.

10 NORMAL MODE REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the SPTX. Normal mode registers (as opposed to test mode registers) are selected when TRS (A[8]) is low.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic 0. Reading back unused bits can produce either a logic 1 or a logic 0; hence unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the SPTX to determine the programming state of the block.

3. Writeable normal mode register bits are cleared to logic 0 upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect SPTX operation unless otherwise noted.

Register 00H: SPTX Master Configuration

Bit	Type	Function	Default
Bit 7	R/W	TESBYP	0
Bit 6	R/W	RESBYP	0
Bit 5	R/W	EXTPT	0
Bit 4	R/W	MONRS	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	DISV1	0
Bit 1	R/W	CONCAT	0
Bit 0	R/W	STS-1	0

This register allows the operational mode of the SPTX to be configured.

STS-1:

When set high, the STS-1 bit configures the SPTX to process a single STS-1 (AU3) stream. Clock signals (PICLK, DCK, ACK, and TCLK) are at 6.48 MHz. When STS-1 is set low, the SPTX is configured to process an STS-3 (three AU3) streams or an STS-3c (AU4) stream. Clock signals (PICLK, DCK, ACK, and TCLK) are at 19.44 MHz. When in STS-1 mode, outputs RPOH[3:2], RPOHCK[3:2], RPOHFP[3:2], BIPE[3:2], LOP[3:2], PAIS[3:2], PFERF[3:2], LOM[3:2], TPOHCK[3:2], and TPOHFP[3:2] are inactive. Inputs RTCEN[3:2], RTCOH[3:2], TPFERF[3:2], TPAIS[3:2], TPOH[3:2], and TPOHEN[3:2] are ignored.

CONCAT:

When set high, the CONCAT bit configures the SPTX to operate with concatenated payload in the receive and transmit streams, i.e., STS-3c (AU4) streams. When the CONCAT bit is set low, the SPTX operates with non-concatenated payloads, i.e., STS-3 (AU3) streams. CONCAT has no effect when STS-1 is set high. When in STS-3c (AU4) mode, outputs RPOH[3:2], RPOHCK[3:2], RPOHFP[3:2], BIPE[3:2], LOP[3:2], PAIS[3:2], PFERF[3:2], LOM[3:2], TPOHCK[3:2], and TPOHFP[3:2] are inactive. Inputs RTCEN[3:2], RTCOH[3:2], TPFERF[3:2], TPAIS[3:2], TPOH[3:2], and TPOHEN[3:2] are ignored.

DISV1:

When set high, the DISV1 bit configures the DC1J1V1, GC1J1V1, and TC1J1V1 outputs to mark only the frame and synchronous payload envelope (virtual container) alignments (C1 and J1 bytes). DC1J1V1, GC1J1V1, and TC1J1V1 will not indicate the tributary multiframe alignment. When DISV1 is set low, DC1J1V1, GC1J1V1, and TC1J1V1 mark all three of the frame, payload envelope and tributary multiframe alignments.

Reserved:

The Reserved register bit must be written to logical low for correct operation of the SPTX.

EXTPT:

When set high, the EXTPT bit configures the SPTX to operate in external path termination mode. The internal receiver path overhead processor is disabled. The receive data is taken from the RECEIVE bus. Transport overhead and payload bytes are distinguished by the RPL input. Frame and SPE alignment are identified by the RC1J1V1 input. Performance monitoring related to the incoming pointer and the path overhead column is disabled. When EXTPT is set low, the internal path overhead processor terminates the path of the receive stream. Inputs RPL and RDP are ignored.

MONRS:

When set high, the MONRS selects the receive side pointer justification events counters to monitor the receive stream directly. When MONRS is set low, the counters accumulates pointer justification events on the DROP bus.

RESBYP:

When set high, the RESBYP bits forces the elastic store in the Receive Telecombus Aligner to be bypassed. The DROP bus stream will be synchronous to the receive stream. The DCK input will be ignored and circuitry timed by DCK will be clocked by PICLK. The transport frame on the DROP bus will be locked to the receive stream and the DFP input is ignored. RESBYP must be set low when EXTPT is set high.

TESBYP:

When set high, the TESBYP bits forces the elastic store in the Transmit Telecombus Aligner to be bypassed. The transmit stream will be synchronous to the ADD bus. The TCK input will be ignored and circuitry timed by TCK will be clocked by ACK. The transport frame in the transmit stream will be locked to that on the ADD bus and the TFP input is ignored.

Register 01H: SPTX Master Alarm Configuration

Bit	Type	Function	Default
Bit 7	R/W	RXSEL[1]	0
Bit 6	R/W	RXSEL[0]	0
Bit 5	R/W	PSLUAIS	1
Bit 4	R/W	PSLMAIS	1
Bit 3	R/W	LOPAIS	1
Bit 2	R/W	LOMAIS	1
Bit 1	R/W	TIUAIS	1
Bit 0	R/W	TIMAIS	1

This register allows the operational mode of the SPTX to be configured.

TIMAIS:

When set high, the TIMAIS bit enables path AIS insertion on the DROP bus when path trace message mismatch (TIM) events are detected in the receive stream. When TIMAIS is set low, trace identifier mismatch events have no effect on the DROP bus.

TIUAIS:

When set high, the TIUAIS bit enables path AIS insertion on the DROP bus when path trace message unstable (TIU) events are detected in the receive stream. When TIUAIS is set low, trace identifier mismatch events have no effect on the DROP bus.

LOMAIS:

When set high, the LOMAIS bit enables tributary path AIS insertion on the DROP bus when loss of multiframe (LOM) events are detected in the receive stream. The path overhead (POH), the fixed stuff, and the pointer bytes (H1, H2) are unaffected. When LOMAIS is set low, loss of multiframe events have no effect on the DROP bus.

LOPAIS:

When set high, the LOPAIS bit enables path AIS insertion on the DROP bus when loss of pointer (LOP) events are detected in the receive stream. When LOPAIS is set low, loss of pointer events have no effect on the DROP bus.

PSLMAIS:

When set high, the PSLMAIS bit enables path AIS insertion on the DROP bus when path signal label mismatch (PSLM) events are detected in the receive stream. When PSLMAIS is set low, path signal label mismatch events have no effect on the DROP bus.

PSLUAIS:

When set high, the PSLUAIS bit enables path AIS insertion on the DROP bus when path signal label unstable (PSLU) events are detected in the receive stream. When PSLUAIS is set low, path signal label unstable events have no effect on the DROP bus.

RXSEL0-RXSEL1:

The RXSEL[1:0] bits controls the source of the associated receive section of the transmit stream. When RXSEL[1:0] is set to 'b00, the receive section is chosen to be one in the local SPTX. The path FEBE count and path FERF status of the transmit stream is taken from the local RPOP. When RXSEL[1:0] is set to 'b01, a remote receive section is chosen and it reports the detected path BIP-8 error count and the path AIS status of its DROP bus via the transmit alarm port. The path status byte in the transmit stream carries the path FEBE and path FERF indications reported in the transmit alarm port. When RXSEL[1:0] is set to 'b10, inband error reporting is chosen. The associated receive section forms a new G1 byte reporting on the path BIP-8 errors detected and path AIS status. The local transmit section pass the FEBE and path FERF bits on the ADD bus to the transmit stream unmodified. When RXSEL[1:0] is set to 'b11, the path status byte in the transmit stream is not associate with any receive stream. No FEBE nor path FERF will be reported.

Register 02H: SPTX Master Parity Configuration

Bit	Type	Function	Default
Bit 7	R	RPI	X
Bit 6	R/W	RPE	0
Bit 5	R	API	X
Bit 4	R/W	APE	0
Bit 3	R/W	OODPG	0
Bit 2	R/W	ODDPC	0
Bit 1	R/W	INCPL	0
Bit 0	R/W	INCC1J1V1	0

This register allows the parity insertion in the ADD and GENERATED busses of the SPTX to be configured.

INCC1J1V1:

The INCC1J1V1 bit controls the whether the composite timing signals (AC1J1V1, DC1J1V1, GC1J1V1,RC1J1V1,TC1J1V1) in the ADD, DROP and GENERATED busses are used to calculate the corresponding parity signals (ADP, DDP, GDP). When INCC1J1V1 is set high, the parity signal set includes the C1J1V1 signal. When INCC1J1V1 is set low, parity is calculated without regard to the state of the corresponding C1J1V1 signal on the three busses.

INCPL:

The INCPL bit controls the whether the payload active signal (APL, DPL, GPL,RPL,TPL) in the ADD, DROP and GENERATED busses are used to calculate the corresponding parity signals (ADP, DDP, and GDP, respectively). When INCPL is set high, the parity signal set includes the PL signal. When INCPL is set low, parity is calculated without regard to the state of the corresponding PL signal on the three busses.

ODDPC:

The ODDPC bit controls the parity expected on the RECEIVE, and ADD bus parity signals (RDP, ADP). When set high, the ODDPC bit configures the bus parity including the corresponding parity signal to be odd. When set low, the ODDPC bit configures the bus parity to be even.

ODDPG:

The ODDPG bit controls the parity placed on the DROP bus, GENERATED bus, and TRANSMIT bus parity signals (DDP, GDP, TDP). When set high, the ODDPG bit configures the bus parity including the corresponding parity signal to be odd. When set low, the ODDPG bit configures the bus parity to be even.

APE:

The APE bit controls the assertion of interrupts when a parity error is detected in the ADD bus. When APE is set high, an interrupt will be asserted (INTB set low) when a parity error has been detected in the ADD bus. When APE is set low, ADD bus parity errors will not affect the interrupt output.

API:

The ADD bus parity interrupt status bit (API) reports the status of the ADD bus parity interrupt. API is set high on detection of a parity error on the ADD bus. This bit and the interupt are cleared when this register is read.

RPE:

The RPE bit controls the assertion of interrupts when a parity error is detected in the RECEIVE bus. When RPE is set high, an interrupt will be asserted (INTB set low) when a parity error has been detected in the RECEIVE bus. When RPE is set low, RECEIVE bus parity errors will not affect the interrupt output.

RPI:

The RECEIVE bus parity interrupt status bit (RPI) reports the status of the RECEIVE bus parity interrupt. RPI is set high on detection of a parity error on the RECEIVE bus. This bit and the interupt are cleared when this register is read.

Register 03H: SPTX Master Reset and Identity

Bit	Type	Function	Default
Bit 7	R/W	RESET	0
Bit 6	R	ID[6]	0
Bit 5	R	ID[5]	0
Bit 4	R	ID[4]	0
Bit 3	R	ID[3]	0
Bit 2	R	ID[2]	0
Bit 1	R	ID[1]	0
Bit 0	R	ID[0]	1

This register allows the revision of the SPTX to be read by software permitting graceful migration to support for newer, feature enhanced versions of the SPTX, should revision of the SPTX occur. It also provides software reset capability.

ID[6:0]:

The ID bits can be read to provide a binary SPTX revision number.

RESET:

The RESET bit allows the SPTX to be reset under software control. If the RESET bit is a logic 1, the entire SPTX is held in reset. This bit is not self-clearing. Therefore, a logic 0 must be written to bring the SPTX out of reset. Holding the SPTX in a reset state places it into a low power, stand-by mode. A hardware reset clears the RESET bit, thus negating the software reset. Otherwise the effect of a software reset is equivalent to that of a hardware reset.

Register 04H: SPTX Master Interrupt Status #1

Bit	Type	Function	Default
Bit 7	R	DPAIS	X
Bit 6		Unused	X
Bit 5	R	RPOP3I	0
Bit 4	R	RPOP2I	0
Bit 3	R	RPOP1I	0
Bit 2	R	RTAL3I	0
Bit 1	R	RTAL2I	0
Bit 0	R	RTAL1I	0

This register, together with the SPTX Master Interrupt Status #2 register, allow the source of an active interrupt to be identified down to the block level. Further register accesses to the block in question are required in order to determine each specific cause of an active interrupt and to acknowledge each interrupt source.

RTALnI:

The RTALnI bits are high when an interrupt request is active from the corresponding RTAL block.

RPOPnI:

The RPOPnI bits are high when an interrupt request is active from the corresponding RPOP block.

DPAIS:

The DROP bus alarm indiction signal (DPAIS) bit is set high when path AIS is inserted in the DROP bus. In STS-3 mode, DPAIS is set high when AIS is inserted in any of the three STS-1 streams

These register bits are not cleared on read.

Register 05H: SPTX Master Interrupt Status #2

Bit	Type	Function	Default
Bit 7	R	TPAIS	X
Bit 6		Unused	X
Bit 5	R	TTAL3I	0
Bit 4	R	TTAL2I	0
Bit 3	R	TTAL1I	0
Bit 2	R	SPTB3I	0
Bit 1	R	SPTB2I	0
Bit 0	R	SPTB1I	0

This register, together with the SPTX Master Interrupt Status #1 register, allow the source of an active interrupt to be identified down to the block level. Further register accesses to the block in question are required in order to determine each specific cause of an active interrupt and to acknowledge each interrupt source.

SPTBnI:

The SPTBnI bits are high when an interrupt request is active from the corresponding SPTB block.

TTALnI:

The TTALnI bits are high when an interrupt request is active from the corresponding TTAL block.

TPAIS

The transmit stream alarm indiction signal (TPAIS) bit is set high when path AIS is inserted in the transmit stream. In STS-3 mode, TPAIS is set high when AIS is inserted in any of the three STS-1 streams

These register bits are not cleared on read.

Register 06H: SPTX Master Transmit Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	TDIS3	0
Bit 4	R/W	TDIS2	0
Bit 3	R/W	TDIS1	0
Bit 2	R/W	TPTB3EN	0
Bit 1	R/W	TPTB2EN	0
Bit 0	R/W	TPTB1EN	0

This register controls the insertion of path overhead in the transmit stream.

TPTBnEN:

The TPTBnEN bits controls whether the path trace message stored in the TPTB block is inserted in the transmit stream. When TPTBnEN is set high, the message in the corresponding transmit path trace buffer (TPTB) is inserted in the transmit stream. When TPTBnEN is set low, the path trace message is supplied by the TPOP block or via the corresponding TPOH input. The TPTBnEN bits must be set low and the serial TPOH stream must be disable to prevent path trace insertion at intermediate tandem connection nodes.

TDISn:

The TDISn bits controls the insertion of path overhead bytes in the transmit stream. When TDIS is set high, the path overhead bytes of the corresponding transmit stream is sourced from the ADD bus. Serial path overhead insertion and corruption via the TPOH input is still available. However, setting TPOHEN high during the B3 byte field corrupts the transmitted byte in an unpredictiable fashion. All other POH bytes may be modified via the TPOH inputs as controlled by the TPOP source control register bits and the TPOHEN input normally. When TDIS is set low, path overhead is processed normally. The TDISn bits must be set high and the TPOHEN[3:1] inputs set low to disable path overhead insertion at intermediate tandem connection nodes.

Register 07H: SPTX Master Loopback, ADD Bus Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	LLBEN	0
Bit 3	R/W	DLBEN	0
Bit 2	R/W	ADDUE3	0
Bit 1	R/W	ADDUE2	0
Bit 0	R/W	ADDUE1	0

This register provides control of line and diagnostic loopback of the SPTX.

LLBEN:

When set high, the line loopback enable bit (LLBEN) activates line loopback in the SPTX. Data from the receive stream propagates to the DROP bus and replaces the data on the ADD bus. When LLBEN is set low, line loopback is disabled, data on the ADD bus is transmitted on the transmit stream.

DLBEN:

When set high, the diagnostic loopback enable bit (DLBEN) activates diagnostic loopback in the SPTX. Data from the ADD bus propagates to the transmit stream and replaces the data on the receive stream. When DLBEN is set low, diagnostic loopback is disabled, data on the receive stream is propagated to the DROP bus.

ADDUEn:

When set high, the ADDUEn bits configure the corresponding STS-1 (AU3) stream in the ADD bus as unequipped. Payload bytes from that STS-1 stream are overwritten with all-ones. When ADDUEn is set low, the STS-1 stream is equipped and carrying valid data.

Register 08H: SPTX Master Signal Activity Monitor, Accumulation Trigger

Bit	Type	Function	Default
Bit 7	R	PINA	X
Bit 6	R	IFPA/RCA	X
Bit 5	R	ADA	X
Bit 4	R	ACA	X
Bit 3	R	TCKA	X
Bit 2	R	PICLKA	X
Bit 1	R	DCKA	X
Bit 0	R	ACKA	X

This register provides activity monitoring on major SPTX inputs. When a monitored input makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point, all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read periodically to detect stuck at conditions.

Writing to this register delimits accumulation intervals in the PMON and RPOP accumulation registers. Counts accumulated in those registers are transferred to holding registers where they can be read. The counters themselves are then cleared to begin accumulating the associated events for the new accumulation interval. The bits in this register are not affected by write accesses.

ACKA:

The ACK active (ACKA) bit monitors for low to high transitions on the ACK input. ACKA is set high on a rising edge of ACK, and is set low when this register is read.

DCKA:

The DCK active (DCKA) bit monitors for low to high transitions on the DCK input. DCKA is set high on a rising edge of DCK, and is set low when this register is read.

PICLKA:

The PICLK active (PICLKA) bit monitors for low to high transitions on the PICLK input. PICLKA is set high on a rising edge of PICLK, and is set low when this register is read.

TCKA:

The TCK active (TCKA) bit monitors for low to high transitions on the TCK input. TCKA is set high on a rising edge of TCKA, and is set low when this register is read.

ACA:

The ADD bus control active (ACA) bit monitors for low to high transitions on the APL, AC1J1V1 and ADP inputs. ACA is set high when rising edges have been observed on all three signals, and is set low when this register is read.

ADA:

The ADD bus data active (ADA) bit monitors for low to high transitions on the AD[7:0] bus. ADA is set high when rising edges have been observed on all the signals in AD[7:0], and is set low when this register is read.

IFPA/RCA:

When external path termination is disabled (EXPPT low the IFP active (IFPA) bit monitors for low to high transitions on the IFP input. IFPA is set high on a rising edge of IFP, and is set low when this register is read. When external path termination is enabled, the RECEIVE bus control active (RCA) bit monitors for low to high transitions on the RPL, RC1J1V1 and RDP inputs. RCA is set high when rising edges have been observed on all three signals, and is set low when this register is read.

PINA:

The receive data active (PINA) bit monitors for low to high transitions on the PIN[7:0] bus. PINA is set high when rising edges have been observed on all the signals in PIN[7:0], and is set low when this register is read.

Register 10H, 50H, 90H: RPOP Status and Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R	LOPCON	X
Bit 5	R	LOP	X
Bit 4	R	PAISCON	X
Bit 3	R	PAIS	X
Bit 2	R	PFERF	X
Bit 1	R	NEWPTRI	X
Bit 0	R/W	NEWPTRE	0

This register provides configuration and reports the status of the corresponding RPOP.

NEWPTRE:

When a 1 is written to the NEWPTRE interrupt enable bit position, the reception of a new_point indication will activate the interrupt (INT) output.

NEWPTRI:

The NEWPTRI bit is set to logic 1 when a new_point indication is received. This bit (and the interrupt) are cleared when this register is read.

PFERF:

The path FERF status bit (PFERF) indicates reception of path FERF alarm in the receive stream.

PAIS:

The path AIS status bit (PAIS) indicates reception of path AIS alarm in the receive stream.

PAISCON:

The concatenation path AIS status bit (PAISCON) indicates reception of path AIS alarm in the concatenation indicator in the receive stream.

LOP:

The loss of pointer status bit (LOP) indicates entry to the LOP_state in the RPOP pointer interpreter state machine.

LOPCON:

The concatenated loss of pointer status bit (LOPCON) indicates entry to LOP_state for the concatenated streams in the RPOP pointer interpreter.

Reserved:

The Reserved bit must be programmed to logic zero for proper operation of the SPTX

Register 11H, 51H, 91H: RPOP Alarm Interrupt Status

Bit	Type	Function	Default
Bit 7	R	Reserved	X
Bit 6	R	LOPCONI	X
Bit 5	R	LOPI	X
Bit 4	R	PAISCONI	X
Bit 3	R	PAISI	X
Bit 2	R	PFERFI	X
Bit 1	R	BIPEI	X
Bit 0	R	FEBEI	X

This register allows identification and acknowledgement of path level alarm and error event interrupts.

FEBEI

The FEBE interrupt status bit (FEBEI) is set high when a path FEBE is detected.

BIPEI:

The BIP error interrupt status bit (BIPEI) is set high when a path BIP-8 error is detected.

PFERFI, PAISI, PAISCONI, LOPI, LOPCONI:

The PFERFI, PAISI, PAISCONI, LOPI and LOPCONI interrupt status bits are set high on assertion and removal of the corresponding alarm states.

Reserved:

The Reserved bit is an interrupt status bit and must be ignored when this register is read.

These bits (and the interrupt) are cleared when the this register is read.

Register 12H, 52H, 92H: RPOP Pointer Interrupt Status

Bit	Type	Function	Default
Bit 7	R	ILLJREQI	X
Bit 6	R	CONCATI	X
Bit 5	R	DISCOPAI	X
Bit 4	R	INVNDFI	X
Bit 3	R	Reserved	X
Bit 2	R	NSEI	X
Bit 1	R	PSEI	X
Bit 0	R	NDFI	X

This register allows identification and acknowledgement of pointer event interrupts.

NDFI:

The NDF enabled indication interrupt status bit (NDFI) is set high when one of the NDF enable patterns is observed in the receive stream.

PSEI, NSEI:

The positive and negative justification event interrupt status bits (PSEI, NSEI) are set high when the RPOP block responds to an inc_ind or dec_ind indication, respectively, in the receive stream.

Reserved:

The Reserved bit is an interrupt status bit and must be ignored when this register is read.

INVNDFI:

The invalid NDF interrupt status bit (NDFI) is set high when an invalid NDF code is observed on the receive stream.

DISCOPAI:

The discontinuous pointer change interrupt status bit (DISCOPAI) is set high when the RPOP active offset is changed due to receiving the same valid pointer for three consecutive frames (3 x eq_new_point indication).

ILLJREQI:

The illegal justification request interrupt status bit (ILLJREQI) is set high when the RPOP detects a positive or negative pointer justification request (inc_req, dec_req) that occurs within three frames of a previous justification event (inc_ind, dec_ind) or an active offset change due to an NDF enable indication (NDF_enable).

CONCATI:

The concatenation indication error interrupt status bit (CONCATI) is set high when the SPTX is operating in concatenation mode and an error is detected in the concatenation indicators of STS-1 #2 and STS-1 #3.

These bits (and the interrupt) are cleared when this register is read.

Register 13H, 53H, 93H: RPOP Alarm Interrupt

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	LOPCONE	0
Bit 5	R/W	LOPE	0
Bit 4	R/W	PAISCONE	0
Bit 3	R/W	PAISE	0
Bit 2	R/W	PFERFE	0
Bit 1	R/W	BIPEE	0
Bit 0	R/W	FEBEE	0

This register allows interrupt generation to be enabled or disabled for alarm and error events.

FEBEE:

When a 1 is written to the FEBEE interrupt enable bit position, the reception of one or more FEBEs will activate the interrupt (INTB) output.

BIPEE:

When a 1 is written to the BIPEE interrupt enable bit position, the detection of one or more path BIP-8 errors will activate the interrupt (INTB) output.

PFERFE:

When a 1 is written to the PFERFE interrupt enable bit position, a change in the path FERF state will activate the interrupt (INTB) output.

PAISE:

When a 1 is written to the PAISE interrupt enable bit position, a change in the path AIS state will activate the interrupt (INTB) output.

PAISCONE:

When a 1 is written to the PAISCONE interrupt enable bit position, a change in the concatenation path AIS state will activate the interrupt (INTB) output.

LOPE:

When a 1 is written to the LOPE interrupt enable bit position, a change in the loss of pointer state will activate the interrupt (INTB) output.

LOPCONE:

When a 1 is written to the LOPCONE interrupt enable bit position, a change in the concatenation loss of pointer state will activate the interrupt (INT) output.

Reserved:

The Reserved bit imust be set low for correct operation of the SPTX.

Register 14H, 54H, 94H: Pointer Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	ILLJREQE	0
Bit 6	R/W	CONCATE	0
Bit 5	R/W	DISCOPAE	0
Bit 4	R/W	INVNDFE	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	NSEE	0
Bit 1	R/W	PSEE	0
Bit 0	R/W	NDFE	0

This register allows interrupt generation to be enabled or disabled for pointer events.

NDFE:

When a 1 is written to the NDFE interrupt enable bit position, the detection of an NDF_enable indication will activate the interrupt (INTB) output.

PSEE:

When a 1 is written to the PSEE interrupt enable bit position, a positive pointer adjustment event will activate the interrupt (INTB) output.

NSEE:

When a 1 is written to the NSEE interrupt enable bit position, a negative pointer adjustment event will activate the interrupt (INTB) output.

Reserved:

The Reserved bit must be programmed to logic zero for proper operation of the SPTX.

INVNDFE:

When a 1 is written to the INVNDFE interrupt enable bit position, an invalid NDF code will activate the interrupt (INTB) output.

DISCOPAE:

When a 1 is written to the DISCOPAE interrupt enable bit position, a change of pointer alignment event will activate the interrupt (INTB) output.

CONCATE:

When a 1 is written to the CONCATE interrupt enable bit position, an invalid Concatenation Indicator event will activate the interrupt (INTB) output.

ILLJREQE:

When a 1 is written to the ILLJREQE interrupt enable bit position, an illegal pointer justification request will activate the interrupt (INTB) output.

Register 15H, 55H, 95H: RPOP Pointer LSB

Bit	Type	Function	Default
Bit 7	R	PTR7	X
Bit 6	R	PTR6	X
Bit 5	R	PTR5	X
Bit 4	R	PTR4	X
Bit 3	R	PTR3	X
Bit 2	R	PTR2	X
Bit 1	R	PTR1	X
Bit 0	R	PTR0	X

The register reports the lower eight bits of the active offset.

PTR7-PTR0:

The PTR7 - PTR0 bits contain the eight LSBs of the active offset value as derived from the H1 and H2 bytes. To ensure reading a valid pointer, the NDFI, NSEI and PSEI bits of the RPOP Pointer Interrupt Status register should be read before and after reading this register to ensure that the pointer value did not changed during the register read.

Register 16H, 56H, 96H: RPOP Pointer MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	CONCAT	X
Bit 3	R	S1	X
Bit 2	R	S0	X
Bit 1	R	PTR9	X
Bit 0	R	PTR8	X

This register reports the upper two bits of the active offset, the SS bits in the receive pointer.

PTR9 - PTR8:

The PTR9 - PTR8 bits contain the two MSBs of the current pointer value as derived from the H1 and H2 bytes. Thus, to ensure reading a valid pointer, the NDFI, NSEI and PSEI bits of the Pointer Interrupt Status register should be read before and after reading this register to ensure that the pointer value did not changed during the register read.

S0, S1:

The S0 and S1 bits contain the two S bits received in the last H1 byte.These bits should be software debounced.

CONCAT:

The CONCAT bit is set high if the H1, H2 pointer byte received matches the concatenation indication (one of the five NDF_enable patterns in the NDF field, don't care in the size field, and all-ones in the pointer offset field).

Register 17H, 57H, 97H: RPOP Path Signal Label

Bit	Type	Function	Default
Bit 7	R	PSL7	X
Bit 6	R	PSL6	X
Bit 5	R	PSL5	X
Bit 4	R	PSL4	X
Bit 3	R	PSL3	X
Bit 2	R	PSL2	X
Bit 1	R	PSL1	X
Bit 0	R	PSL0	X

This register reports the path label byte in the receive stream.

PSL7 - PSL0:

The PSL7 - PSL0 bits contain the path signal label byte (C2). The value in this register is updated to a new path signal label value if the same new value is observed for three consecutive frames.

Register 18H, 58H, 98H: RPOP Path BIP-8 LSB

Bit	Type	Function	Default
Bit 7	R	BE7	X
Bit 6	R	BE6	X
Bit 5	R	BE5	X
Bit 4	R	BE4	X
Bit 3	R	BE3	X
Bit 2	R	BE2	X
Bit 1	R	BE1	X
Bit 0	R	BE0	X

This register reports the lower eight bits.of the BIP-8 error counter.

Register 19H, 59H, 99H: Path BIP-8 MSB

Bit	Type	Function	Default
Bit 7	R	BE15	X
Bit 6	R	BE14	X
Bit 5	R	BE13	X
Bit 4	R	BE12	X
Bit 3	R	BE11	X
Bit 2	R	BE10	X
Bit 1	R	BE9	X
Bit 0	R	BE8	X

This register reports the upper eight bits of the BIP-8 error counter.

BE0 - BE15:

Bits BE0 through BE15 represent the number of path bit-interleaved parity errors that have been detected since the last time the path BIP-8 registers were polled by writing to the SPTX Accumulation Trigger register. The write access transfers the internally accumulated error count to the path BIP-8 registers within twelve PICLK cycles (or ~ 1 µs) and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Register 1AH, 5AH, 9AH: RPOP FEBE LSB

Bit	Type	Function	Default
Bit 7	R	FE7	X
Bit 6	R	FE6	X
Bit 5	R	FE5	X
Bit 4	R	FE4	X
Bit 3	R	FE3	X
Bit 2	R	FE2	X
Bit 1	R	FE1	X
Bit 0	R	FE0	X

This register reports the lower eight bits of the FEBE accumulation counter.

Register 1BH, 5BH, 9BH: RPOP FEBE MSB

Bit	Type	Function	Default
Bit 7	R	FE15	X
Bit 6	R	FE14	X
Bit 5	R	FE13	X
Bit 4	R	FE12	X
Bit 3	R	FE11	X
Bit 2	R	FE10	X
Bit 1	R	FE9	X
Bit 0	R	FE8	X

This register reports the upper eight bits of the FEBE accumulation counter.

FE0 - FE15:

Bits FE0 through FE15 represent the number of far end block errors that have been received since the last time the FEBE registers were polled by writing to SPTX Accumulation Trigger register. The write access transfers the internally accumulated error count to the FEBE registers within twelve PICLK cycles (or ~ 1 µs) and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Register 1CH, 5CH, 9CH: RPOP Tributary Multiframe Status and Control

Bit	Type	Function	Default
Bit 7	R	LOMI	X
Bit 6	R	LOMV	X
Bit 5	R/W	LOME	0
Bit 4		Unused	X
Bit 3	R	COMAI	X
Bit 2	R/W	COMAE	0
Bit 1		Unused	X
Bit 0		Unused	X

This register reports the status of the multiframe framer and enables interrupts due to framer events.

COMAE:

The change of multiframe alignment interrupt enable bit (COMAE) controls the generation of interrupts on when the SPTX dectect a change in the multiframe phase. When LOME is set high, an interrupt is generated upon change of multiframe alignment. When COMAE is set low, COMA has no effect on the interrupt output (INTB).

COMAI:

The change of multiframe alignment interrupt status bit (COMAI) is set high on changes in the multiframe alignment. This bit is cleared (and the interrupt acknowledged) when this register is read.

LOME:

The loss of multiframe interrupt enable bit (LOME) controls the generation of interrupts on declaration and removal of loss of multiframe indication (LOM). When LOME is set high, an interrupt is generated upon loss of multiframe. When LOME is set low, LOM has no effect on the interrupt output (INTB).

LOMV:

The loss of multiframe status bit (LOMV) reports the current state of the multiframe framer monitoring the receive stream. LOMV is set high when loss

of multiframe is declared and is set low when multiframe alignment has been acquired.

LOMI:

The loss of multiframe interrupt status bit (LOMI) is set high on changes in the loss of multiframe status. This bit is cleared (and the interrupt acknowledged) when this register is read.

Register 1DH, 5DH, 9DH: RPOP Tandem Connection and Ring Control

Bit	Type	Function	Default
Bit 7	R/W	SOS	0
Bit 6	R/W	ENSS	0
Bit 5	R/W	BLKBIP	0
Bit 4	R/W	DISFS	0
Bit 3		Unused	X
Bit 2	R/W	CDIFF	0
Bit 1	R/W	ISF	0
Bit 0	R/W	OTCTE	0

This register contains tandem connection and ring control bits.

OTCTE:

When set high, the OTCTE bit configures the RPOP to operates as a piece of originating TCTE (tandem connection terminating equipment). RPOP will place the receive BIP-8 error count from the previous frame on the IEC field and source the tandem path data link presented on the corresponding RTCOH input in the DL field of the tandem connection maintenance byte (Z5) on the DROP bus. The BIP-8 byte (B3) is updated to reflect the current and all previous modifications of the Z5 byte. When a loss of pointer or path AIS event is detected in the receive stream, RPOP will maintain the previous pointer on the H1, H2 bytes, and set the IEC field to indicate ISF (IEC = 'b1111). Correct B3 and Z5 bytes, and all ones on remaining synchronous payload envelope (virtual container) bytes will be placed on the DROP bus. When OTCTE is set high, the H4BYP bit in the RTAL Control register must be set high. When OTCTE is set low, RPOP is not an originating TCTE; payload data in receive stream is placed on the DROP bus unmodified.

ISF:

The ISF bit controls the insertion of incoming signal failure codes in the SPE bytes. When ISF is set high, the IEC field of the Z5 byte is set to indicated ISF ('b1111). The tandem connection data link remains active. An error-free path BIP is inserted in the B3 byte. All remaining SPE bytes are set to all-ones. When ISF is set low, data is processed normally. ISF is ignored when OTCTE is set low.

CDIFF:

The CDIFF bit controls the method of accumulating incoming error counts. When CDIFF is set low, the Tandem Connection IEC Count registers accumulate the counts reported in the IEC field of the Z5 byte directly. When CDIFF is set low, the Tandem Connection IEC Count registers accumulate the absolute value of the difference between the number of BIP errors detected in the current frame and the IEC count value.

DISFS:

When set high, the DISFS bit controls the BIP-8 calculations to ignore the fixed stuffed columns in an AU3 carrying a VC3. When DISFS is set low, BIP-8 calculations include the fixed stuff columns in an STS-1 stream. This bit is ignored when the SPTX is processing an STS-3c (STM-1/AU4) stream.

BLKBIP:

When set high, the block BIP-8 bit (BLKBIP) indicates that path BIP-8 errors are to be reported and accumulated on a block basis. A single BIP error is accumulated and reported to the return transmit path overhead processor if any of the BIP-8 results indicates a mismatch. When BLKBIP is set low, BIP-8 errors are accumulated and reported on a bit basis.

ENSS:

The enable size bit (ENSS) controls whether the SS bits in the payload pointer are used to determine offset changes in the pointer interpreter state machine. When a logic 1 is written to this bit, an incorrect SS bit pattern (i.e.,≠10).will prevent RPOP from issuing NDF_enable, inc_ind and dec_ind indications. When a logic 0 is written to this bit, the SS bits received do not affect active offset change events. Regardless of the logic state of the ENSS bit, an incorrect SS bit pattern will trigger an inv_point indication.

SOS:

The stuff opportunity spacing control bit (SOS) controls the spacing between consecutive pointer justification events on the receive stream. When a logic 1 is written to this bit, the definition of inc_ind and dec_ind indications includes the requirement that active offset changes have occurred a least three frame ago. When a logic 0 is written to this bit, pointer justification indications in the receive stream are followed without regard to the proximity of previous active offset changes.

Register 1EH, 5EH, 9EH: RPOP Tandem Connection IEC Count LSB

Bit	Type	Function	Default
Bit 7	R	IEC7	X
Bit 6	R	IEC6	X
Bit 5	R	IEC5	X
Bit 4	R	IEC4	X
Bit 3	R	IEC3	X
Bit 2	R	IEC2	X
Bit 1	R	IEC1	X
Bit 0	R	IEC0	X

This register reports the lower eight bits of the incoming error count counter.

Register 1FH, 5FH, 9FH: RPOP Tandem Connection IEC Count MSB

Bit	Type	Function	Default
Bit 7	R	IEC15	X
Bit 6	R	IEC14	X
Bit 5	R	IEC13	X
Bit 4	R	IEC12	X
Bit 3	R	IEC11	X
Bit 2	R	IEC10	X
Bit 1	R	IEC9	X
Bit 0	R	IEC8	X

This register reports the upper eight bits of the incoming error count counter.

IEC0 - IEC15:

Bits IEC0 through IEC15 represent the sum of the tandem connection incoming error counts that have been detected since the last time the tandem connection incoming error count registers were polled by writing to the SPTX Accumulation Trigger register. The write access transfers the internally accumulated error count to the tandem connection incoming error count registers within twelve PICLK cycles (or ~ 1 µs) and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Register 24H, 64H, A4H: PMON Receive Positive Pointer Justification Count

Bit	Type	Function	Default
Bit 7	R	RPJE[7]	X
Bit 6	R	RPJE[6]	X
Bit 5	R	RPJE[5]	X
Bit 4	R	RPJE[4]	X
Bit 3	R	RPJE[3]	X
Bit 2	R	RPJE[2]	X
Bit 1	R	RPJE[1]	X
Bit 0	R	RPJE[0]	X

This register reports the number of positive pointer justification events that occurred on the receive side in the previous accumulation interval. The counter is selectable to accumulate positive pointer justifications in the receive stream when the MONRS bit in the SPTX Master Configuration register is set high, and to accumulate justifications on the DROP bus when MONRS is set low.

RPJE0 - RPJE7:

Bits RPJE0 through RPJE7 represent the number of positive pointer justification events observed on the receive stream since the RPJE register was polled by writing to SPTX Accumulation Trigger register. The write access transfers the internally accumulated error count to the RPJE register within twelve PICLK cycles (or ~ 1 µs) and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Register 25H, 65H, A5H: PMON Receive Negative Pointer Justification Count

Bit	Type	Function	Default
Bit 7	R	RNJE[7]	X
Bit 6	R	RNJE[6]	X
Bit 5	R	RNJE[5]	X
Bit 4	R	RNJE[4]	X
Bit 3	R	RNJE[3]	X
Bit 2	R	RNJE[2]	X
Bit 1	R	RNJE[1]	X
Bit 0	R	RNJE[0]	X

This register reports the number of negative pointer justification events that occurred on the receive side in the previous accumulation interval. The counter is selectable to accumulate negative pointer justifications in the receive stream when the MONRS bit in the SPTX Master Configuration register is set high, and to accumulate justifications on the DROP bus when MONRS is set low.

RNJE0 - RNJE7:

Bits RNJE0 through RNJE7 represent the number of negative pointer justification events observed on the receive side since the RNJE register was polled by writing to SPTX Accumulation Trigger register. The write access transfers the internally accumulated error count to the RNJE register within twelve PICLK cycles (or ~ 1 µs) and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Register 26H, 66H, A6H: PMON Transmit Positive Pointer Justification Count

Bit	Type	Function	Default
Bit 7	R	TPJE [7]	X
Bit 6	R	TPJE [6]	X
Bit 5	R	TPJE [5]	X
Bit 4	R	TPJE [4]	X
Bit 3	R	TPJE [3]	X
Bit 2	R	TPJE [2]	X
Bit 1	R	TPJE [1]	X
Bit 0	R	TPJE [0]	X

This register reports the number on positive pointer justification events that occurred on the transmit stream in the previous accumulation interval.

TPJE 0 - TPJE 7:

Bits TPJE 0 through TPJE 7 represent the number of positive pointer justification events inserted in the transmit stream since the TPJE register was polled by writing to SPTX Accumulation Trigger register. The write access transfers the internally accumulated error count to the TPJE register within twelve PICLK cycles (or ~ 1 µs) and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Register 27H, 67H, A7H: PMON Transmit Negative Pointer Justification Count

Bit	Type	Function	Default
Bit 7	R	TNJE [7]	X
Bit 6	R	TNJE [6]	X
Bit 5	R	TNJE [5]	X
Bit 4	R	TNJE [4]	X
Bit 3	R	TNJE [3]	X
Bit 2	R	TNJE [2]	X
Bit 1	R	TNJE [1]	X
Bit 0	R	TNJE [0]	X

This register reports the number of negative pointer justification events that occurred on the transmit stream in the previous accumulation interval.

TNJE 0 - TNJE 7:

Bits TNJE 0 through TNJE 7 represent the number of negative pointer justification events inserted in the transmit stream since the TNJE register was polled by writing to SPTX Accumulation Trigger register. The write access transfers the internally accumulated error count to the TNJE register within twelve PICLK cycles (or ~ 1 µs) and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Register 28H, 68H, A8H: RTAL Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	H4BYP	0
Bit 5	R/W	CLRFS	0
Bit 4	R/W	SSS	1
Bit 3	R/W	ISFE	0
Bit 2	R/W	ESEE	0
Bit 1	R/W	DPJEE	0
Bit 0	R/W	IPAIS	0

This register allows the operation of the Receive Telecombus Aligner to be configured.

IPAIS:

The insert path alarm indication signal (IPAIS) bit controls the insertion of PAIS in the DROP bus. When IPAIS is set high, path AIS is inserted in the DROP bus. The pointer bytes (H1, H2 and H3) and the entire SPE (VC) are set to all-ones. Path FERF indication is reported in the receive alarm port and to the companion TPOP in the SPTX. Normal operation resumes when the IPAIS bit is set low.

DPJEE:

The DROP bus pointer justification event interrupt enable bit (DPJEE) controls the activation of the interrupt output when a pointer justification is inserted in the DROP bus. When DPJEE is set high, insertion of pointer justification events in the DROP bus will activate the interrupt (INTB) output. When DPJEE is set low, insertion of pointer justification events in the DROP bus will not affect INTB.

ESEE:

The elastic store error interrupt enable bit (ESEE) controls the activation of the interrupt output when a FIFO underflow or overflow has been detected in the elastic store . When ESEE is set high, FIFO flow error events affect the interrupt (INTB) output. When ESEE is set low, FIFO flow error events will not affect INTB.

ISFE:

The incoming signal failure interrupt enable bit (ISFE) controls the activation of the interrupt output when the status of the ISF code in the tandem connection maintenance byte changes to indicate failure or to indicate normal operation.

SSS:

The set ss bit (SSS) controls the value of the ss field in the H1 pointer byte in the DROP bus. When SSS is set high, the ss bits are set to 'b10. When SSS is set low, the ss bits are set to 'b00.

CLRFS:

The clear fixed stuff column bit (CLRFS) enables the setting of the fixed stuff columns to zero. When a logic 1 is written to CLRFS, the fixed stuff column data are set to 00H. When a logic 0 is written to CLRFS, the fixed stuff column data from the receive stream is placed on the DROP bus unchanged. The location of the fixed stuff columns in the synchronous payload envelope (virtual container) is dependent on the whether the SPTX is processing concatenated payload.

H4BYP:

The tributary multiframe bypass bit (H4BYP) controls whether the RTAL block overwrites the H4 byte in the path overhead with an internally generated sequence. When H4BYP is set high, the H4 byte carried in the receive stream is placed on the DROP bus unchanged. When H4BYP is set low, the H4 byte is replaced by the sequence 'hFC, 'hFD, 'hFE and 'hFF. The phase of the four frames in the multiframe is synchronized by the multiframe framer in the RPOP block. In originating tandem connection terminating equipment mode (OTCTE set high in RPOP Tandem Connection and Ring Control register), H4BYP must be set high for proper operation of the SPTX.

Reserved:

The Reserved bit must be set low for correct operation of the SPTX.

Register 29H, 69H, A9H: RTAL Interrupt Status and Diagnostic

Bit	Type	Function	Default
Bit 7	R/W	DOPJ[1]	0
Bit 6	R/W	DOPJ[0]	0
Bit 5	R/W	ESD[1]	1
Bit 4	R/W	ESD[0]	0
Bit 3	R	ESEI	X
Bit 2	R	PPJI	X
Bit 1	R	NPJI	X
Bit 0	R/W	DLOP	0

This register allows the control of the DROP bus interface and sensing of interrupt status.

DLOP:

The diagnose loss of pointer control bit (DLOP) allows downstream pointer processing elements to be diagnosed. When DLOP is set high, the new data flag (NDF) field of the payload pointer inserted in the DROP bus is inverted causing downstream pointer processing elements to enter a loss of pointer (LOP) state.

NPJI:

The DROP bus negative pointer justification interrupt status bit (NPJI) is set high when the RTAL inserts a positive pointer justification event on the DROP bus.

PPJI:

The DROP bus positive pointer justification interrupt status bit (PPJI) is set high when the RTAL inserts a positive pointer justification event on the DROP bus.

ESEI:

The DROP bus elastic store error interrupt status bit (ESEI) is set high when the FIFO in RTAL underflows or overflows.

ESD0- ESD1:

The elastic store depth control bits (ESD[1:0]) set elastic store FIFO fill thresholds. I.e., the thresholds for the ES_upperT and ES_lowerT indications. The thresholds for the four ESD[1:0] codes are:

Table 4 - Receive Elastic Store Depth Control

ESD[1:0]	Hard neg limit	Soft neg limit	Soft pos limit	Hard pos limit
00	4	0	0	4
01	5	1	1	4
10	6	4	4	6
11	7	6	6	7

Definitions:

Soft neg limit: The maximum number of incoming negative justification (after several incoming positive justifications) before entering the soft region of the FIFO (In the soft region, the RTAL generates outgoing negative justifications at the rate of 1 in every 16 frames).

Hard neg limit : The maximum number of incoming negative justification (after several incoming positive justifications) before entering the hard region of the FIFO (In the hard region, the RTAL generates outgoing negative justification at the rate of 1 in every 4 frames).

Soft pos limit: The maximum number of incoming positive justification (after several incoming negative justifications) before entering the soft region of the FIFO (In the soft region, the RTAL generates outgoing positive justification at the rate of 1 in every 16 frames).

Hard pos limit: The maximum number of incoming positive justification (after several incoming negative justifications) before entering the hard region of the FIFO (In the hard region the RTAL will start generates outgoing positive justification at the rate of 1 in every 4 frames).

DOPJ0- DOPJ1:

The diagnose pointer justification bits (DOPJ[1:0]) allow downstream pointer processing elements to be diagnosed for correct reaction to pointer justification events. Setting DOPJ[1] high and DOPJ[0] low, forces the RTAL to generate positive stuff justification events on the DROP bus at the rate of one every four frames regardless of the current depth of the internal FIFO. Prolonged application may cause the FIFO to overflow. Setting DOPJ[1] low and DOPJ[0] high, forces the RTAL to generate negative stuff justification events at the rate of one every four frames, regardless of the current depth of the internal FIFO. Prolonged application may cause the FIFO to underflow. Setting both DOPJ[1] and DOPJ[0] high disables the RTAL from generating pointer justification events. If the incoming and outgoing clocks have a frequency offset, the internal FIFO may under/overflow depending on the relative frequencies of the clocks. Pointer justification events are generated based on the current depth of the internal FIFO when DOPJ[1] and DOPJ[0] are both set low. When DOPJ[1:0] is set to values other than 'b00, the detection of elastic store over/underflow is disabled.

The interrupt bits (and the interrupt) are cleared when this register is read.

Register 2AH, 6AH, AAH: RTAL Alarm and Diagnostic Control

Bit	Type	Function	Default
Bit 7	R	ISFV	X
Bit 6	R	ISFI	X
Bit 5	R/W	H4AISB	0
Bit 4	R/W	ITUAIS	0
Bit 3	R/W	FISF	0
Bit 2	R/W	TTCTE	0
Bit 1	R/W	ESAIS	0
Bit 0	R/W	DH4	0

This register reports alarms and controls diagnostics on the DROP bus.

DH4:

The diagnose multiframe indicator enable bit (DH4) controls the inversion of the multiframe indicator (H4) byte in the DROP bus. This bit may be used to cause an out of multiframe alarm in downstream circuitry when the SPE (VC) is used to carry virtual tributary (VT) or tributary unit (TU) based payloads. When a logic 0 is written to this bit position, the H4 byte is unmodified. When a logic 1 is written to this bit position, the H4 byte is inverted.

ESAIS:

The elastic store error path AIS insertion enable bit (ESAIS) controls the insertion of path AIS in the DROP bus when a FIFO underflow or overflow has been detected in the elastic store . When ESAIS is set high, detection of FIFO flow error will cause path AIS to be inserted in the DROP bus for three frames. When ESAIS is set low, path AIS is not inserted as a result of FIFO errors.

TTCTE:

The TTCTE bit controls whether the RTAL is terminating a tandem connection. When TTCTE is set high, Incoming Signal Failure codes (ISF) in the Incoming Error Count field (IEC) of the tandem connection maintenance byte (Z5) is translated into path AIS in the DROP bus. Z5 bytes carrying a normal IEC value are cleared to zero, and the B3 byte is update to reflect the

change to Z5. When TTCTE is set low, the RTAL is not terminating a tandem connection. The B3 and Z5 bytes are not modified by the RTAL.

FISF:

The FISF bit controls the filtering of ISF codes in the receive stream in terminating tandem connection terminating equipment mode (TTCTE high). When FISF is set high, the ISF state is entered after receiving an active ISF code ('b1111) for three consecutive frames. Similarly, path AIS is removed after detection of inactive ISF codes for three consecutive frames. When FISF is set low, the ISF state is asserted immediately on detection of active ISF and removal occurs immediately on detection of inactive ISF.

ITUAIS:

The insert tributary path AIS bits controls the insertion of Tributary Path AIS in the DROP bus. When ITUAIS is set high, columns in the DROP bus carrying tributary traffic are set to all ones. The pointer bytes (H1, H2, and H3), the path overhead column, and the fixed stuff columns are unaffected. Normal operation resumes when the ITUAIS bit is set low.

H4AISB:

The insert H4 AIS bits controls the insertion of the all-ones AIS pattern in the H4 byte. When H4AISB is set low, the H4 byte will be over-written with 'hFF when path AIS is inserted in the DROP bus. When H4AISB is set high, the H4 byte is not over-written during path AIS insertion.

ISFI:

The incoming signal failure alarm interrupt status bit (ISFI) is set high when the RTAL detects a change in the ISF state (from normal to signal failure, or vice versa). This bit is cleared when this register is read.

ISFV:

The incoming signal failure alarm status bit (ISFV) reports the status of the ISF state derived from the ISF code in the tandem connection maintenance byte (Z5) of the receive stream.

Register 30H, 70H, B0H: TPOP Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	EXCFS	0
Bit 2	R/W	DH4	0
Bit 1	R/W	DB3	0
Bit 0	R/W	PAIS	0

The register controls the operation of the transport overhead processor for downstream diagnostics and tandem connection applications.

PAIS:

The PAIS bit controls the insertion of path alarm indication signal in the transmit stream. This register bit is logically ORed with the corresponding TPAIS[3:1] input. When a logic one is written to this bit, the synchronous payload envelope and the pointer bytes (H1 - H3) are set to all-ones. When a logic zero is written to this bit, the SPE and pointer bytes are processed normally. Upon de-activation of path AIS, a new data flag accompanies the first valid pointer.

DB3:

The diagnose BIP-8 enable bit (DB3) controls the inversion of the path BIP-8 byte (B3) in the transmit stream. When a logic zero is written to this bit position, the B3 byte is transmitted uncorrupted. When a logic one is written to this bit position, the B3 byte is inverted, causing the insertion of eight path BIP-8 errors per frame. This bit overrides the state of the B3 error insertion mask controlled by the corresponding TPOHEN primary input.

DH4:

The diagnose multiframe indicator enable bit (DH4) controls the inversion of the multiframe indicator (H4) byte in the transmit stream. This bit may be used to cause an out of multiframe alarm in downstream circuitry when the SPE (VC) is used to carry virtual tributary (VT) or tributary unit (TU) based

payloads. When a logic 0 is written to this bit position, the H4 byte is unmodified. When a logic 1 is written to this bit position, the H4 byte is inverted.

EXCFS:

The fixed stuff column BIP-8 exclusion bit (EXCFS) controls the inclusion of bytes in the fixed stuff columns of the STS-1 payload carrying tributaries in path BIP-8 calculations. When EXCFS is set high, the value of bytes in the fixed stuff columns do not affect the path BIP-8 byte (B3). When EXCFS is set low, data in the fixed stuff bytes are included in path BIP-8 calculations. This bit has no effect when the SPTX is processing an STS-3c (STM-1) stream.

Register 31H, 71H, B1H: TPOP GENERATED Bus Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	FTPTR	0
Bit 5	R/W	SOS	0
Bit 4	R/W	PLD	0
Bit 3	R/W	NDF	0
Bit 2	R/W	NSE	0
Bit 1	R/W	PSE	0
Bit 0	R/W	Reserved1	0

This registers controls the active offset on the GENERATED bus.

Reserved1:

The Reserved1 bit must be written to logic 0 for proper operation of the SPTX.

PSE:

The positive stuff enable bit (PSE) controls the generation of positive pointer movements in the GENERATED bus. A zero to one transition on this bit enables the insertion of a single positive pointer justification in the GENERATED bus. This register bit is automatically cleared after the pointer movement is inserted. If the NSE and PSE register bits are both asserted, no pointer movement is generated, but the PSE and NSE bits are cleared anyway.

NSE:

The negative stuff enable bit (NSE) controls the generation of negative pointer movements in the GENERATED bus. A zero to one transition on this bit enables the insertion of a single positive pointer justification in the GENERATED bus. This register bit is automatically cleared after the pointer movement is inserted. If the NSE and PSE register bits are both asserted, no pointer movement is generated, but the PSE and NSE bits are cleared anyway.

NDF:

The NDF insert bit (NDF) controls the insertion of new data flags in the payload pointer. When a logic one is written to this bit, the pattern contained in the NDF[3:0] bits in the Arbitrary Pointer MSB register is inserted continuously in the payload pointer of the transmit stream. When a logic zero is written to this bit, the normal pattern ('b0110) is inserted in the payload pointer..

PLD:

The payload pointer load enable bit (PLD) controls the loading of the pointer value contained in the Payload Pointer registers. If a legal value (i.e.,0 ≤ pointer value ≤ 782) is found in the TPOP Payload Pointer registers, writing a one to this bit causes the J1 indication pulse on GC1J1V1 pulse to immediately jump to the corresponding byte position. If a value greater than 782 is found in the Payload Pointer registers, GC1J1V1 pulses will retain the previous alignment. This bit is automatically cleared after the new payload pointer has been loaded. The J1 indicator will not track changes in GFP. To maintain a constant J1 offset with respect to GFP, PLD must be reasserted each time the GFP changes position.

SOS:

The stuff opportunity spacing control bit (SOS) bit controls the spacing between consecutive SPE positive or negative stuff events on the GENERATED bus. When a logic 0 is written to this bit, stuff events may be generated every frame as controlled by the PSE, and NSE register bits. When a logic 1 is written to this bit, no positive or negative stuffs occur within three frames of the latest pointer movement (including an arbitrary movement). An arbitrary pointer movement can still occur in any frame.

FTPTR:

The force transmit pointer bit (FTPTR) enables the insertion of the pointer value contained in the Arbitrary Pointer Registers into the TD[7:0] stream for diagnostic purposes. This allows upstream payload mapping circuitry to continue functioning normally and a valid SPE to continue to be generated. If FTPTR is set to logic 1, the APTR[9:0] bits of the Arbitrary Pointer Registers are inserted into the H1 and H2 bytes of the TD[7:0] stream. When FTPTR is set and immediately reset at least one Arbitrary Pointer substitution is guaranteed to be sent . If FTPTR is a logic 0, a valid pointer is inserted.

Register 32H, 72H, B2H: TPOP Source Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	SRCZ5	0
Bit 5	R/W	SRCZ4	0
Bit 4	R/W	SRCZ3	0
Bit 3	R/W	SRCC2	0
Bit 2	R/W	SRCG1	0
Bit 1	R/W	SRCF2	0
Bit 0	R/W	SRCJ1	0

This register controls the source of path overhead bytes in the transmit stream.

SRCJ1:

The SRCJ1 bit select the source of the path trace message byte (J1) in the transmit stream. When the corresponding TPTBnEN bit in the Master Transmit Control register is set high, SRCJ1 is ignored and the path trace message is sourced from the SPTB block. When the corresponding TPTBnEN bit is set low, SRCJ1 is logically ORed with corresponding TPOHEN input to select the source for the J1 byte. When a logic 1 is written to SRCJ1, the J1 byte is inserted from the data sampled on corresponding TPOH input during the J1 byte position. When a logic 0 is written to SRCJ1, the J1 byte source is determined by the corresponding TPOHEN input.

SRCF2, SRCG1, SRCC2, SRCZ3, SRCZ4, SRCZ5:

The SRCxx bits are logically ORed with corresponding TPOHEN input to select the source for the path overhead bytes in the transmit stream. For example, when a logic 1 is written to SRCF2, the F2 byte is inserted from the data sampled on corresponding TPOH input during the F2 byte position. When a logic 0 is written to SRCF2, the F2 byte source is determined by the corresponding TPOHEN input.

Register 33H, 73H, B3H: TPOP Current Pointer LSB

Bit	Type	Function	Default
Bit 7	R	CPTR[7]	X
Bit 6	R	CPTR[6]	X
Bit 5	R	CPTR[5]	X
Bit 4	R	CPTR[4]	X
Bit 3	R	CPTR[3]	X
Bit 2	R	CPTR[2]	X
Bit 1	R	CPTR[1]	X
Bit 0	R	CPTR[0]	X

This register reports the less significant byte of the active offset on the transmit stream.

Register 34H, 74H, B4H: TPOP Current Pointer MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	CPTR[9]	X
Bit 0	R	CPTR[8]	X

This register reports the most significant two bits of the active offset on the transmit stream.

CPTR0-CPTR9:

The CPTR[9:0] bits reflect the value of the active offset on the transmit stream as indicated by pulses on the AC1J1V1 signal. It is recommended the CPTR[9:0] value be software debounced to ensure a correct value is received.

Register 35H, 75H, B5H: TPOP Payload Pointer LSB

Bit	Type	Function	Default
Bit 7	R/W	APTR[7]	0
Bit 6	R/W	APTR[6]	0
Bit 5	R/W	APTR[5]	0
Bit 4	R/W	APTR[4]	0
Bit 3	R/W	APTR[3]	0
Bit 2	R/W	APTR[2]	0
Bit 1	R/W	APTR[1]	0
Bit 0	R/W	APTR[0]	0

This register contains the less significant byte of the active offset placed on the GENERATED bus.

Register 36H, 76H, B6H: TPOP Payload Pointer MSB

Bit	Type	Function	Default
Bit 7	R/W	NDF[3]	1
Bit 6	R/W	NDF[2]	0
Bit 5	R/W	NDF[1]	0
Bit 4	R/W	NDF[0]	1
Bit 3	R/W	S[1]	1
Bit 2	R/W	S[0]	0
Bit 1	R/W	APTR[9]	0
Bit 0	R/W	APTR[8]	0

This register contains the most significant two bits of the active offset placed on the GENERATED bus.

APTR0-APTR9:

The APTR[9:0] bits are used to set an arbitrary active offset value on the GENERATED bus. The arbitrary pointer value is transferred by writing a logic one to the PLD bit in the TPOP Pointer Control Register. A legal value (i.e. $0 \leq$ pointer value ≤ 782) results in the J1 pulse on the GC1J1V1 signal shifting to the corresponding byte position. A value of greater than 782 has no effect.

S1-S0:

The payload pointer size bits (S[1:0]) are inserted in the S[1:0] bit postions in the payload pointer in the transmit stream.

NDF3-NDF0:

The new data flag bits (NDF[3:0]) are inserted in the NDF bit positions when the TPOP makes a discontinuous change in active offset or when the NDF bit in the TPOP Payload Pointer Control register is set to logic one.

Register 37H, 77H, B7H: TPOP Path Trace

Bit	Type	Function	Default
Bit 7	R/W	J1[7]	0
Bit 6	R/W	J1[6]	0
Bit 5	R/W	J1[5]	0
Bit 4	R/W	J1[4]	0
Bit 3	R/W	J1[3]	0
Bit 2	R/W	J1[2]	0
Bit 1	R/W	J1[1]	0
Bit 0	R/W	J1[0]	0

This register contains the value to be inserted in the path trace byte (J1) of the transmit stream when the Transmit Path Trace Buffer block is disabled (TPTBxEN set low).

J10-J17:

The J1[7:0] bits are inserted in the J1 byte position in the transmit stream when the associated TPTB block is disabled, the SRCJ1 bit of the Source Control Register is logic 0 and corresponding TPOHEN input is low during the path trace bit positions in the path overhead input stream, TPOH.

Register 38H, 78H, B8H: TPOP Path Signal Label

Bit	Type	Function	Default
Bit 7	R/W	C2[7]	0
Bit 6	R/W	C2[6]	0
Bit 5	R/W	C2[5]	0
Bit 4	R/W	C2[4]	0
Bit 3	R/W	C2[3]	0
Bit 2	R/W	C2[2]	0
Bit 1	R/W	C2[1]	0
Bit 0	R/W	C2[0]	1

This register contains the value to be inserted in the path signal label byte (C2) of the transmit stream.

C20-C27:

The C2[7:0] bits are inserted in the C2 byte position in the transmit stream when the SRCC2 bit of the Source Control Register is logic 0 and corresponding TPOHEN input is low during the path signal label bit positions in the path overhead input stream, TPOH. Upon reset, the register value defaults to 01H, which represents "Equipped - Non Specific Payload."

Register 39H, 79H, B9H: TPOP Path Status

Bit	Type	Function	Default
Bit 7	R/W	FEBE[3]	0
Bit 6	R/W	FEBE[2]	0
Bit 5	R/W	FEBE[1]	0
Bit 4	R/W	FEBE[0]	0
Bit 3	R/W	PFERF	0
Bit 2	R/W	G1[2]	0
Bit 1	R/W	G1[1]	0
Bit 0	R/W	G1[0]	0

This register reflects the value inserted in the path status byte (G1) of the transmit stream.

FEBE0-FEBE3:

The far end block error count (FEBE[3:0]) is inserted in the FEBE bit positions in the path status byte when the SRCG1 bit of the Source Control Register is logic 0 and the corresponding TPOHEN input is low during the path status FEBE bit positions in the corresponding path overhead input stream, TPOH. The value contained in FEBE[3:0] is cleared after being inserted in the path status byte. Any non-zero FEBE[3:0] value overwrites the value that would normally have been inserted based on the number of FEBEs accumulated from the BIP-8 errors detected by the companion RPOP in the SPTX during the last frame. When reading this register, a non-zero value in these bit positions indicates that the insertion of this value is still pending.

PFERF:

The path FERF indication bit (PFERF) controls the insertion of the STS path FERF alarm. This register bit value is logically ORed with the alarm indications from the associated RPOP in the SPTX or the transmit alarm port. When a logic 1 is written to this bit position, the PFERF bit position in the path status byte is set high. When a logic 0 is written to this bit position, the PFERF bit position in the path status byte is set low. This bit has no effect if the SRCG1 bit of the Source Control Register is logic 1 or the corresponding TPOHEN is high during the path status PFERF bit position in the corresponding path overhead input stream, TPOH, in which case the value is taken from TPOH.

G10-G12:

The G1[2:0] bits are inserted in the unused bit positions in the path status byte when the SRCG1 bit of the Source Control Register is logic 0 and the corresponding TPOHEN input is low during the unused bit positions in the corresponding path overhead input stream, TPOH.

Register 3AH, 7AH, BAH: TPOP Path User Channel

Bit	Type	Function	Default
Bit 7	R/W	F2[7]	0
Bit 6	R/W	F2[6]	0
Bit 5	R/W	F2[5]	0
Bit 4	R/W	F2[4]	0
Bit 3	R/W	F2[3]	0
Bit 2	R/W	F2[2]	0
Bit 1	R/W	F2[1]	0
Bit 0	R/W	F2[0]	0

This register contains the value to be inserted in the path user channel byte (F2) of the transmit stream.

F20-F27:

The F2[7:0] bits are inserted in the F2 byte position in the transmit stream when the SRCF2 bit of the Source Control Register is logic 0 and the corresponding TPOHEN input is low during the path user channel bit positions in the corresponding path overhead input stream, TPOH.

Register 3BH, 7BH, BBH: TPOP Path Growth #1

Bit	Type	Function	Default
Bit 7	R/W	Z3[7]	0
Bit 6	R/W	Z3[6]	0
Bit 5	R/W	Z3[5]	0
Bit 4	R/W	Z3[4]	0
Bit 3	R/W	Z3[3]	0
Bit 2	R/W	Z3[2]	0
Bit 1	R/W	Z3[1]	0
Bit 0	R/W	Z3[0]	0

This register contains the value to be inserted in the path growth byte #1 (Z3) of the transmit stream.

Z30-Z37:

The Z3[7:0] bits are inserted in the Z3 byte position in the transmit stream when the SRCZ3 bit of the Source Control Register is logic 0 and corresponding TPOHINS input is low during the path growth #1 bit positions in the corresponding path overhead input stream, TPOH.

Register 3CH, 7CH, BCH: TPOP Path Growth #2

Bit	Type	Function	Default
Bit 7	R/W	Z4[7]	0
Bit 6	R/W	Z4[6]	0
Bit 5	R/W	Z4[5]	0
Bit 4	R/W	Z4[4]	0
Bit 3	R/W	Z4[3]	0
Bit 2	R/W	Z4[2]	0
Bit 1	R/W	Z4[1]	0
Bit 0	R/W	Z4[0]	0

This register contains the value to be inserted in the path growth byte #2 (Z4) of the transmit stream.

Z40-Z47:

The Z4[7:0] bits are inserted in the Z4 byte position in the transmit stream when the SRCZ3 bit of the Source Control Register is logic 0 and corresponding TPOHINS input is low during the path growth #2 bit positions in the corresponding path overhead input stream, TPOH.

Register 3DH, 7DH, BDH: TPOP Tandem Connection Maintenance

Bit	Type	Function	Default
Bit 7	R/W	Z5[7]	0
Bit 6	R/W	Z5[6]	0
Bit 5	R/W	Z5[5]	0
Bit 4	R/W	Z5[4]	0
Bit 3	R/W	Z5[3]	0
Bit 2	R/W	Z5[2]	0
Bit 1	R/W	Z5[1]	0
Bit 0	R/W	Z5[0]	0

This register contains the value to be inserted in the tandem connection maintenance byte (Z5) of the transmit stream.

Z50-Z57:

The Z5[7:0] bits are inserted in the Z5 byte position in the transmit stream when the SRCZ5 bit of the Source Control Register is logic 0 and the corresponding TPOHEN input is low during the tandem connection maintenance byte positions in the corresponding path overhead input stream, TPOH.

Register 3EH: TPOP Concatenation LSB

Bit	Type	Function	Default
Bit 7	R/W	CONCAT[7]	1
Bit 6	R/W	CONCAT[6]	1
Bit 5	R/W	CONCAT[5]	1
Bit 4	R/W	CONCAT[4]	1
Bit 3	R/W	CONCAT[3]	1
Bit 2	R/W	CONCAT[2]	1
Bit 1	R/W	CONCAT[1]	1
Bit 0	R/W	CONCAT[0]	1

Register 3FH: TPOP Concatenation MSB

Bit	Type	Function	Default
Bit 7	R/W	CONCAT[15]	1
Bit 6	R/W	CONCAT[14]	0
Bit 5	R/W	CONCAT[13]	0
Bit 4	R/W	CONCAT[12]	1
Bit 3	R/W	CONCAT[11]	0
Bit 2	R/W	CONCAT[10]	0
Bit 1	R/W	CONCAT[9]	1
Bit 0	R/W	CONCAT[8]	1

The Concatenation LSB and MSB Registers controls the value inserted in the concatenation indicators in the transmit stream.

CONCAT[15:0]:

The CONCAT[15:0] bits control the value inserted in the second and third H1 and H2 byte positions when transmitting an STS-3c or STM-1 stream. The value written to CONCAT[15:8] is inserted in the H1 byte position of STS-1 #2 and STS-1 #3 in the concatenated transmit stream. The value written to CONCAT[7:0] is inserted in the H2 byte position of STS-1 #2 and STS-1 #3 in the concatenated transmit stream. The default values represent the normal concatenation indication (all ones in the pointer bits, zeros in the unused bits, and NDF enabled indication). CONCAT[15:0] is not used when transmitting an STS-1 or an STS-3 stream.

Register 40H, 80H, C0H: TTAL Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved3	0
Bit 6	R/W	H4BYP	0
Bit 5	R/W	CLRFS	0
Bit 4	R/W	Reserved2	1
Bit 3	R/W	ISFE	0
Bit 2	R/W	ESEE	0
Bit 1	R/W	PJEE	0
Bit 0	R/W	Reserved1	0

This register allows the operation of the Transmit Telecombus Aligner to be configured.

Reserved1:

The reserved1 bit must be set low for correct operation of the SPTX.

PJEE:

The pointer justification event interrupt enable bit (PJEE) controls the activation of the interrupt output when a pointer justification is inserted in the transmit stream. When PJEE is set high, insertion of pointer justification events in the transmit stream will activate the interrupt (INTB) output. When PJEE is set low, insertion of pointer justification events in the transmit stream will not affect INTB.

ESEE:

The elastic store error interrupt enable bit (ESEE) controls the activation of the interrupt output when a FIFO underflow or overflow has been detected in the elastic store . When ESEE is set high, FIFO flow error events the interrupt (INTB) output. When ESEE is set low, FIFO flow error events will not affect INTB.

ISFE:

The incoming signal failure interrupt enable bit (ISFE) controls the activation of the interrupt output when the ISF state in the tandem connection maintenance byte changes to indicate failure or to indicate normal operation.

Reserved2:

The reserved2 bit must be set high for correct operation of the SPTX.

CLRFS:

The clear fixed stuff column bit (CLRFS) enables the setting of the fixed stuff columns to zero. When a logic 1 is written to CLRFS, the fixed stuff column data are set to 00H. When a logic 0 is written to CLRFS, the fixed stuff column data from the ADD bus is placed on the transmit stream unchanged. The location of the fixed stuff columns in the synchronous payload envelope (virtual container) is dependent on the whether the SPTX is processing concatenated payload.

H4BYP:

The tributary multiframe bypass bit (H4BYP) controls whether the TTAL block overwrites the H4 byte in the path overhead with an internally generated sequence. When H4BYP is set high, the H4 byte carried in the ADD bus is placed in the transmit stream unchanged. When H4BYP is set low, the H4 byte is replaced by the sequence 'hFC, 'hFD, 'hFE and 'hFF. The phase of the four frames in the multiframe is synchronized by the V1 pulse in AC1J1V1 input.

Reserved3:

The Reserved3 bit must be set low for correct operation of the SPTX.

Register 41H, 81H, C1H: TTAL Interrupt Status and Diagnostic

Bit	Type	Function	Default
Bit 7	R/W	DOPJ[1]	0
Bit 6	R/W	DOPJ[0]	0
Bit 5	R/W	ESD[1]	1
Bit 4	R/W	ESD[0]	0
Bit 3	R	ESEI	X
Bit 2	R	PPJI	X
Bit 1	R	NPJI	X
Bit 0	R/W	Reserved	0

This register allows the control of the transmit stream and sensing of interrupt status.

Reserved:

The Reserved bit must be set low for correct operation of the SPTX.

NPJI:

The transmit stream negative pointer justification interrupt status bit (NPJI) is set high when the TTAL inserts a positive pointer justification event in the transmit stream.

PPJI:

The transmit stream positive pointer justification interrupt status bit (PPJI) is set high when the TTAL inserts a positive pointer justification event in the transmit stream.

ESEI:

The DROP bus elastic store error interrupt status bit (ESEI) is set high when the FIFO in TTAL underflows or overflows.

ESD0- ESD1:

The elastic store depth control bits (ESD[1:0]) set elastic store FIFO fill thresholds. I.e., the thresholds for the ES_upperT and ES_lowerT indications. The thresholds for the four ESD[1:0] codes are:

Table 5 - Transmit Elastic Store Depth Control

ESD[1:0]	Hard neg limit	Soft neg limit	Soft pos limit	Hard pos limit
00	4	0	0	4
01	5	1	1	4
10	6	4	4	6
11	7	6	6	7

Definitions:

Soft neg limit: The maximum number of incoming negative justification (after several incoming positive justifications) before entering the soft region of the FIFO (In the soft region, the TTAL generates outgoing negative justification at the rate of 1 in every 16 frames).

Hard neg limit: The maximum number of incoming negative justification (after several incoming positive justifications) before entering the hard region of the FIFO (In the hard region, the TTAL generates outgoing negative justification at the rate of 1 in every 4 frames).

Soft pos limit: The maximum number of incoming positive justification (after several incoming negative justifications) before entering the soft region of the FIFO (In the soft region, the TTAL generates outgoing positive justification at the rate of 1 in every 16 frames).

Hard pos limit: The maximum number of incoming positive justification (after several incoming negative justifications) before entering the hard region of the FIFO (In the hard region the TTAL will start generates outgoing positive justification at the rate of in 1 every 4 frames).

DOPJ0- DOPJ1:

The diagnose pointer justification bits (DOPJ[1:0]) allow downstream pointer processing elements to be diagnosed for correct reaction to pointer justification events. Setting DOPJ[1] high and DOPJ[0] low, forces the TTAL to generate positive stuff justification events in the transmit stream at the rate of one every four frames regardless of the current depth of the internal FIFO. Prolonged application may cause the FIFO to overflow. Setting DOPJ[1] low

and DOPJ[0] high, forces the TTAL to generate negative stuff justification events at the rate of one every four frames, regardless of the current depth of the internal FIFO. Prolonged application may cause the FIFO to underflow. Setting both DOPJ[1] and DOPJ[0] high disables the TTAL from generating pointer justification events. If the incoming and outgoing clocks have a frequency offset, the internal FIFO may under/overflow depending on the relative frequencies of the clocks. Pointer justification events are generated based on the current depth of the internal FIFO when DOPJ[1] and DOPJ[0] are both set low. When DOPJ[1:0] is set to values other than 'b00, the detection of elastic store over/underflow is disabled.

The interrupt bits (and the interrupt) are cleared when this register is read.

Register 42H, 82H, C2H: TTAL Alarm and Diagnostic Control

Bit	Type	Function	Default
Bit 7	R	ISFV	X
Bit 6	R	ISFI	X
Bit 5	R/W	Reserved2	0
Bit 4	R/W	ITUAIS	0
Bit 3	R/W	FISF	0
Bit 2	R/W	TTCTE	0
Bit 1	R/W	ESAIS	0
Bit 0	R/W	Reserved1	0

This register controls the tributary format on the transmit stream.

Reserved1:

The Reserved1 bit must be set to logic 0 for correct operation of the SPTX.

ESAIS:

The elastic store error path AIS insertion enable bit (ESAIS) controls the insertion of path AIS in the transmit stream when a FIFO underflow or overflow has been detected in the elastic store . When ESAIS is set high, detection of FIFO flow error will cause path AIS to be inserted in the transmit stream for three frames. When ESAIS is set low, path AIS is not inserted as a result of FIFO errors.

TTCTE:

The TTCTE bit controls whether the TTAL is terminating a tandem connection. When TTCTE is set high, Incoming Signal Failure codes (ISF) in the Incoming Error Count field (IEC) of the tandem connection maintenance byte (Z5) is translated into path AIS in the transmit stream. For normal IEC values, the Z5 byte is cleared to zero and the B3 byte is updated to reflect the change to Z5. When TTCTE is set high, the TTAL is not terminating a tandem connection. The Z5 and B3 bytes are not modified by the TTAL.

FISF:

The FISF bit controls the filtering of ISF codes in the receive stream. When FISF is set high, path AIS will only be inserted in the transmit stream after

detection of active ISF in three consecutive frames. Similarly, path AIS is removed after detection of inactive ISF in three consecutive frames. When FISF is set low, path AIS insertion occurs immediately on detection of active ISF and removal occurs immediately on detection of inactive ISF.

ITUAIS:

The insert tributary path AIS bits controls the insertion of Tributary Path AIS in the DROP bus. When ITUAIS is set high, columns in the DROP bus carrying tributary traffic are set to all ones. The pointer bytes (H1, H2, and H3), the path overhead column, and the fixed stuff columns are unaffected. Normal operation resumes when the ITUAIS bit is set low.

Reserved2:

The Reserved bit must be set to logic 0 for correct operation of the SPTX.

ISFI:

The incoming signal failure alarm interrupt status bit (ISFI) is set high when the TTAL detects a change in the ISF state (from normal to signal failure, or vice versa). This bit is cleared when this register is read.

ISFV:

The incoming signal failure alarm status bit (ISFV) reports the status of the ISF state derived from the ISF code in the tandem connection maintenance byte (Z5) of the ADD bus.

Register 48H, 88H, C8H: SPTB Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	RRAMACC	0
Bit 5	R/W	RTIUIE	0
Bit 4	R/W	RTIMIE	0
Bit 3	R/W	PER5	0
Bit 2	R/W	TNULL	1
Bit 1	R/W	NOSYNC	0
Bit 0	R/W	LEN16	0

This register controls the receive and transmit portions of the SPTB.

LEN16:

The path trace message length bit (LEN16) selects the length of the path trace message to be 16 bytes or 64 bytes.

NOSYNC:

The path trace message synchronization disable bit (NOSYNC) disables the writing of the path trace message into the trace buffer to be synchronized to the content of the message. When LEN16 is set high and NOSYNC is set low, the receive path trace message byte with its most significant bit set will be written to the first location in the buffer. When LEN16 is set low, and NOSYNC is also set low, the byte after the carriage return/linefeed (CR/LF) sequence will be written to the first location in the buffer. When NOSYNC is set high, synchronization is disabled, and the path trace message buffer behaves as a circular buffer.

TNULL:

The transmit null bit (TNULL) controls the insertion of an all-zero path trace identifier message in the transmit stream. When TNULL is set high, the contents of the transmit buffer is ignore and all-zeros bytes are provided to the TPOP block. When TNULL is set low the contents of the transmit path trace buffer is sent to TPOP. TNULL should be set high before changing the contents of the trace buffer to avoid sending partial messages.

PER5:

The receive trace identifier persistence bit (PER5) control the number of times a path trace identifier message must be received unchanged before being accepted. When PER5 is set high, a message is accepted when it is received unchanged five times consecutively. When PER5 is set low, the message is accepted after three identical repetitions.

RTIMIE:

The receive path trace identifier message mismatch interrupt enable bit (RTIMIE) controls the activation of the interrupt output when the comparison between accepted identifier message and the expected message changes state from match to mismatch and vice versa. When RTIMIE is set high, changes in match state activates the interrupt (INTB) output. When RTIMIE is set low, path trace identifier message state changes will not affect INTB.

RTIUIE:

The receive path trace identifier message unstable interrupt enable bit (RTIUIE) controls the activation of the interrupt output when the receive identifier message state changes from stable to unstable and vice versa. The unstable state is entered when the current identifier message differs from the previous message for eight messages. The stable state is entered when the same identifier message is received for three or five consecutive messages as controlled by the PER5 bit. When RTIUIE is set high, changes in the received path trace identifier message stable/unstable state of will activate the interrupt (INTB) output. When RTIUIE is set low, path trace identifier state changes will not affect INTB.

RRAMACC:

The receive RAM access control bit (RRAMACC) directs read and writes access to between the receive and transmit portion of the SPTX. When RRAMACC is set high, subsequent microprocessor read and write accesses are directed to the receive side trace buffers. When RRAMACC is set low, microprocessor accesses are directed to the transmit side trace buffer.

Register 49H, 89H, C9H: SPTB Path Trace Identifier Status

Bit	Type	Function	Default
Bit 7	R	BUSY	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	RTIUI	X
Bit 2	R	RTIUV	X
Bit 1	R	RTIMI	X
Bit 0	R	RTIMV	X

This register reports the path trace identifier status of the SPTB.

RTIMV:

The receive path trace identifier message mismatch status bit (RTIMV) reports the match/mismatch status of the identifier message framer. RTIMV is set high when the accepted identifier message differs from the expected message written by the microprocessor. RTIMV is set low when the accepted message matches the expected message.

RTIMI:

The receive path trace identifier mismatch interrupt status bit (RTIMI) is set high when match/mismatch status of the trace identifier framer changes state. This bit (and the interrupt) are cleared when this register is read.

RTIUV:

The receive path trace identifier message unstable status bit (RTIUV) reports the stable/unstable status of the identifier message framer. An unstable counter is increment when the current message differs from its immediate predecessor. RTIUV is set high when the unstable count reaches eight. RTIUV is set low when the current message becomes the accepted message.

RTIUI:

The receive path trace identifier message unstable interrupt status bit (RTIUI) is set high when stable/unstable status of the trace identifier framer changes state. This bit (and the interrupt) are cleared when this register is read.

BUSY:

The BUSY bit reports whether a previously initiated indirect read or write to a message buffer has been completed. BUSY is set high upon writing to the SPTB Indirect Address register, and stays high until the initiated access has completed. At which point, BUSY is set low. This register should be polled to determine when new data is available in the SPTB Indirect Data register.

Register 4AH, 8AH, CAH: SPTB Indirect Address Register

Bit	Type	Function	Default
Bit 7	R/W	RWB	0
Bit 6	R/W	A[6]	0
Bit 5	R/W	A[5]	0
Bit 4	R/W	A[4]	0
Bit 3	R/W	A[3]	0
Bit 2	R/W	A[2]	0
Bit 1	R/W	A[1]	0
Bit 0	R/W	A[0]	0

This register supplies the address used to index into path trace identifier buffers.

A0-A6:

The indirect read address bits (A[6:0]) indexes into the path trace identifier buffers. When RRAMACC is set high, addresses 0 to 63 reference the receive capture page while addresses 64 to 127 reference the receive expected page. The receive capture page contains the identifier bytes extracted from the receive stream. The receive expected page contains the expected trace identifier message down-loaded from the microprocessor. When RRAMACC is set low, addresses 0 to 63 reference the transmit message buffer which contains the identifier message to be inserted in the J1 bytes of the transmit stream. Addresses 64 to 127 are unused and must not be accessed.

RWB:

The access control bit (RWB) selects between an indirect read or write access to the static page of the path trace message buffer. Writing to this register initiates an external microprocessor access to the static page of the path trace message buffer. When RWB is set high, a read access is initiated. The data read can be found in the SPTB Indirect Data register. When RWB is set low, a write access is initiated. The data in the SPTB Indirect Data register will be written to the addressed location in the static page.

Register 4BH, 8BH, CBH: SPTB Indirect Data Register

Bit	Type	Function	Default
Bit 7	R/W	D[7]	0
Bit 6	R/W	D[6]	0
Bit 5	R/W	D[5]	0
Bit 4	R/W	D[4]	0
Bit 3	R/W	D[3]	0
Bit 2	R/W	D[2]	0
Bit 1	R/W	D[1]	0
Bit 0	R/W	D[0]	0

This register contains the data read from the path trace message buffer after a read operation or the data to be written into the buffer before a write operation.

D0-D7:

The indirect data bits (D[7:0]) reports the data read from a message buffer after an indirect read operation has completed. The data to be written to a buffer must be set up in this register before initiating an indirect write operation.

Register 4CH, 8CH, CCH: SPTB Expected Path Signal Label

Bit	Type	Function	Default
Bit 7	R/W	EPSL7	0
Bit 6	R/W	EPSL6	0
Bit 5	R/W	EPSL5	0
Bit 4	R/W	EPSL4	0
Bit 3	R/W	EPSL3	0
Bit 2	R/W	EPSL2	0
Bit 1	R/W	EPSL1	0
Bit 0	R/W	EPSL0	0

This register contains the expected path signal label byte in the receive stream..

EPSL7 - EPSL0:

The EPSL7 - EPSL0 bits contain the expected path signal label byte (C2). EPSL[7:0] is compared with the accepted path signal label extracted from the receive stream. A path signal label mismatch (PSLM) is declared if the accepted PSL differs from the expected PSL. Path AIS may be optionally inserted in the DROP bus when PSLM is declared. If enabled, an interrupt is asserted upon declaration and removal of PSLM.

Register 4DH, 8DH, CDH: SPTB Path Signal Label Status

Bit	Type	Function	Default
Bit 7	R/W	RPSLUIE	0
Bit 6	R/W	RPSLMIE	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	RPSLUI	X
Bit 2	R	RPSLUV	X
Bit 1	R	RPSLMI	X
Bit 0	R	RPSLMV	X

This register reports the path signal label status of the SPTB.

RPSLMV:

The receive path signal label mismatch status bit (RPSLMV) reports the match/mismatch status between the expected and the accepted path signal label. RPSLMV is set high when the accepted PSL differs from the expected PSL written by the microprocessor. PSLMV is set low when the accepted PSL matches the expected PSL.

RPSLMI:

The receive path signal label mismatch interrupt status bit (RPSLMI) is set high when the match/mismatch status between the accepted and the expected path signal label changes state. This bit (and the interrupt) are cleared when this register is read.

RPSLUV:

The receive path signal label unstable status bit (RPSLUV) reports the stable/unstable status of the path signal label in the receive stream. RPSLUV is set high when the current received C2 byte differs from the previous C2 byte for five consecutive frames. RPSLUV is set low when the same PSL code is received for five consecutive frames.

RPSLUI:

The receive path signal label unstable interrupt status bit (RPSLUI) is set high when the stable/unstable status of the path signal label changes state. This bit (and the interrupt) are cleared when this register is read.

RPSLMIE:

The receive path signal label mismatch interrupt enable bit (RPSLMIE) controls the activation of the interrupt output when the comparison between accepted and the expected path signal label changes state from match to mismatch and vice versa. When RPSLMIE is set high, changes in match state activates the interrupt (INTB) output. When RPSLMIE is set low, path signal label state changes will not affect INTB.

RPSLUIE:

The receive path signal label unstable interrupt enable bit (RPSLUIE) controls the activation of the interrupt output when the received path signal label changes state from stable to unstable and vice versa. When RPSLUIE is set high, changes in stable state activates the interrupt (INTB) output. When RPSLUIE is set low, path signal label state changes will not affect INTB.

11 TEST FEATURES DESCRIPTION

Simultaneously asserting (low) the CSB, RDB and WRB inputs causes all output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the SPTX. Test mode registers (as opposed to normal mode registers) are selected when TRS (A[8]) is high.

Test mode registers may also be used for board testing. When all of the TSBs within the SPTX are placed in test mode 0, device inputs may be read and device outputs may be forced via the microprocessor interface (refer to the section "Test Mode 0" for details).

11.1 Test Mode Register Memory Map

Table 6 - Test Mode Register Memory Map

Address	Register
000H-07FH	Normal Mode Registers
100H	Master Test
101H-1FFH	Reserved For Test

Notes on Test Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic 0. Reading back unused bits can produce either a logic 1 or a logic 0; hence unused register bits should be masked off by software when read.

2. Writeable test mode register bits are not initialized upon reset unless otherwise noted.

Register 100H: Master Test

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	W	PMCTST	X
Bit 3	W	DBCTRL	X
Bit 2	R/W	IOTST	0
Bit 1	W	HIZDATA	X
Bit 0	R/W	HIZIO	0

This register is used to enable SPTX test features. All bits, except PMCTST, are reset to zero by a reset of the SPTX.

HIZIO,HIZDATA:

The HIZIO and HIZDATA bits control the tri-state modes of the SPTX . While the HIZIO bit is a logic 1, all output pins of the SPTX except the data bus are held in a high-impedance state. The microprocessor interface is still active. While the HIZDATA bit is a logic 1, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles.

IOTST:

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each TSB block in the SPTX for board level testing. When IOTST is a logic 1, all blocks are held in test mode and the microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block and consequently the device outputs (refer to the "Test Mode 0 Details" in the "Test Features" section).

DBCTRL:

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic 1, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the SPTX to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The

DBCTRL bit is used to measure the drive capability of the data bus driver pads.

PMCTST:

The PMCTST bit is used to configure the SPTX for PMC's manufacturing tests. When PMCTST is set to logic 1, the SPTX microprocessor port becomes the test access port used to run the PMC "canned" manufacturing test vectors. The PMCTST bit is logically "ORed" with the IOTST bit, and can only be cleared by setting CSB to logic 1.

11.2 I/O Test Mode

In I/O test mode (IOTST in Master Test Register set high), the SPTX allows the logic levels on the device inputs to be read through the microprocessor interface, and allows the device outputs to be forced to either logic level through the microprocessor interface.

Test Register 101H: (Write in I/O test mode)

Bit	Type	Function	Default
Bit 7	W	TD[7]	X
Bit 6	W	TD[6]	X
Bit 5	W	TD[5]	X
Bit 4	W	TD[4]	X
Bit 3	W	TD[3]	X
Bit 2	W	TD[2]	X
Bit 1	W	TD[1]	X
Bit 0	W	TD[0]	X

Test Register 102H: (Write in I/O test mode)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	W	INTB	X
Bit 4	W	RAD	X
Bit 3	W	TFPOUT	X
Bit 2	W	TDP	X
Bit 1	W	TPL	X
Bit 0	W	TC1J1V1	X

Test Register 103H: (Write in I/O test mode)

Bit	Type	Function	Default
Bit 7	W	DD[7]	X
Bit 6	W	DD[6]	X
Bit 5	W	DD[5]	X
Bit 4	W	DD[4]	X
Bit 3	W	DD[3]	X
Bit 2	W	DD[2]	X
Bit 1	W	DD[1]	X
Bit 0	W	DD[0]	X

Test Register 104H: (Write in I/O test mode)

Bit	Type	Function	Default
Bit 7	W	GD[1]	X
Bit 6	W	GD[0]	X
Bit 5	W	GPL	X
Bit 4	W	GC1J1V1	X
Bit 3	W	GDP	X
Bit 2	W	DDP	X
Bit 1	W	DPL	X
Bit 0	W	DC1J1V1	X

Test Register 101H: (Read in I/O test mode)

Bit	Type	Function	Default
Bit 7	R	PIN[7]	X
Bit 6	R	PIN[6]	X
Bit 5	R	PIN[5]	X
Bit 4	R	PIN[4]	X
Bit 3	R	PIN[3]	X
Bit 2	R	PIN[2]	X
Bit 1	R	PIN[1]	X
Bit 0	R	PIN[0]	X

Test Register 102H: (Read in I/O test mode)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	TPAIS[3]	X
Bit 5	R	TPAIS[2]	X
Bit 4	R	TPAIS[1]	X
Bit 3	R	TFP	X
Bit 2	R	RDP	X
Bit 1	R	RPL	X
Bit 0	R	IFP	X

Test Register 103H: (Read in I/O test mode)

Bit	Type	Function	Default
Bit 7	R	AD[7]	X
Bit 6	R	AD[6]	X
Bit 5	R	AD[5]	X
Bit 4	R	AD[4]	X
Bit 3	R	AD[3]	X
Bit 2	R	AD[2]	X
Bit 1	R	AD[1]	X
Bit 0	R	AD[0]	X

Test Register 104H: (Read in I/O test mode)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	DPAIS[3]	X
Bit 5	R	DPAIS[2]	X
Bit 4	R	DPAIS[1]	X
Bit 3	R	DFP	X
Bit 2	R	ADP	X
Bit 1	R	APL	X
Bit 0	R	AC1J1V1	X

Notes:

†Writing a logic 1 to any of the block interrupt signals asserts the INTB output low.

Test Register 105H: (Read in I/O test mode)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	GMFP	X
Bit 2	R	GFP	X
Bit 1	R	TAD	X
Bit 0	R	TAFP	X

12 OPERATION

The SPTX is a SONET (SDH) path terminating transceiver. It processes the path overhead of an STS-1 stream, an STS-3c (STM-1 carrying an AU4) or an STS-3 (STM-1 carrying 3 AU3s).

In the receive section, the SPTX interprets the incoming STS (AU) pointer(s) to locate the path overhead column(s). A variety of path level statistics, such as BIP-8 errors, and pointer justification events are accumulated for performance monitoring purposes. The path overhead bytes are serialized on low speed interface for external processing. The synchronous payload envelope (virtual container) in the receive stream is placed on a Telecombus formatted DROP bus. Plesiochronous timing relationships between the receive stream and the DROP bus is accommodated via pointer processing.

In the transmit section, the SPTX takes payload data from a Telecombus formatted ADD bus, inserts the path overhead column, and places the resulting synchronous payload envelope (virtual container) in the transmit stream. Path overhead data may be sourced from internal registers or from a low speed serial interface. Plesiochronous timing relationships between the transmit stream and the ADD bus is accommodated via pointer processing.

The SPTX is also a SONET (SDH) tandem connection terminating transceiver. In a piece of originating tandem connection termination equipment (TCTE), the SPTX sources a tandem connection maintenance byte (Z5) reporting incoming BIP-8 errors and a data link sourced from a low speed serial interface. The BIP-8 byte (B3) is updated to reflect changes to the Z5 byte. In a piece of terminating TCTE, the SPTX reconstructs the path AIS indication received at the originating TCTE. SPTXs residing in the middle of a tandem connection may be programmed to pass the path overhead unchanged.

12.1 Configuration Options

12.1.1 STS-1 (Single AU3) Mode

The SPTX terminates and sources the payload path of a duplex STS-1 stream or one-third of an STM-1 stream carrying three AU3 administrative units. The receive and transmit stream as well as the ADD and DROP bus clock rate is 6.48 MHz.

12.1.2 STS-3 (Triple AU3) Mode

The SPTX terminates and sources the payload path of a duplex STS-3 stream or an STM-1 stream carrying three AU3 administrative units. The path overhead of the three multiplexed STS-1 streams (AU3 administrative units) are processed independently. The receive and transmit stream as well as the ADD and DROP bus clock rate is 19.44 MHz.

12.1.3 STS-3c (AU4) Mode

The SPTX terminates and sources the payload path of a duplex STS-3c stream or an STM-1 stream carrying a single AU4 administrative unit. The receive and transmit stream as well as the ADD and DROP bus clock rate is 19.44 MHz.

12.1.4 Originating TCTE Mode

The SPTX receive section originates a tandem connection. Incoming BIP-8 errors and a data link are inserted in the tandem connection maintenance byte (Z5) of the DROP bus. The remaining path overhead bytes are unchanged, except under path AIS conditions. The SPTX transmit section operates independently in any applicable mode with transmit TCTE bypass mode being most likely. The receive and transmit stream as well as the ADD and DROP bus clock rate may be 6.48 MHz or 19.44 MHz, as appropriate.

12.1.5 Transmit TCTE Terminating Mode

The SPTX transmit section terminates a tandem connection. Incoming signal failure indication (ISF) generated by the originating TCTE triggers path AIS insertion in the transmit stream. The SPTX receive section operates independently in any applicable mode with receive TCTE bypass mode being most likely. The receive and transmit stream as well as the ADD and DROP bus clock rate may be 6.48 MHz or 19.44 MHz, as appropriate.

12.1.6 Path and TCTE Terminating Mode

The SPTX receive section is simultaneously terminating a path payload and a tandem connection. The incoming error count (IEC) in the tandem connection maintenance byte (Z5) is accumulated and the data link serialized on the low speed RPOH output. Received incoming signal failure code (ISF) will trigger path AIS insertion in the DROP bus. The transmit section of the SPTX is unlikely to be in any of the TCTE modes.

12.1.7 Receive TCTE Bypass Mode

The SPTX receive section interprets the incoming pointer on the receive stream and passively monitors the receive path overhead. The path overhead data on the receive stream is placed unchanged in the DROP bus.

12.1.8 Transmit TCTE Bypass Mode

The SPTX transmit section does not source the path overhead in the transmit stream. The path overhead data on the ADD bus is placed unchanged in the transmit stream.

13 FUNCTIONAL TIMING

The functional timing of receive and transmit streams and the ADD and DROP buses is illustrated in Figures 3 to 32. Transport overhead bytes are labelled for notational convenience only. With the exception of the pointer bytes (H1, H2, H3), TOH bytes in the receive stream are ignore as are all TOH bytes on the ADD bus. In the transmit stream and on the DROP bus, TOH bytes (except pointers) are set to zero.

13.1 Receive Section

13.1.1 Receive Stream Timing

Figure 5 below shows the receive stream timing in STS-1 mode. PICLK is a 6.48 MHz clock. The frame pulse IFP marks the first synchronous payload envelope byte in the STS-1 frame. It is not necessary for IFP to be present at every frame. An internal counter fly-wheels based on the most recent IFP received. The negative stuff opportunity byte is labelled (H3) and the positive stuff opportunity byte is labelled (PSO). In a negative justification event, an extra payload data byte is carried in the H3 byte. In a positive justification event, the PSO byte temporarily carries a stuff byte instead of payload data.

Figure 5 - STS-1 (Single AU3) Receive Stream Timing

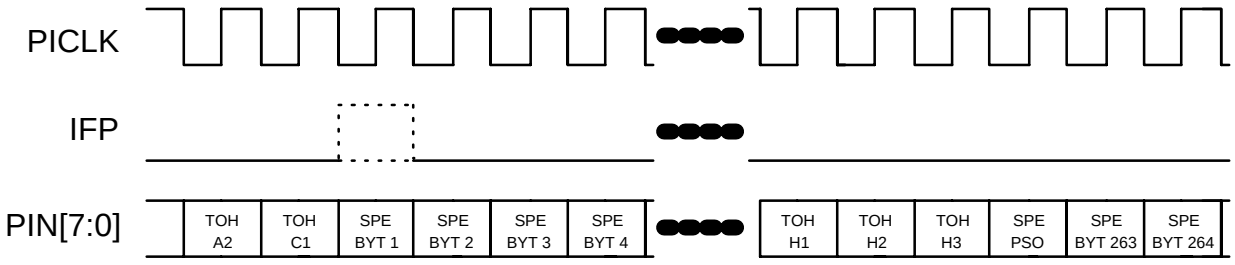


Figure 6 below shows the receive stream timing in STS-3 mode. PICLK is a 19.44 MHz clock. The frame pulse IFP marks the first synchronous payload envelope byte in the first STS-1 stream in the STS-3 frame. It is not necessary for IFP to be present at every frame. An internal counter fly-wheels based on the most recent IFP received.

Figure 6 - STS-3 (STM1 - AU3) Receive Stream Timing

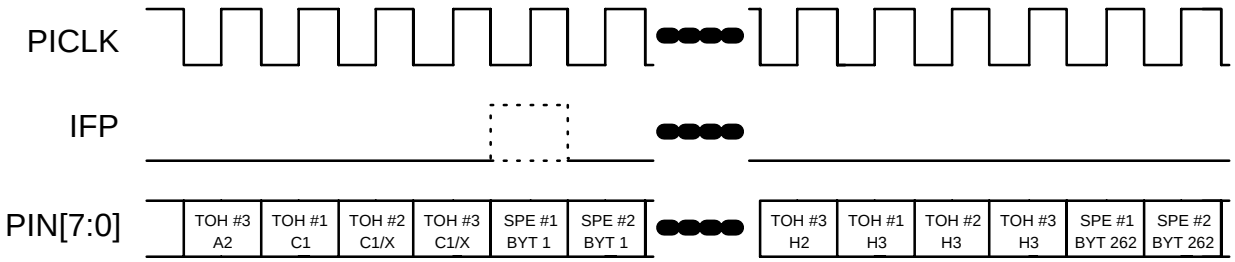
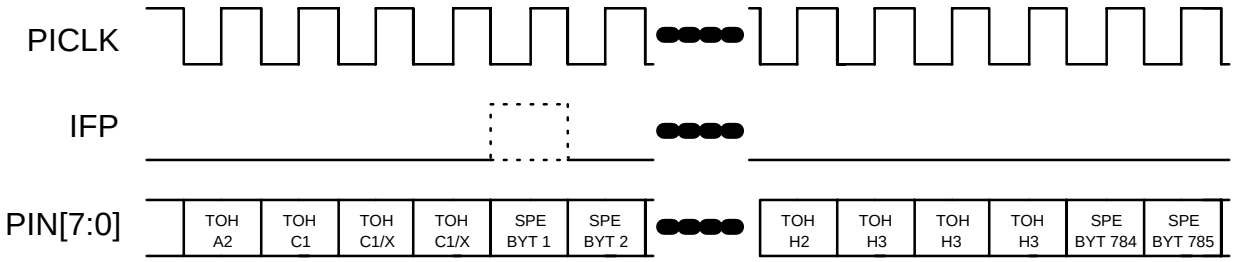


Figure 7 below shows the receive stream timing in STS-3c mode. PICLK is a 19.44 MHz clock. The frame pulse IFP marks the first synchronous payload envelope byte in the in the STS-3c frame. It is not necessary for IFP to be present at every frame. An internal counter fly-wheels based on the most recent IFP received.

Figure 7 - STS-3c (STM1 - AU4) Receive Stream Timing



13.1.2 External Path Termination RECEIVE Bus Timing

Figure 8 below shows the RECEIVE bus timing in STS-1 mode when external path termination is enabled. RCK is a 6.48 MHz clock. Transport overhead and payload bytes are distinguished by the RPL input which is set low to mark transport overhead bytes and set high to mark payload bytes. During a negative justification event (labelled NJE), RPL is set high during the H3 byte to indicate that payload data is available. During a positive justification event (labelled PJE), RPL is set low during the PSO byte to indicate that payload data is not available. The RECEIVE bus composite timing signal RC1J1V1 is set high when RPL is set low to mark the C1 byte. RC1J1V1 is set high when RPL is also set high to mark the J1 byte. Optionally, RC1J1V1 is set high on the first payload byte after J1 once every multiframe to mark the first frame of the RECEIVE bus tributary multiframe. The alignment of the transport frame and the synchronous payload envelope shown in Figure 6 corresponds to an active offset of 523 and is for

illustration only. Other alignments are possible. The RECEIVE bus parity input RDP carries the parity of RD[7:0] and optionally includes RPL and RC1J1V1.

Figure 8 - STS-1 Mode RECEIVE Bus Timing

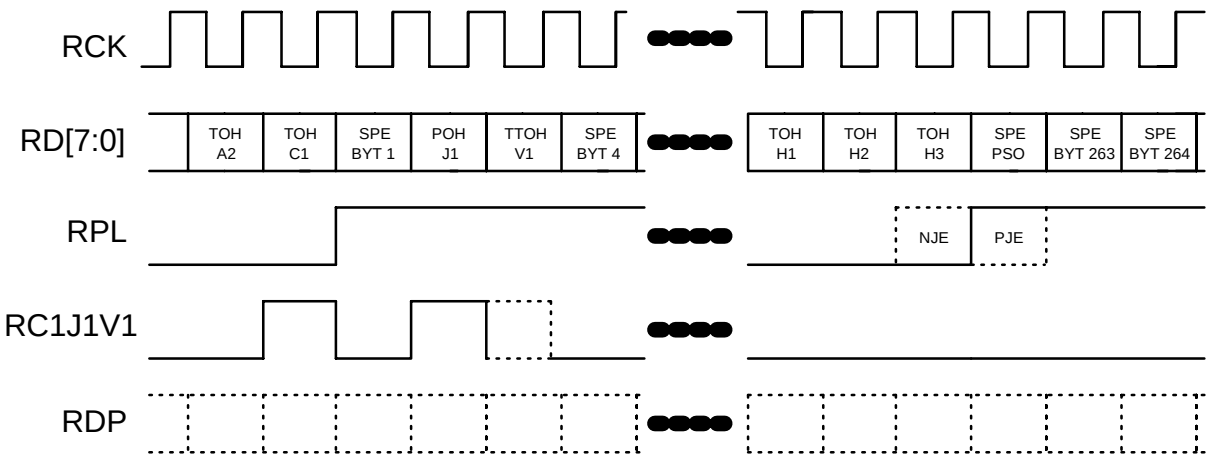


Figure 9 below shows the RECEIVE bus timing in STS-3 mode. RCK is a 19.44 MHz clock. Transport overhead and payload bytes are distinguished by the RPL input which is set low to mark transport overhead bytes and set high to mark payload bytes. A positive justification event is shown for STS-1 #3 Figure 9. A stuff byte is place in the positive stuff opportunity byte and RPL is set low to indicate that data is not available. The RECEIVE bus composite timing signal RC1J1V1 is set high when RPL is set low to mark the C1 byte. RC1J1V1 is set high when RPL is also set high to mark the J1 byte in each of the three STS-1 streams. Optionally, RC1J1V1 is set high once every multiframe to mark the first frame of the RECEIVE bus tributary multiframe in each STS-1 stream. The alignment of the transport frame and the synchronous payload envelope of STS-1 #1 shown in Figure 9 corresponds to an active offset of 0 and is for illustration only. Other alignments are possible. The RECEIVE bus parity input RDP carries the parity of RD[7:0] and optionally includes RPL and RC1J1V1.

Figure 9 - STS-3 (STM1 - AU3) Mode RECEIVE Bus Timing

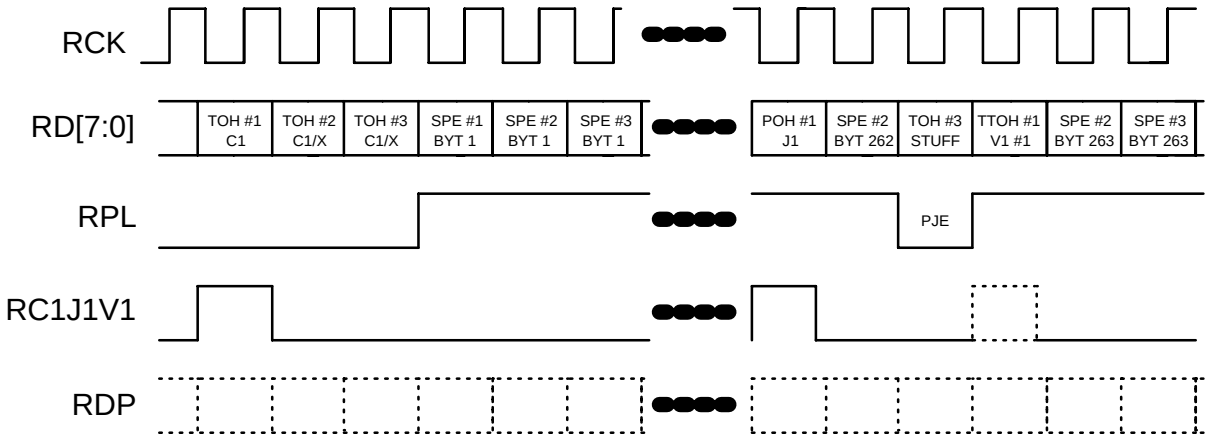
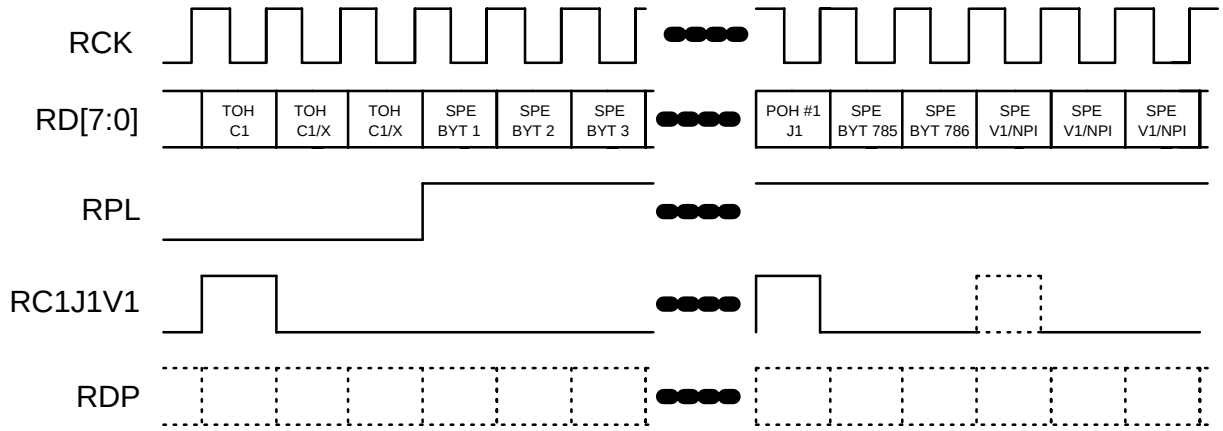


Figure 10 below shows the RECEIVE bus timing in STS-3c mode. RCK is a 19.44 MHz clock. Transport overhead and payload bytes are distinguished by the RPL input which is set low to mark transport overhead bytes and set high to mark payload bytes. The RECEIVE bus composite timing signal RC1J1V1 is set high when RPL is set low to mark the C1 byte. RC1J1V1 is set high when RPL is also set high to mark the J1 byte in each of the three STS-1 streams. Optionally, RC1J1V1 is set high once every multiframe to mark the first frame of the RECEIVE bus tributary multiframe. When processing an STS-3c stream, the V1 pulse marks the V1 byte of the first tributary. When processing an STM1 stream carrying an AU4, the V1 pulse marks the more significant byte of the Null Pointer Indication (NPI) of the first frame in each tributary multiframe. The alignment of the transport frame and the synchronous payload envelope of STS-3c stream shown in Figure 10 corresponds to an active offset of 0 and is for illustration only. Other alignments are possible. The RECEIVE bus parity input RDP carries the parity of RD[7:0] and optionally includes RPL and RC1J1V1.

Figure 10 - STS-3c (STM1 - AU4) Mode RECEIVE Bus Timing



13.1.3 DROP Bus Timing

Figure 11 below shows the DROP bus timing in STS-1 mode. DCK is a 6.48 MHz clock. The frame pulse DFP marks the first synchronous payload envelope byte in the STS-1 frame on DD[7:0]. It is not necessary for DFP to be present at every frame. An internal counter fly-wheels based on the most recent DFP received. Transport overhead and payload bytes are distinguished by the DPL output which is set low to mark transport overhead bytes and set high to mark payload bytes. During a negative justification event (labelled NJE), DPL is set high during the H3 byte to indicate that payload data is available. During a positive justification event (labelled PJE), DPL is set low during the PSO byte to indicate that payload data is not available. The DROP bus composite timing signal DC1J1V1 is set high when DPL is set low to mark the C1 byte. DC1J1V1 is set high when DPL is also set high to mark the J1 byte. Optionally, DC1J1V1 is set high on the first payload byte after J1 once every multiframe to mark the first frame of the DROP bus tributary multiframe. The alignment of the transport frame and the synchronous payload envelope shown in Figure 11 corresponds to an active offset of 523 and is for illustration only. Other alignments are possible. The DROP bus parity output DDP reports the parity of DD[7:0] and optionally includes DPL and DC1J1V1.

Figure 11 - STS-1 Mode DROP Bus Timing

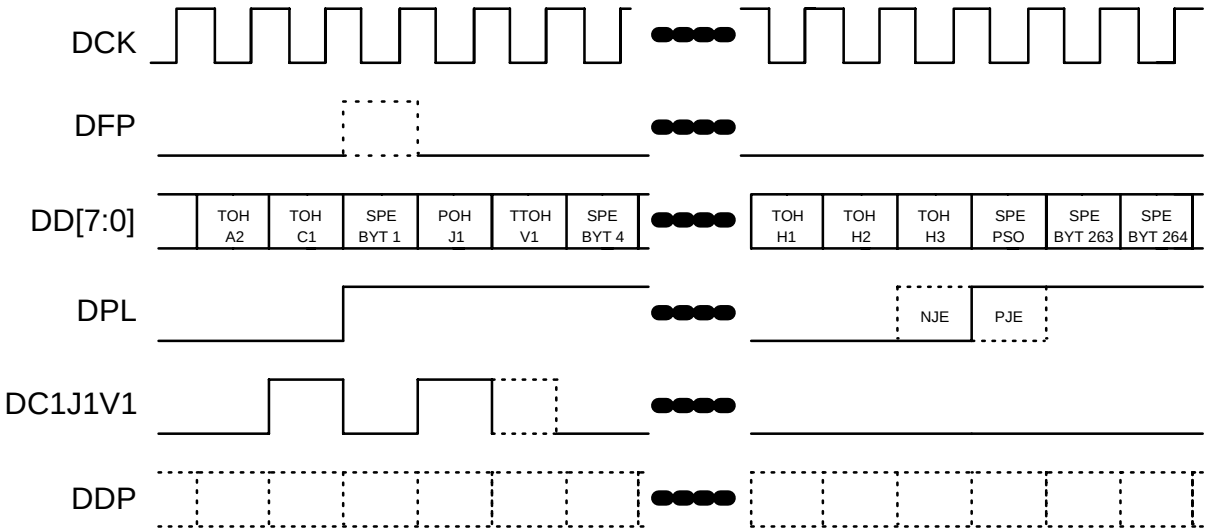


Figure 12 below shows the DROP bus timing in STS-3 mode. DCK is a 19.44 MHz clock. The frame pulse DFP marks the first synchronous payload envelope byte in the STS-3 frame on DD[7:0]. It is not necessary for DFP to be present at every frame. An internal counter fly-wheels based on the most recent DFP received. Transport overhead and payload bytes are distinguished by the DPL output which is set low to mark transport overhead bytes and set high to mark payload bytes. A positive justification event is shown for STS-1 #3 Figure 9. A stuff byte is place in the positive stuff opportunity byte and DPL is set low to indicate that data is not available. The DROP bus composite timing signal DC1J1V1 is set high when DPL is set low to mark the C1 byte. DC1J1V1 is set high when DPL is also set high to mark the J1 byte in each of the three STS-1 streams. Optionally, DC1J1V1 is set high once every multiframe to mark the first frame of the DROP bus tributary multiframe in each STS-1 stream. The alignment of the transport frame and the synchronous payload envelope of STS-1 #1 shown in Figure 12 corresponds to an active offset of 0 and is for illustration only. Other alignments are possible. The DROP bus parity output DDP reports the parity of DD[7:0] and optionally includes DPL and DC1J1V1.

Figure 12 - STS-3 (STM1 - AU3) Mode DROP Bus Timing

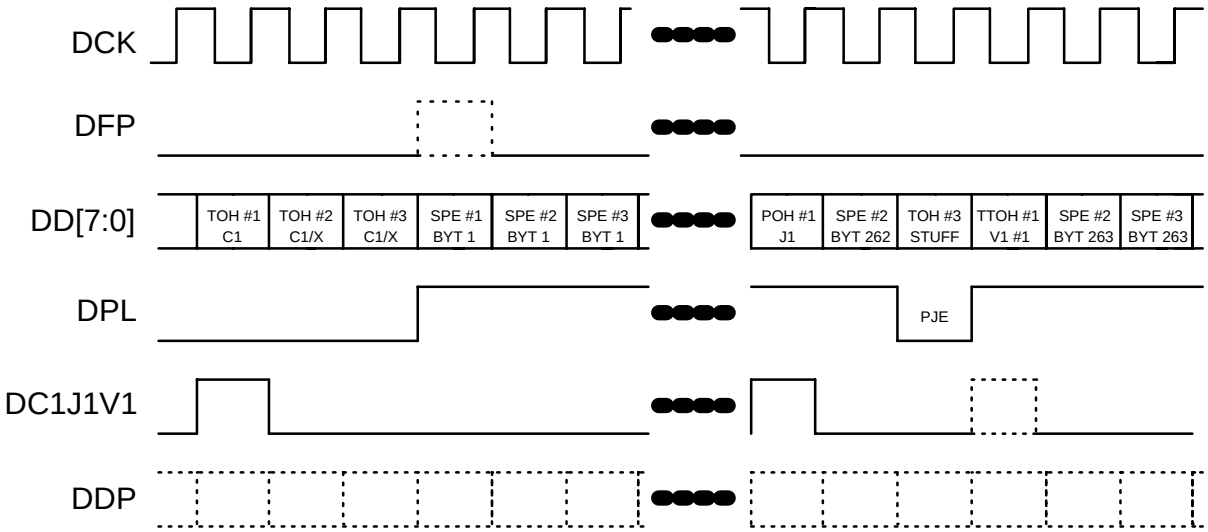
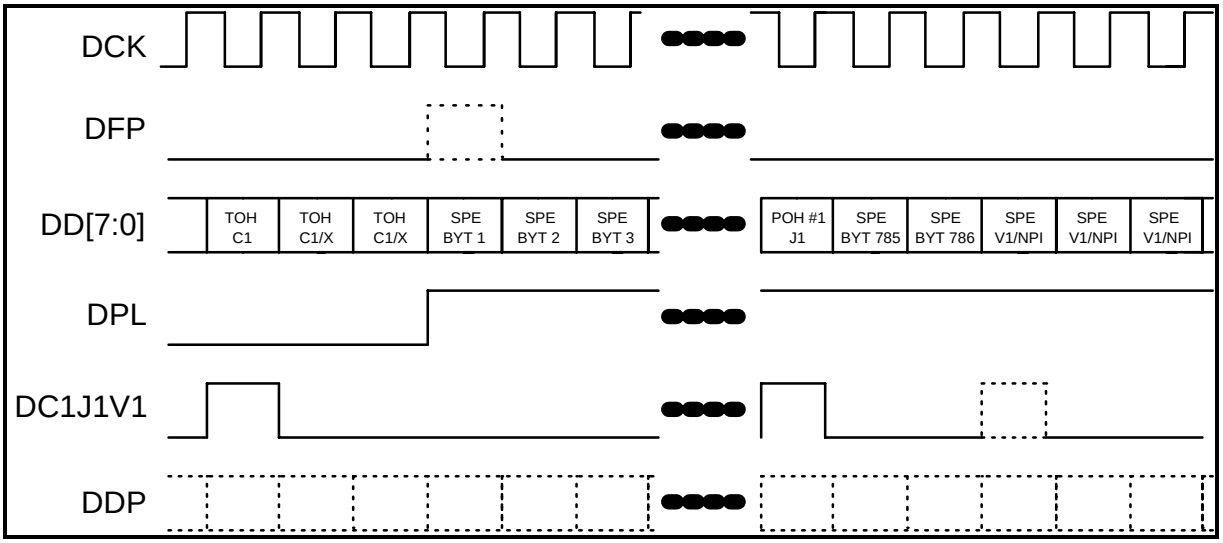


Figure 13 below shows the DROP bus timing in STS-3c mode. DCK is a 19.44 MHz clock. The frame pulse DFP marks the first synchronous payload envelope byte on DD[7:0]. It is not necessary for DFP to be present at every frame. An internal counter fly-wheels based on the most recent DFP received. Transport overhead and payload bytes are distinguished by the DPL output which is set low to mark transport overhead bytes and set high to mark payload bytes. The DROP bus composite timing signal DC1J1V1 is set high when DPL is set low to mark the C1 byte. DC1J1V1 is set high when DPL is also set high to mark the J1 byte in each of the three STS-1 streams. Optionally, DC1J1V1 is set high once every multiframe to mark the first frame of the DROP bus tributary multiframe. When processing an STS-3c stream, the V1 pulse marks the V1 byte of the first tributary. When processing and STM1 stream carrying an AU4, the V1 pulse marks the more significant byte of the Null Pointer Indication (NPI) of the first frame in each tributary multiframe. The alignment of the transport frame and the synchronous payload envelope of STS-3c stream shown in Figure 13 corresponds to an active offset of 0 and is for illustration only. Other alignments are possible. The DROP bus parity output DDP reports the parity of DD[7:0] and optionally includes DPL and DC1J1V1.

Figure 13 - STS-3c (STM1 - AU4) Mode DROP Bus Timing



13.1.4 Receive Low-speed Interface Timing

Figure 14 below shows the extraction of the path overhead column into a low speed serial stream. RPOHCK[3:1] are nominally 576 kHz clocks. The entire path overhead (J1, B3, C2, G1, F2, H4, Z3, Z4, Z5 bytes) is extracted, serialized and placed on RPOH[3:1] over a frame period. For each byte, the most significant bit is transmitted first. RPOHFP[3:1] mark the most significant bit of the J1 byte. BIPE[3:1] identify the bits within the B3 bytes containing a parity error. The index in the signal names refer to the STS-1 stream number within the receive STS-3 stream. I.e., signals carrying an index of 1 reflect the status of STS-1 #1, those with index of 2 reflect STS-1 #2, and those with index of 3 reflex STS-1 #3. In STS-1 or STS-3c mode, only RPOHCK[1], RPOH[1], RPOHFP[1] and BIPE[1] are active. The remaining outputs are set low.

Figure 14 - Receive Path Overhead Extraction Timing

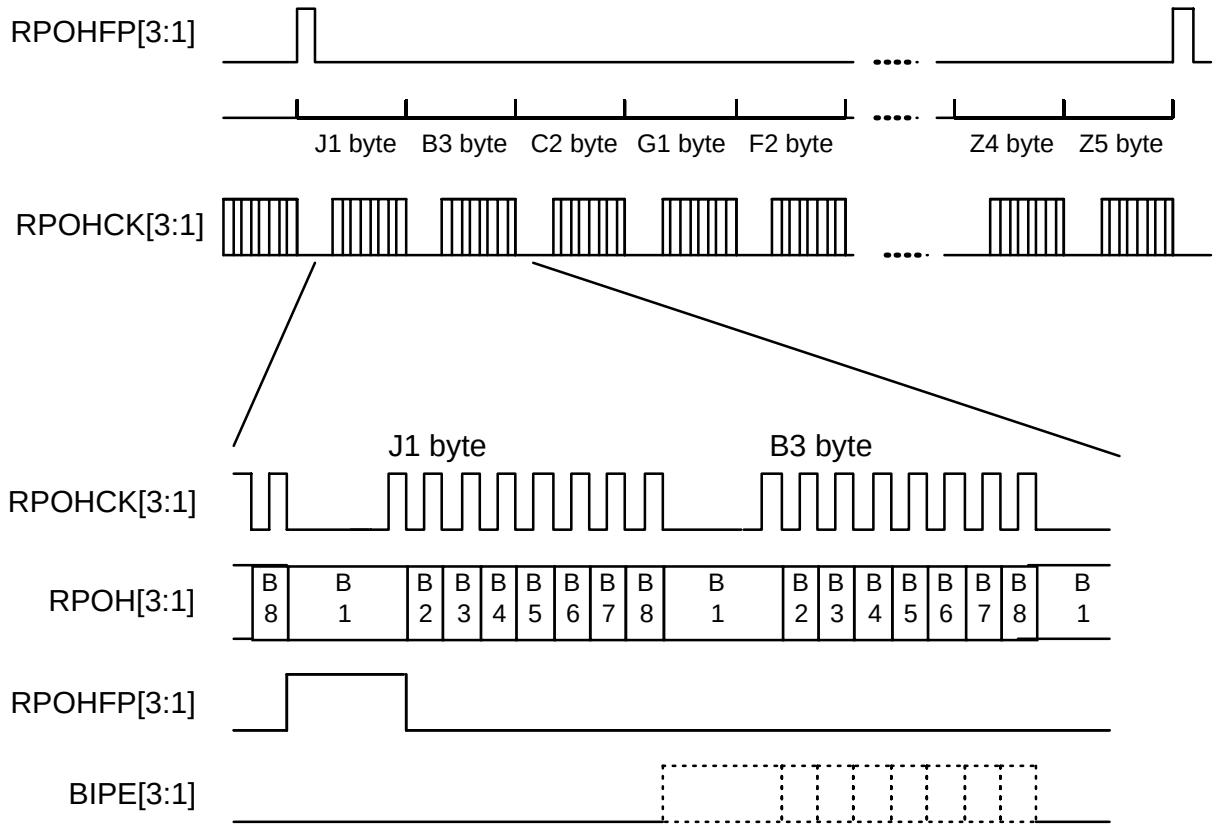


Figure 15 below shows the format of the receive alarm port. The path BIP-8 counts from all three STS-1 streams are serialized in the receive alarm data output (RAD) and clocked out by RPOHCK[1]. The eight BIP count bit positions for each STS-1 are left justified. If there are eight BIP errors in the corresponding STS-1 stream, all bit positions are set high. If there are fewer BIP errors, only the first N positions corresponding to the number of detected errors are set high, the remainder are set low. The FERF bit is set high when path AIS is inserted in the DROP bus for the corresponding STS-1 stream. In STS-1 or STS-3c mode, only the bit positions assigned to STS-1 #1 are active, those assigned to streams #2, and #3 are set low.

Figure 15 - Receive Alarm Port Timing

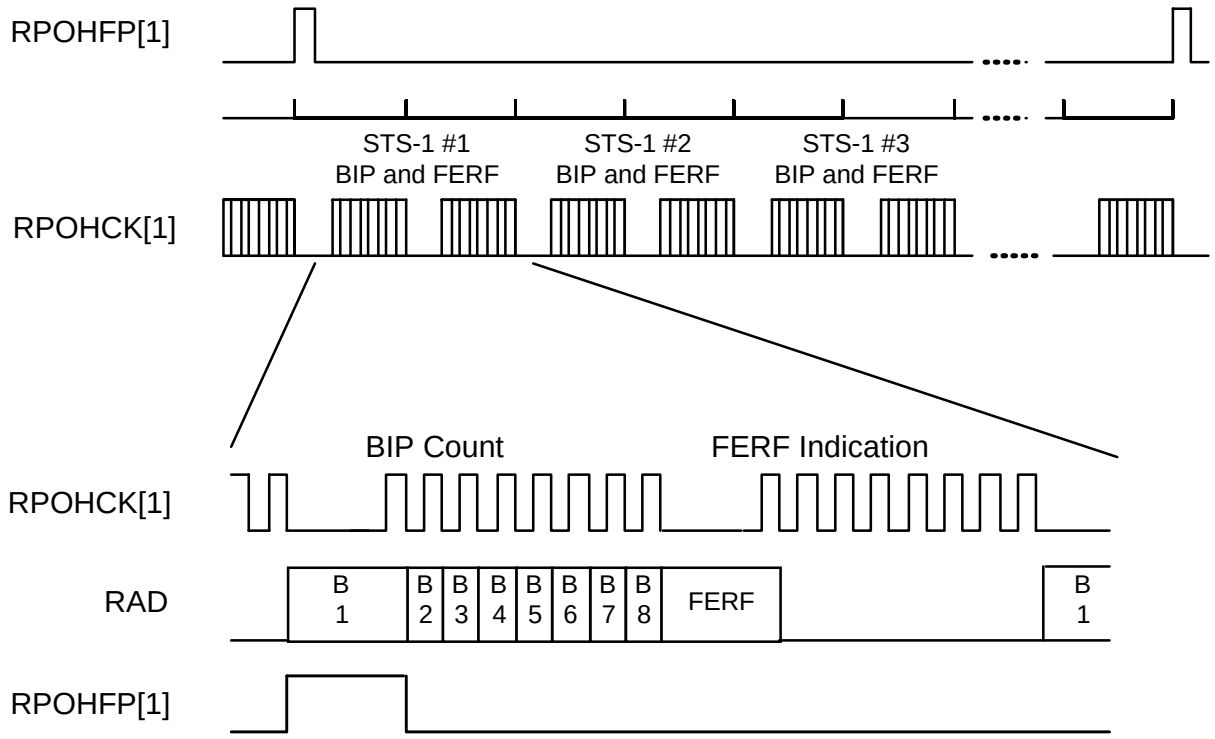
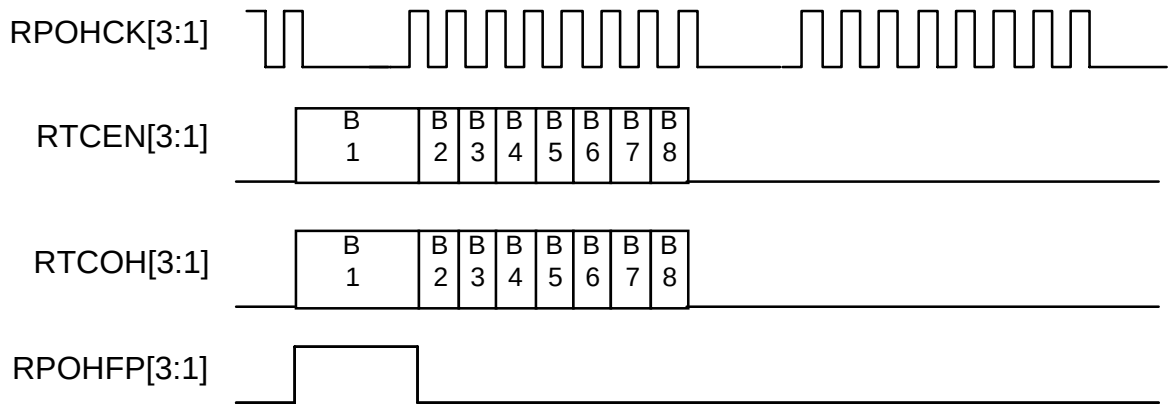


Figure 16 below illustrates the Tandem Connection Maintenance byte interface. RTCOH[3:1] carries the data to be inserted in the tandem connection maintenance byte (Z5) in the DROP bus. RTCOH[1] and RTCEN[1] are associated with STS-1 #1, RTCOH[2] and RTCEN[2] with STS-1 #2, and RTCOH[3] and RTCEN[3] with STS-1 #3. The first bit on RTCOH (B1) corresponds to the most significant bit of Z5. The RTCEN[3:1] signal controls whether the corresponding bit in RTCOH[3:1] is inserted in the Z5 byte. The data bit on RTCOH[3:1] is inserted in the Z5 byte if the corresponding bit of RTCEN[3:1] is high. The incoming error count bit or a logic one data link bit is placed on the Z5 byte if the corresponding bit in RTCEN[3:1] is low.

Figure 16 - Receive Tandem Connect Maintenance Insertion Timing



13.1.5 Receive Alarm Status Timing

Figure 17 below illustrates the operation of the loss of pointer outputs (LOP[3:1]). LOP[1], LOP[2], LOP[3] reports the status of streams STS-1 #1, #2, and #3, respectively. In STS-1 or STS-3c mode, only LOP[1] is active. LOP[3:2] are set low. Loss of pointer is declared if a valid pointer has not been received in eight consecutive frames. Loss of pointer is removed immediately if the same valid pointer is received in three consecutive frames.

Figure 17 - Loss of Pointer (LOP) Declaration/Removal Timing

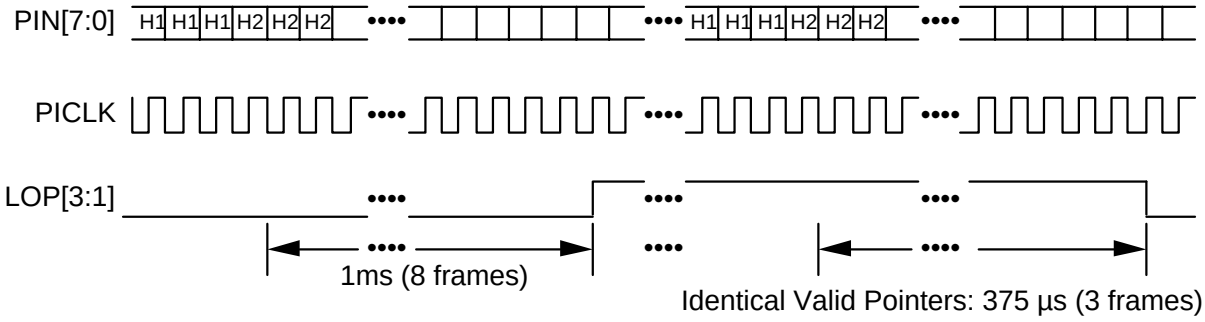


Figure 18 below illustrates the operation of the path AIS outputs (PAIS[3:1]). PAIS[1], PAIS[2], PAIS[3] reports the status of receive streams STS-1 #1, #2, and #3, respectively. In STS-1 or STS-3c mode, only PAIS[1] is active. PAIS[3:2] are set low. Path AIS is declared if an all-ones pointer is received for three consecutive frames. Path AIS is removed immediately if a valid pointer with

active NDF is received or if the same valid pointer is received in three consecutive frames.

Figure 18 - Path AIS (PAIS) Declaration/Removal Timing

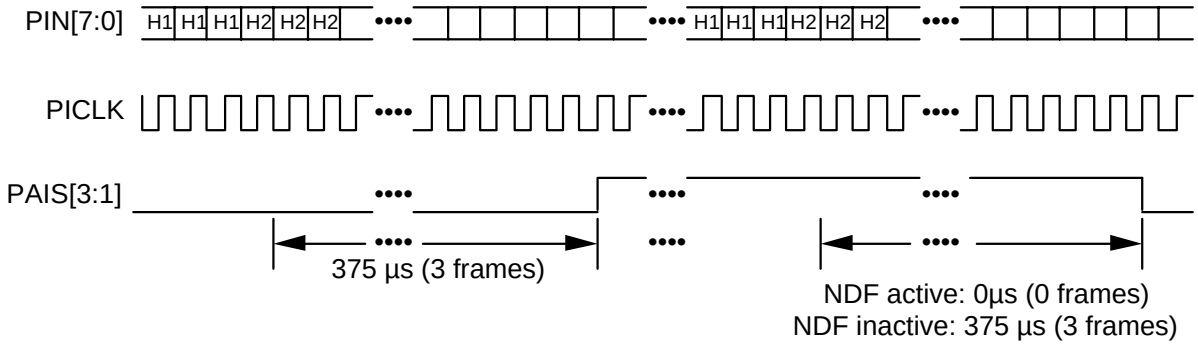


Figure 19 below illustrates the operation of the path FERF alarm outputs (PFERF[3:1]). PFERF[1], PFERF[2], PFERF[3] reports the status of streams STS-1 #1, #2, and #3, respectively. In STS-1 or STS-3c mode, only PFERF[1] is active. PFERF[3:2] are set low. Path FERF alarm is declared the path FERF bit in the path status byte (G1) is set high for ten consecutive frames. Path FERF alarm is removed if the path FERF bit is set low for ten consecutive frames.

Figure 19 - Path FERF Alarm (PFERF) Declaration/Removal Timing

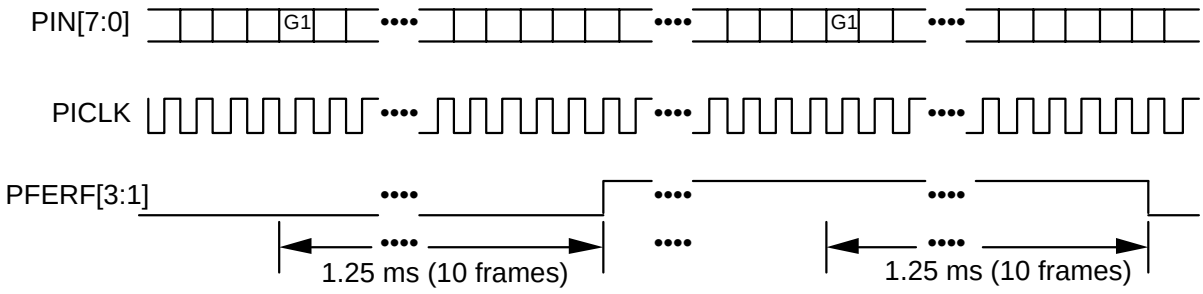
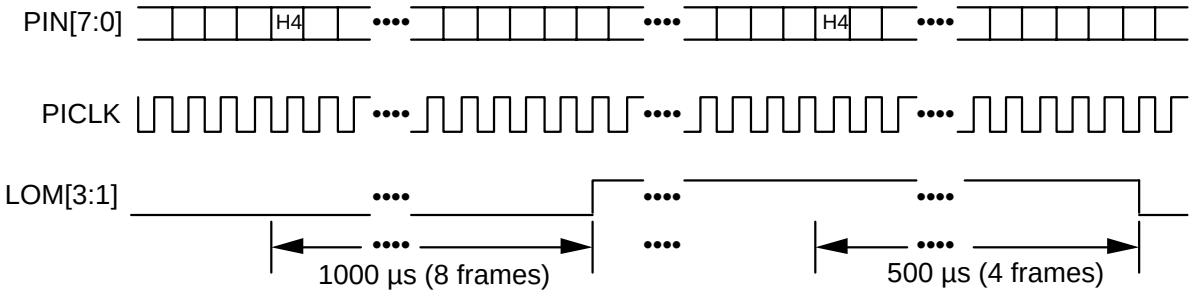


Figure 20 below illustrates the operation of the loss of multiframe outputs (LOM[3:1]). LOM[1], LOM[2], LOM[3] reports the status of streams STS-1 #1, #2, and #3, respectively. In STS-1 or STS-3c mode, only LOM[1] is active. LOM[3:2] are set low. The internal state of Out of Multiframe (OOM) is declared when the least significant two bits of the H4 byte do not follow the expected sequence. OOM is removed if the least significant two bits of the H4 byte follow in sequence for four frames. Loss of multiframe is declared when OOM remains in effect for eight consecutive frames periods (After the ninth H4 starting with the

first non-sequential H4). Loss of multiframe is removed when the H4 byte follows the expected patten for four consecutive frames.

Figure 20 - Loss of Multiframe (LOM) Declaration/Removal Timing



13.2 Transmit Section

13.2.1 GENERATED Bus Timing

Figure 21 below shows the GENERATED bus timing in STS-1 mode. ACK is a 6.48 MHz clock. The frame pulse GFP marks the first synchronous payload envelope byte in the STS-1 frame on GD[1:0]. The tributary multiframe frame pulse GMFP marks the byte after J1 of the first frame in a tributary multiframe on GD[1:0]. It is not necessary for GFP or GMFP to be present at every opportunity. Internal counters fly-wheel based on the most recent GFP and GMFP received. In the first frame of a tributary multiframe, GD[1:0] is set to 01B. The data on GD[1:0] is update once per frame on the byte after the J1 byte in the sequence of 01B, 10B, 11B and 00B. Transport overhead and payload bytes are distinguished by the GPL output which is set low to mark transport overhead bytes and set high to mark payload bytes. During a negative justification event (labelled NJE), GPL is set high during the H3 byte to indicate that payload data is available. During a positive justification event (labelled PJE), GPL is set low during the PSO byte to indicate that payload data is not available. The GENERATED bus composite timing signal GC1J1V1 is set high when GPL is set low to mark the C1 byte. GC1J1V1 is set high when GPL is also set high to mark the J1 byte. Optionally, GC1J1V1 is set high on the first payload byte after J1 to mark the first frame of the GENERATED bus tributary multiframe. The alignment of the transport frame and the synchronous payload envelope shown in Figure 21 corresponds to an active offset of 523 and is for illustration only. Other alignments are possible. The GENERATED bus parity output GDP reports the parity of GD[G:0] and optionally includes GPL and GC1J1V1.

Figure 21 - STS-1 Mode GENERATED Bus Timing

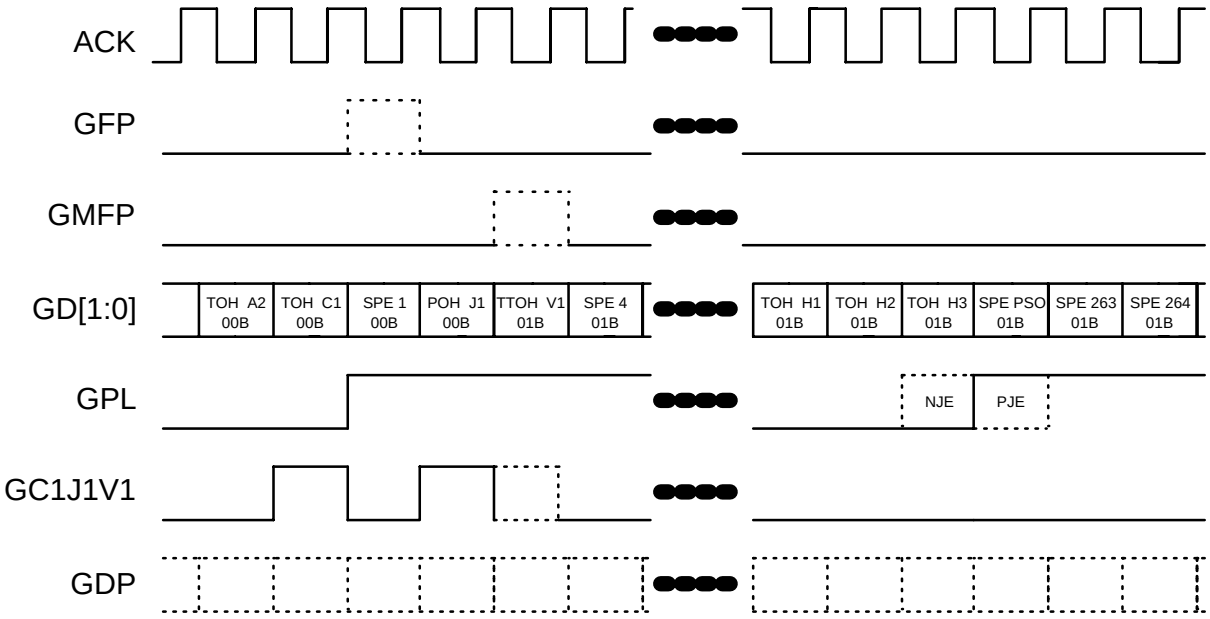


Figure 22 below shows the GENERATED bus timing in STS-3 mode. ACK is a 19.44 MHz clock. The frame pulse GFP marks the first synchronous payload envelope byte in the STS-3 frame on GD[1:0]. The tributary multiframe frame pulse GMFP marks the byte after J1 of the first frame in a tributary multiframe of each STS-1 stream. It is not necessary for GFP or GMFP to be present at every opportunity. Internal counters fly-wheel based on the most recent GFP and GMFP received. Transport overhead and payload bytes are distinguished by the GPL output which is set low to mark transport overhead bytes and set high to mark payload bytes. All three synchronous payload envelops are shown to have the same active offset in Figure 22 for illustration only; any combination of active offsets are possible. The tributary multiframe alignments of the three STS-1 streams are independent. The value on GD[1:0] reflect the different alignments. The GENERATED bus composite timing signal GC1J1V1 is set high when GPL is set low to mark the C1 byte. GC1J1V1 is set high when GPL is also set high to mark the J1 byte in each of the three STS-1 streams. Optionally, GC1J1V1 is set high once every multiframe to mark the first frame of the GENERATED bus tributary multiframe in each STS-1 stream. The GENERATED bus parity output GDP reports the parity of GD[1:0] and optionally includes GPL and GC1J1V1.

Figure 22 - STS-3 (STM1 - AU3) Mode GENERATED Bus Timing

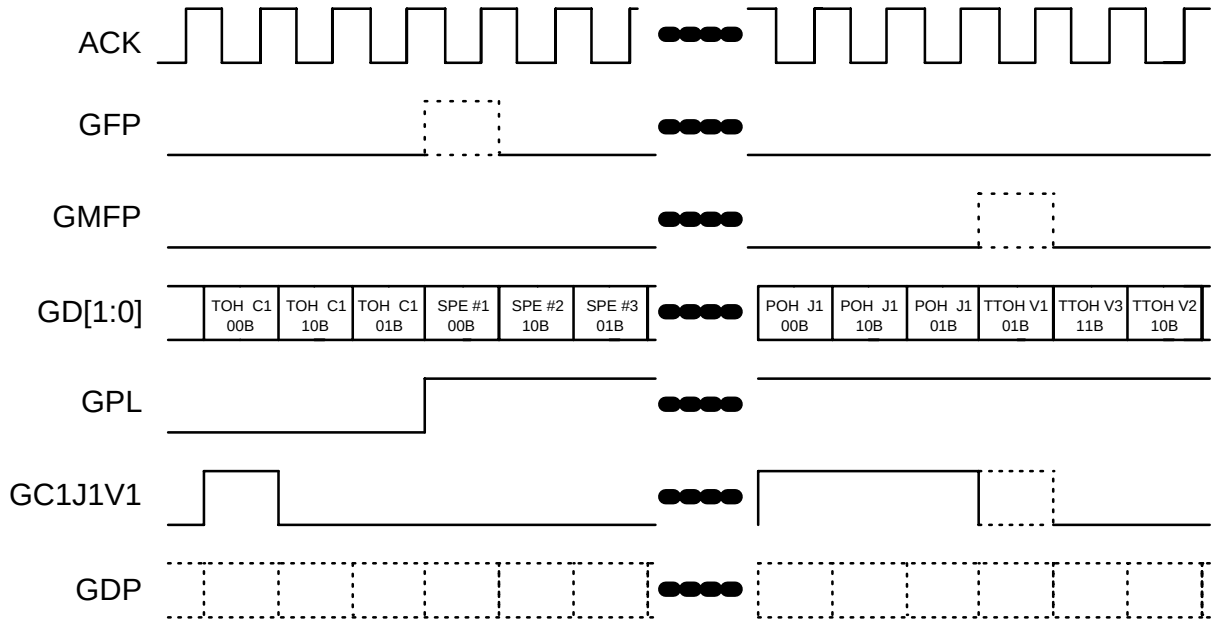
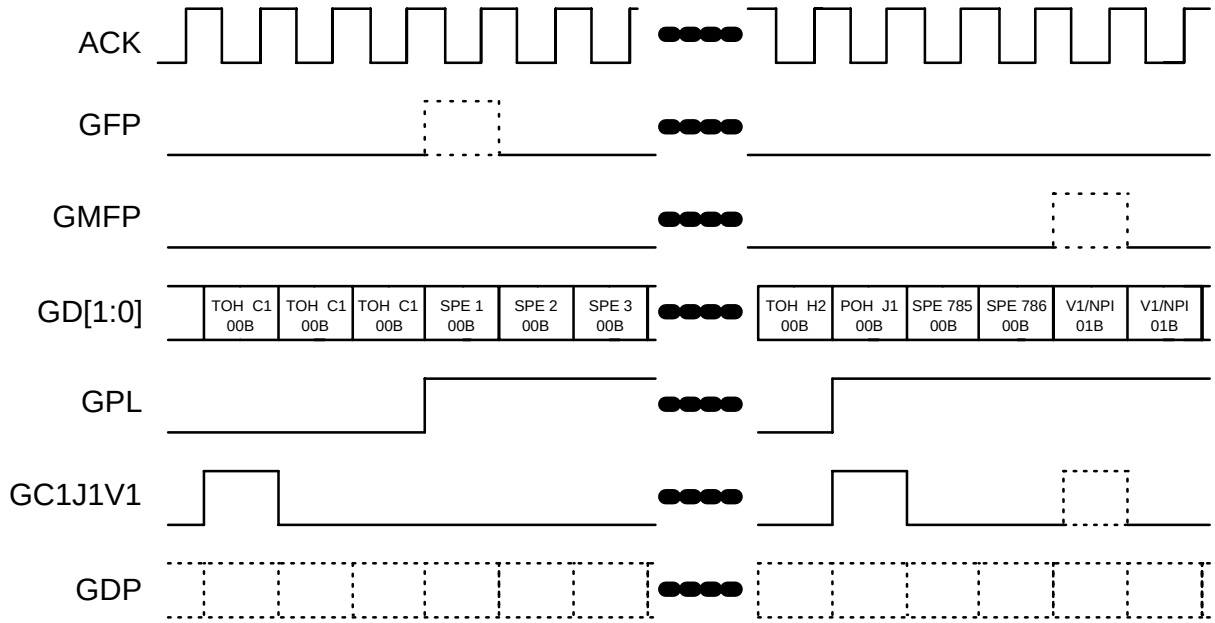


Figure 23 below shows the GENERATED bus timing in STS-3c mode. ACK is a 19.44 MHz clock. The frame pulse GFP marks the first synchronous payload envelope byte in the STS-3c frame on GD[1:0]. The tributary multiframe frame pulse GMFP marks three bytes after J1 of the first frame in a tributary multiframe on GD[1:0]. It is not necessary for GFP or GMFP to be present at every opportunity. Internal counters fly-wheel based on the most recent GFP and GMFP received. Transport overhead and payload bytes are distinguished by the GPL output which is set low to mark transport overhead bytes and set high to mark payload bytes. The GENERATED bus composite timing signal GC1J1V1 is set high when GPL is set low to mark the C1 byte. GC1J1V1 is set high when GPL is also set high to mark the J1 byte in each of the three STS-1 streams. Optionally, GC1J1V1 is set high once every multiframe to mark the first frame of the GENERATED bus tributary multiframe. When processing an STS-3c stream, the V1 pulse marks the V1 byte of the first tributary. When processing and STM1 stream carrying an AU4, the V1 pulse marks the more significant byte of the Null Pointer Indication (NPI) of the first frame in each tributary multiframe. A negative justification event (NJE) is shown in Figure 23. Prior to the NJE, the alignment of the transport frame and the synchronous payload envelope corresponds to an active offset of 0. After the event, the active offset will be 782. The active offsets shown are for illustration only; other alignments are possible. The GENERATED bus parity output GDP reports the parity of GD[1:0] and optionally includes GPL and GC1J1V1.

Figure 23 - STS-3c (STM1 - AU4) Mode GENERATED Bus Timing



13.2.2 ADD Bus Timing

Figure 24 below shows the ADD bus timing in STS-1 mode. ACK is a 6.48 MHz clock. Transport overhead and payload bytes are distinguished by the APL input which is set low to mark transport overhead bytes and set high to mark payload bytes. During a negative justification event (labelled NJE), APL is set high during the H3 byte to indicate that payload data is available. During a positive justification event (labelled PJE), APL is set low during the PSO byte to indicate that payload data is not available. The ADD bus composite timing signal AC1J1V1 is set high when APL is set low to mark the C1 byte. AC1J1V1 is set high when APL is also set high to mark the J1 byte. Optionally, AC1J1V1 is set high on the first payload byte after J1 once every multiframe to mark the first frame of the ADD bus tributary multiframe. The alignment of the transport frame and the synchronous payload envelope shown in Figure 24 corresponds to an active offset of 523 and is for illustration only. Other alignments are possible. The ADD bus parity input ADP carries the parity of AD[7:0] and optionally includes APL and AC1J1V1.

Figure 24 - STS-1 Mode ADD Bus Timing

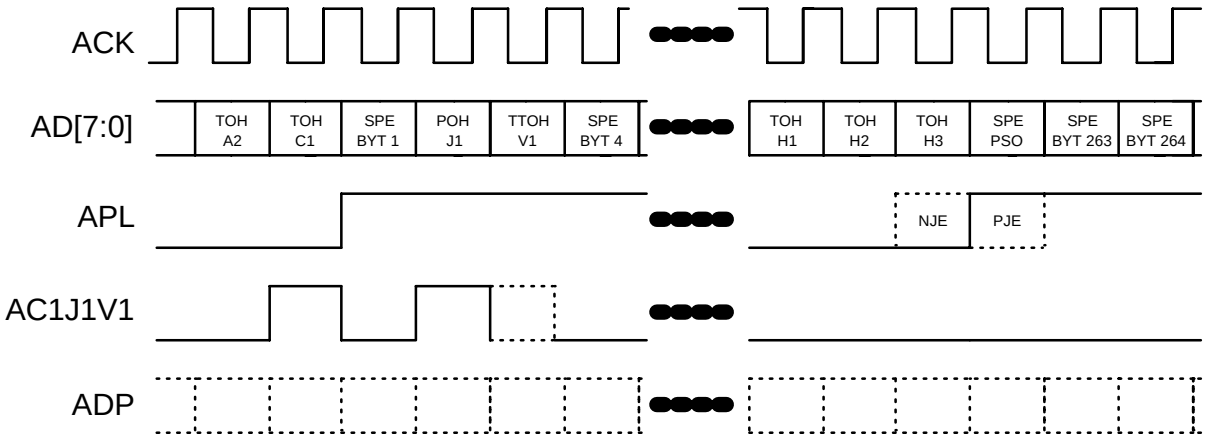


Figure 25 below shows the ADD bus timing in STS-3 mode. ACK is a 19.44 MHz clock. Transport overhead and payload bytes are distinguished by the APL input which is set low to mark transport overhead bytes and set high to mark payload bytes. A positive justification event is shown for STS-1 #3 in Figure 25. A stuff byte is place in the positive stuff opportunity byte and APL is set low to indicate that data is not available. The ADD bus composite timing signal AC1J1V1 is set high when APL is set low to mark the C1 byte. AC1J1V1 is set high when APL is also set high to mark the J1 byte in each of the three STS-1 streams. Optionally, AC1J1V1 is set high once every multiframe to mark the first frame of the ADD bus tributary multiframe in each STS-1 stream. The alignment of the transport frame and the synchronous payload envelope of STS-1 #1 shown in Figure 25 corresponds to an active offset of 0 and is for illustration only. Other alignments are possible. The ADD bus parity input ADP carries the parity of AD[7:0] and optionally includes APL and AC1J1V1.

Figure 25 - STS-3 (STM1 - AU3) Mode ADD Bus Timing

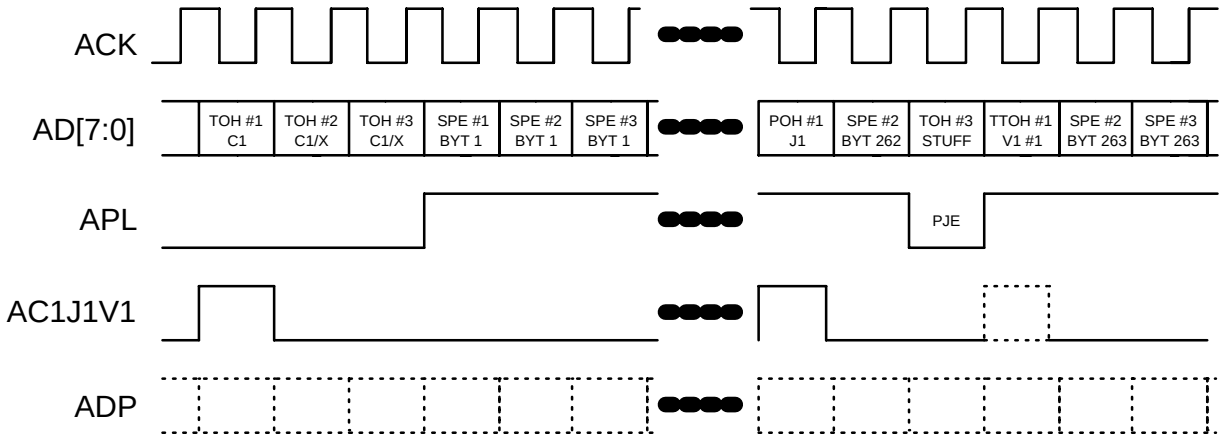
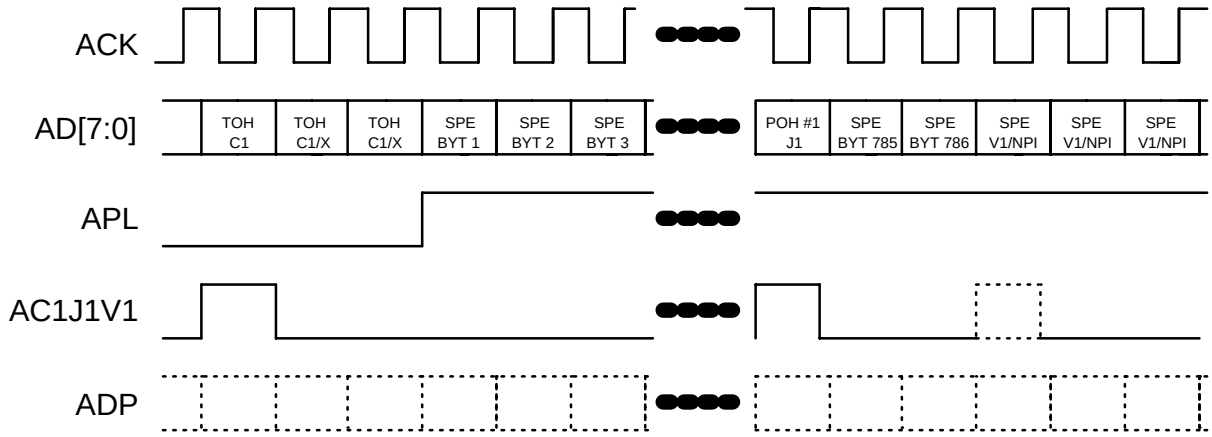


Figure 26 below shows the ADD bus timing in STS-3c mode. ACK is a 19.44 MHz clock. Transport overhead and payload bytes are distinguished by the APL input which is set low to mark transport overhead bytes and set high to mark payload bytes. The ADD bus composite timing signal AC1J1V1 is set high when APL is set low to mark the C1 byte. AC1J1V1 is set high when APL is also set high to mark the J1 byte in each of the three STS-1 streams. Optionally, AC1J1V1 is set high once every multiframe to mark the first frame of the ADD bus tributary multiframe. When processing an STS-3c stream, the V1 pulse marks the V1 byte of the first tributary. When processing and STM1 stream carrying an AU4, the V1 pulse marks the more significant byte of the Null Pointer Indication (NPI) of the first frame in each tributary multiframe. The alignment of the transport frame and the synchronous payload envelope of STS-3c stream shown in Figure 26 corresponds to an active offset of 0 and is for illustration only. Other alignments are possible. The ADD bus parity input ADP carries the parity of AD[7:0] and optionally includes APL and AC1J1V1.

Figure 26 - STS-3c (STM1 - AU4) Mode ADD Bus Timing



13.2.3 Transmit Low-Speed Interface Timing

Figure 27 below shows the insertion of the path overhead column into a low speed serial stream. TPOHCK[3:1] are nominally a 576 kHz clocks. The entire path overhead, except B3 and H4, (J1, C2, G1, F2, Z3, Z4, Z5 bytes) can be inserted into the transmit stream via TPOH[3:1] over a frame period. In each byte, the most significant bit is transmitted first. TPOHFP[3:1] mark the most significant bit of the J1 byte. TPOHEN[3:1] control the insertion of data on TPOH[3:1] on a bit-by-bit basis. The data on TPOH is inserted in the path overhead of the transmit stream if TPOH is set high at the corresponding bit position. In Figure 27, TPOHEN is set high during bits 1, 4 and 5 of the C2 byte and the entire G1 byte. For this sample configuration, the G1 byte and bits 1, 4 and 5 of the C2 byte will be taken from TPOH while the remaining bits (2, 3, 6, 7 and 8) retain their default values. The index in the signal names refer to the STS-1 stream number within the receive STS-3 stream. I.e., signals carrying an index of 1 are associated with STS-1 #1, those with index of 2 with STS-1 #2, and those with index of 3 with STS-1 #3. In STS-1 or STS-3c mode, only TPOHCK[1], TPOH[1], TPOHFP[1] and TPOHEN[1] are active. The remaining outputs are set low and inputs are ignored.

An error insertion feature is provided for the B3 byte. When TPOHEN and TPOH are both set high, the corresponding path BIP bit will be inverted before insertion in the transmit stream. The H4 byte cannot be manipulated by TPOH.

Figure 27 - Transmit Path Overhead Insertion Timing

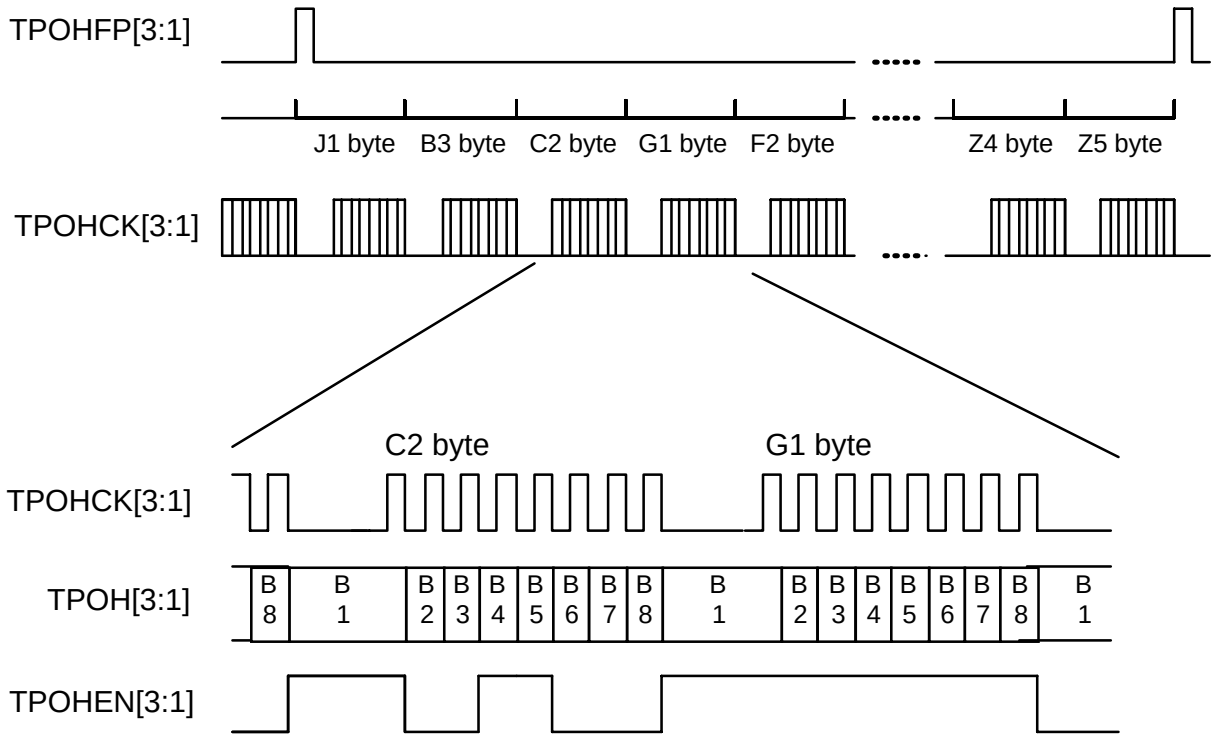
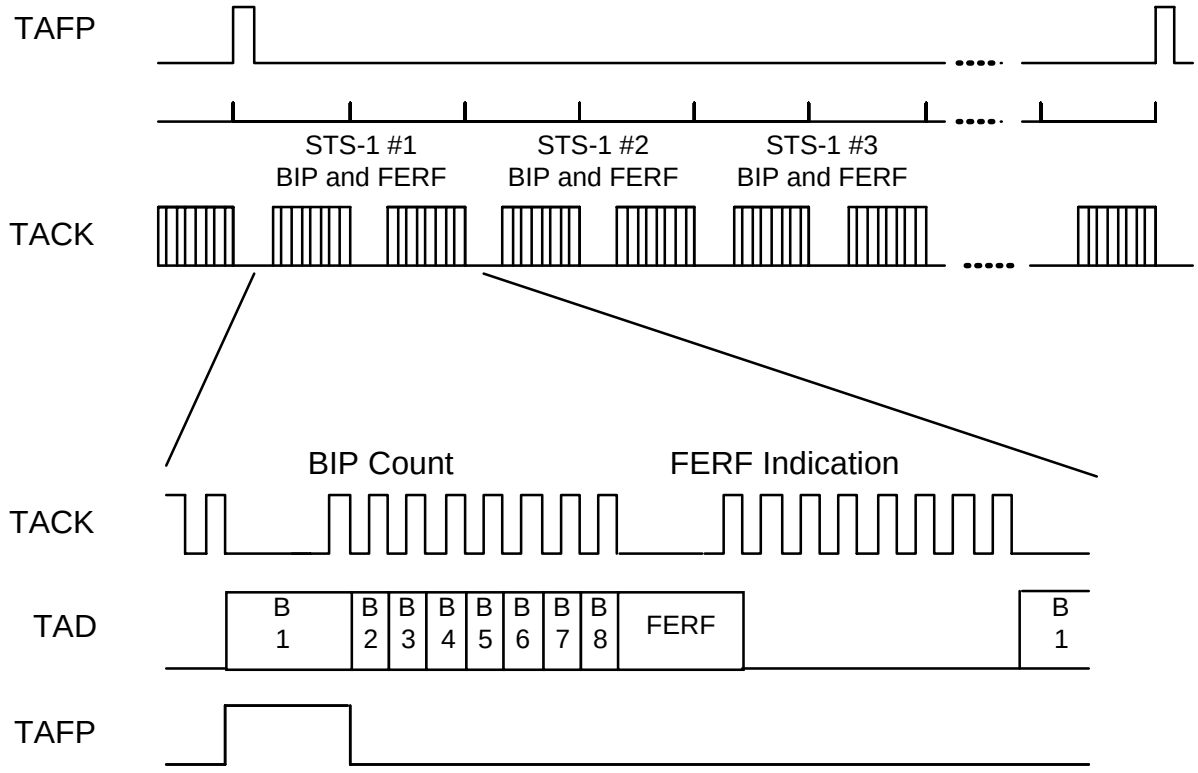


Figure 28 below shows the format of the transmit alarm port. The path FEBE counts from all three STS-1 streams are serialized in the transmit alarm data input (TAD) and clocked in by TACK. The eight BIP count bit positions for each STS-1 are left justified. If there are eight BIP errors in the corresponding STS-1 stream, all bit positions are set high. If there are fewer BIP errors, only the first N positions corresponding to the number of detected errors are set high, the remainder are set low. The FERF bit is set high when the corresponding STS-1 stream in the peer receive section inserts path AIS in the DROP bus. In STS-1 or STS-3c mode, only the bit positions assigned to STS-1 #1 are active, those assigned to streams #2, and #3 are ignored.

Figure 28 - Transmit Alarm Port Timing



13.2.4 TRANSMIT Bus Timing

Figure 29 below shows the TRANSMIT bus timing in STS-1 mode. TCK is a 6.48 MHz clock. The frame pulse TFP marks the first synchronous payload envelope byte in the STS-1 frame on TD[7:0]. It is not necessary for TFP to be present at every frame. An internal counter fly-wheels based on the most recent TFP received. Transport overhead and payload bytes are distinguished by the TPL output which is set low to mark transport overhead bytes and set high to mark payload bytes. During a negative justification event (labelled NJE), TPL is set high during the H3 byte to indicate that payload data is available. During a positive justification event (labelled PJE), TPL is set low during the PSO byte to indicate that payload data is not available. The TRANSMIT bus composite timing signal TC1J1V1 is set high when TPL is set low to mark the C1 byte. TC1J1V1 is set high when TPL is also set high to mark the J1 byte. Optionally, TC1J1V1 is set high on the first payload byte after J1 once every multiframe to mark the first frame of the TRANSMIT bus tributary multiframe. The frame pulse output FPOUT marks the first SPE byte of the STS-1 stream on the TRANSMIT bus. It may be connected to the TFP input of slave SPTX devices to synchronize them

to a common frame alignment. The alignment of the transport frame and the synchronous payload envelope shown in Figure 29 corresponds to an active offset of 523 and is for illustration only. Other alignments are possible. The TRANSMIT bus parity output TDP reports the parity of TD[7:0] and optionally includes TPL and TC1J1V1.

Figure 29 - STS-1 Mode TRANSMIT Bus Timing

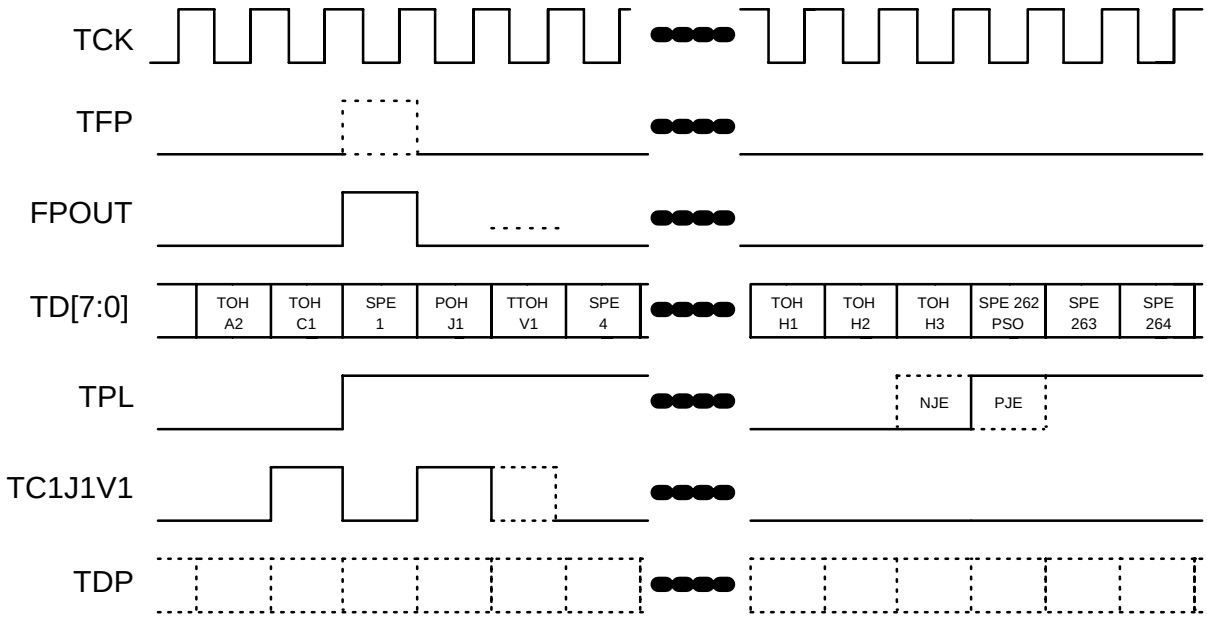


Figure 30 below shows the TRANSMIT bus timing in STS-3 mode. TCK is a 19.44 MHz clock. The frame pulse TFP marks the first synchronous payload envelope byte in the STS-3 frame on TD[7:0]. It is not necessary for TFP to be present at every frame. An internal counter fly-wheels based on the most recent TFP received. Transport overhead and payload bytes are distinguished by the TPL output which is set low to mark transport overhead bytes and set high to mark payload bytes. All three synchronous payload envelops are shown to have the same active offset in Figure 30 for illustration only; any combination of active offsets are possible. The tributary multiframe alignments of the three STS-1 streams are independent. The TRANSMIT bus composite timing signal TC1J1V1 is set high when TPL is set low to mark the C1 byte. TC1J1V1 is set high when TPL is also set high to mark the J1 byte in each of the three STS-1 streams. Optionally, TC1J1V1 is set high once every multiframe to mark the first frame of the TRANSMIT bus tributary multiframe in each STS-1 stream. The frame pulse output FPOUT marks the first SPE byte of the STS-3 stream on the TRANSMIT bus. It may be connected to the TFP input of slave SPTX devices to synchronize

them to a common frame alignment. The TRANSMIT bus parity output TDP reports the parity of TD[7:0] and optionally includes TPL and TC1J1V1.

Figure 30 - STS-3 (STM1 - AU3) Mode TRANSMIT Bus Timing

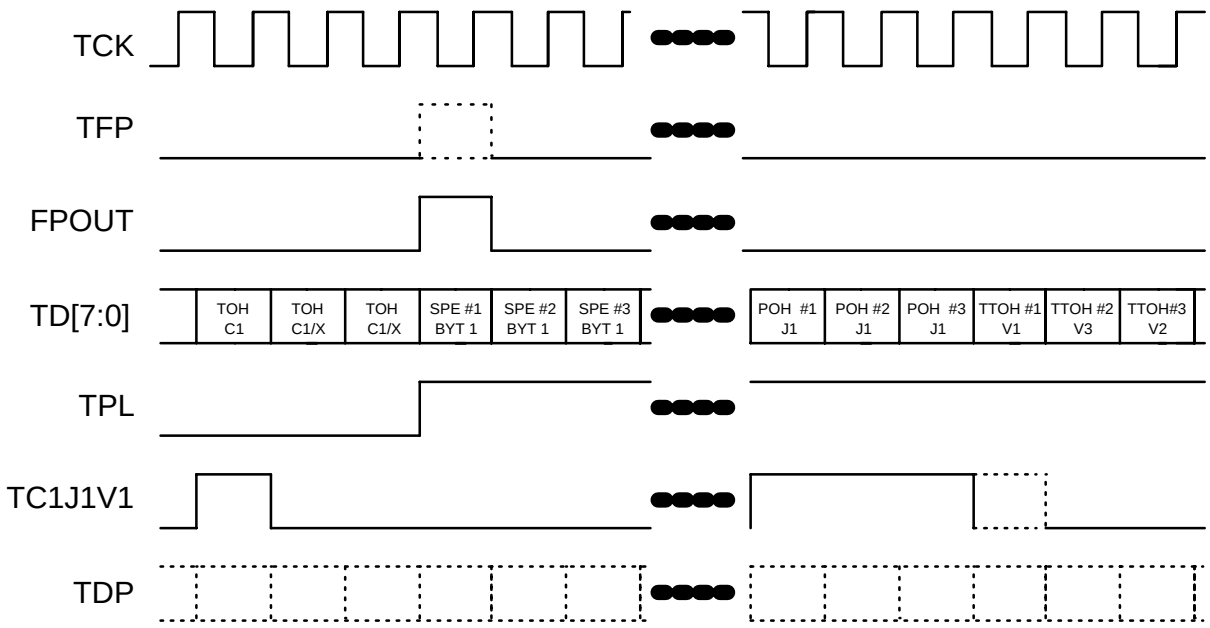
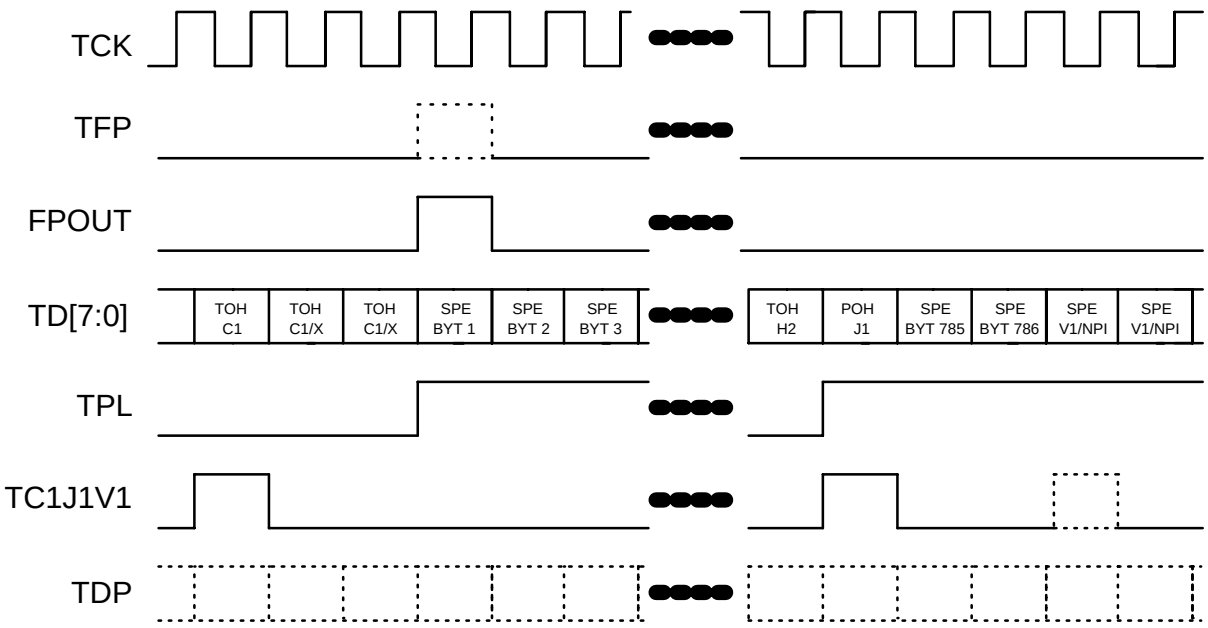


Figure 31 below shows the TRANSMIT bus timing in STS-3c mode. TCK is a 19.44 MHz clock. The frame pulse TFP marks the first synchronous payload envelope byte on TD[7:0]. It is not necessary for TFP to be present at every frame. An internal counter fly-wheels based on the most recent TFP received. Transport overhead and payload bytes are distinguished by the TPL output which is set low to mark transport overhead bytes and set high to mark payload bytes. The TRANSMIT bus composite timing signal TC1J1V1 is set high when TPL is set low to mark the C1 byte. TC1J1V1 is set high when TPL is also set high to mark the J1 byte in each of the three STS-1 streams. Optionally, TC1J1V1 is set high once every multiframe to mark the first frame of the TRANSMIT bus tributary multiframe. When processing an STS-3c stream, the V1 pulse marks the V1 byte of the first tributary. When processing and STM1 stream carrying an AU4, the V1 pulse marks the more significant byte of the Null Pointer Indication (NPI) of the first frame in each tributary multiframe. A negative justification event (NJE) is shown in Figure 31. Prior to the NJE, the alignment of the transport frame and the synchronous payload envelope corresponds to an active offset of 0. After the event, the active offset will be 782. The frame pulse output FPOUT marks the first SPE byte of the STS-3c stream on the TRANSMIT bus. It may be connected to the TFP input of slave SPTX devices to synchronize them to a common frame alignment. The active offsets shown are for illustration only; other alignments are

possible. The TRANSMIT bus parity output TDP reports the parity of TD[7:0] and optionally includes TPL and TC1J1V1.

Figure 31 - STS-3c (STM1 - AU4) Mode TRANSMIT Bus Timing



13.2.5 Elastic Store Bypass Timing

Figure 32 below shows the timing relationship between the receive stream and the DROP bus in STS-1 mode when the elastic store in the Receive Telecombus Aligner block is bypassed. The DROP bus is synchronous to the receive stream. Signals normally timed relative to DCK are now timed to the receive clock PICLK.

Figure 32 - STS-1 (Single AU3) Receive Elastic Store Bypass Timing

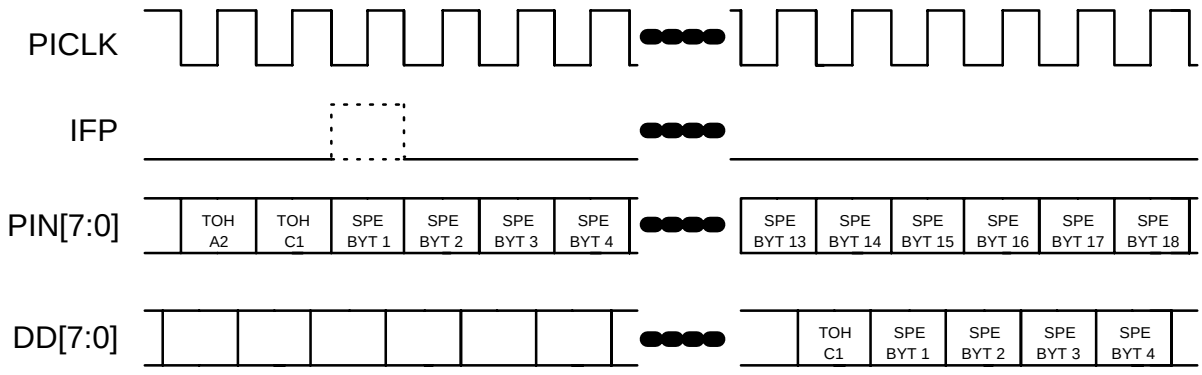


Figure 33 below shows the timing relationship between the receive stream and the DROP bus in STS-3 mode when the elastic store in the Receive Telecombus Aligner block is bypassed. The DROP bus is synchronous to the receive stream. Signals normally timed relative to DCK are now timed to the receive clock PICLK.

Figure 33 - STS-3 (STM1 - AU3) Receive Elastic Store Bypass Timing

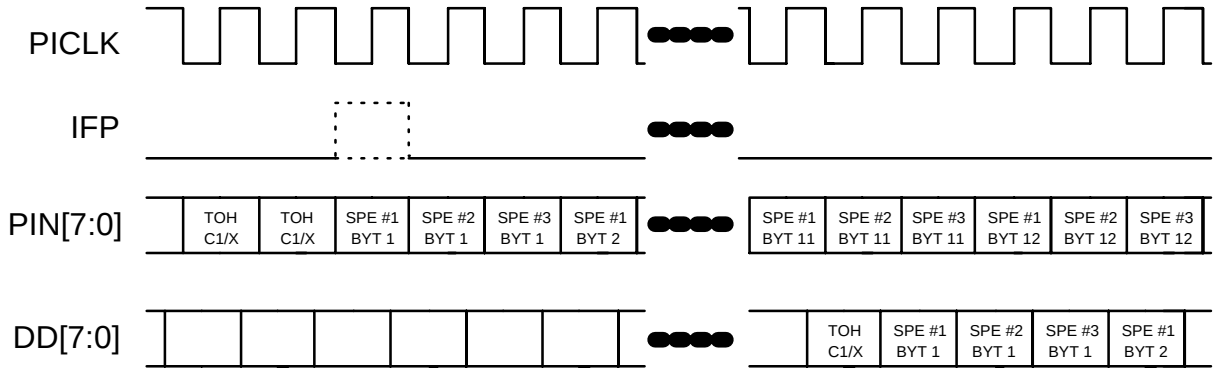


Figure 34 below shows the timing relationship between the receive stream and the DROP bus in STS-3c mode when the elastic store in the Receive Telecombus Aligner block is bypassed. The DROP bus is synchronous to the receive stream. Signals normally timed relative to DCK are now timed to the receive clock PICLK.

Figure 34 - STS-3c (STM1 - AU4) Receive Elastic Store Bypass Timing

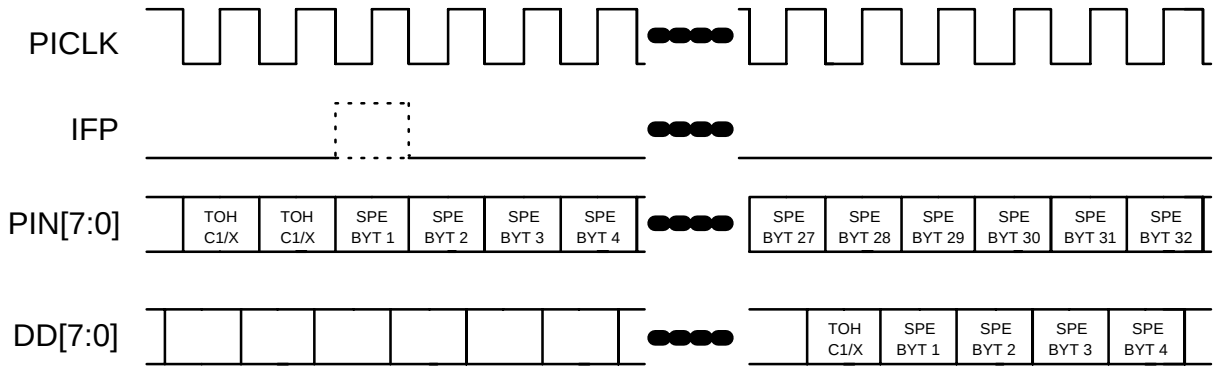


Figure 35 below shows the timing relationship between the transmit stream and the ADD bus in STS-1 mode when the elastic store in the Transmit Telecombus Aligner block is bypassed. The transmit stream is synchronous to the ADD bus. Signals normally timed relative to TCK are now timed to the receive clock ACK.

Figure 35 - STS-1 (Single AU3) Transmit Elastic Store Bypass Timing

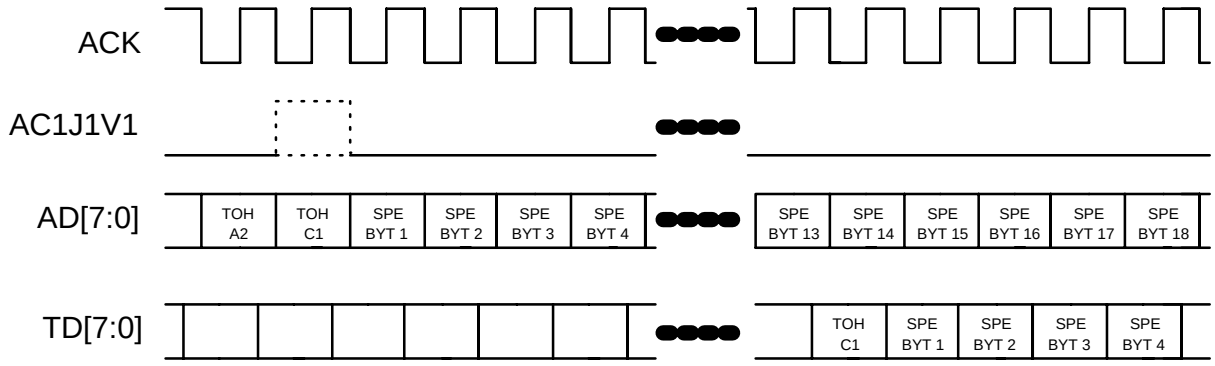


Figure 36 below shows the timing relationship between the transmit stream and the ADD bus in STS-3 mode when the elastic store in the Transmit Telecombus Aligner block is bypassed. The transmit stream is synchronous to the ADD bus. Signals normally timed relative to TCK are now timed to the receive clock ACK.

Figure 36 - STS-3 (STM1 - AU3) Transmit Elastic Store Bypass Timing

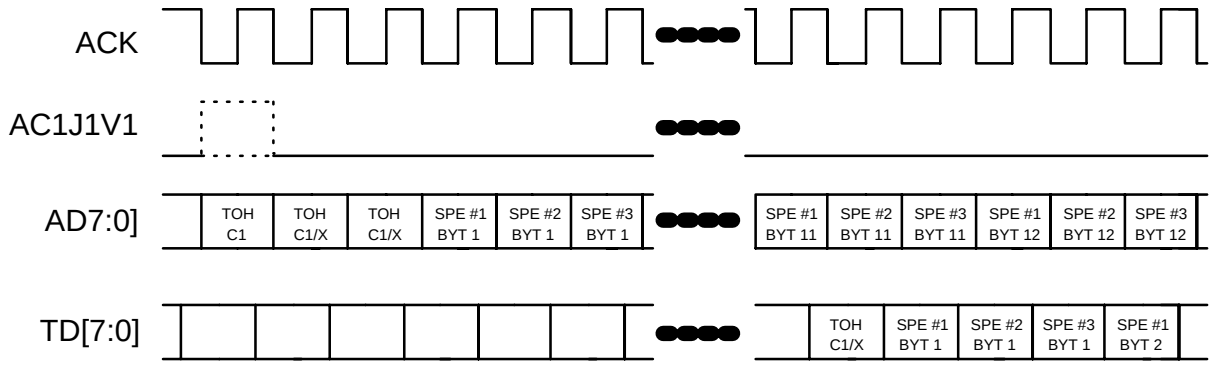
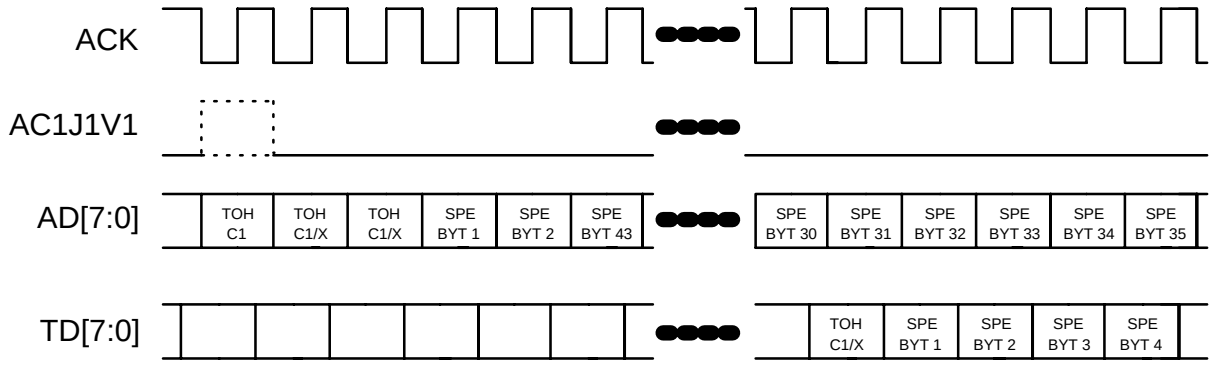


Figure 37 below shows the timing relationship between the transmit stream and the ADD bus in STS-3c mode when the elastic store in the Transmit Telecombus Aligner block is bypassed. The transmit stream is synchronous to the ADD bus. Signals normally timed relative to TCK are now timed to the receive clock ACK.

Figure 37 - STS-3c (STM1 - AU4) Transmit Elastic Store Bypass Timing



14 ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias 40°C to +85°C

Storage Temperature -40°C to +125°C

Supply Voltage -0.5V to +6.0V

Voltage on Any Pin 0.5V to V_{DD}+0.5V

Static Discharge Voltage ±500 V

Latch-Up Current ±100 mA

DC Input Current ±20 mA

Lead Temperature +300°C

Absolute Maximum Junction Temperature +150°C

Power Dissipation 1.5 W

15 D.C. CHARACTERISTICS

(T_A = -40°C to +85°C, V_{DD} = 5 V ±10%)

Table 7 - D.C. Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{IL}	Input Low Voltage	-0.5		0.8	Volts	Guaranteed Input LOW Voltage
V_{IH}	Input High Voltage	2.0		V_{DD} +0.5	Volts	Guaranteed Input HIGH Voltage
V_{OL}	Output or Bidirectional Low Voltage			0.4	Volts	V_{DD} = min, I_{OL} = 4 mA for D[7:0] and INTB, and 2 mA for all others, Note 3
V_{OH}	Output or Bidirectional High Voltage	2.4			Volts	V_{DD} = min, I_{OH} = 4 mA for D[7:0] and 2 mA for all others, Note 3
V_{T+}	Reset Input High Voltage	3.5			Volts	
V_{T-}	Reset Input Low Voltage			.8	Volts	
V_{TH}	Reset Input Hysteresis Voltage		.5		Volts	
I_{ILPU}	Input Low Current	+20		+200	µA	V_{IL} = GND, Notes 1, 3
I_{IHPU}	Input High Current	-10		+10	µA	V_{IH} = V_{DD}, Notes 1, 3
I_{ILPD}	Input Low Current	-10		+10	µA	V_{IL} = GND, Notes 4, 3
I_{IHPD}	Input High Current	-200		-20	µA	V_{IH} = V_{DD}, Notes 4, 3
I_{IL}	Input Low Current	-10		+10	µA	V_{IL} = GND, Notes 2, 3

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input High Current	-10		+10	µA	$V_{IH} = V_{DD}$, Notes 2, 3
C_{IN}	Input Capacitance		5		pF	Excluding Package, Package Typically 2 pF
C_{OUT}	Output Capacitance		5		pF	Excluding Package, Package Typically 2 pF
C_{IO}	Bidirectional Capacitance		5		pF	Excluding Package, Package Typically 2 pF
I_{DDOP1}	Operating Current Processing STS-1 Streams			36	mA	V_{DD} = 5.5 V, Outputs Unloaded, TCLK = 6.48 MHz, PICLK = 6.48 MHz, ACK = 6.48 MHz, DCK = 6.48 MHz
I_{DDOP3}	Operating Current Processing STS-3 Streams			55	mA	V_{DD} = 5.5 V, Outputs Unloaded, TCLK = 19.44 MHz, PICLK = 19.44 MHz, ACK = 19.44 MHz, DCK = 19.44 MHz
I_{DDOP3c}	Operating Current Processing STS-3c Streams			83	mA	V_{DD} = 5.5 V, Outputs Unloaded, TCLK = 19.44 MHz, PICLK = 19.44 MHz, ACK = 19.44 MHz DCK = 19.44 MHz

Notes on D.C. Characteristics:

1. Input pin or bidirectional pin with internal pull-up resistor.

2. Input pin or bidirectional pin without internal pull-up resistor

3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).

4. Input pin or bidirectional pin with internal pull-down resistor.

16 MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

(T_A = -40°C to +85°C, V_{DD} = 5 V ±10%)

Table 8 - Microprocessor Interface Read Access (Figure 38, Figure 39)

Symbol	Parameter	Min	Max	Units
tS_{AR}	Address to Valid Read Set-up Time	25		ns
tH_{AR}	Address to Valid Read Hold Time	20		ns
tS_{RWB}	RWB to Valid Read Set-up Time	25		ns
tH_{RWB}	RWB to Valid Read Hold Time	20		ns
tS_{ALR}	Address to Latch Set-up Time	20		ns
tH_{ALR}	Address to Latch Hold Time	20		ns
tV_{L}	Valid Latch Pulse Width	20		ns
tS_{LR}	Latch to Read Set-up	0		ns
tH_{LR}	Latch to Read Hold	20		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		80	ns
tZ_{RD}	Valid Read Negated to Output Tri-state		20	ns
tZ_{INTH}	Valid Read Negated to Output Tri-state		50	ns

Figure 38 - Microprocessor Interface Read Timing (Intel Mode)

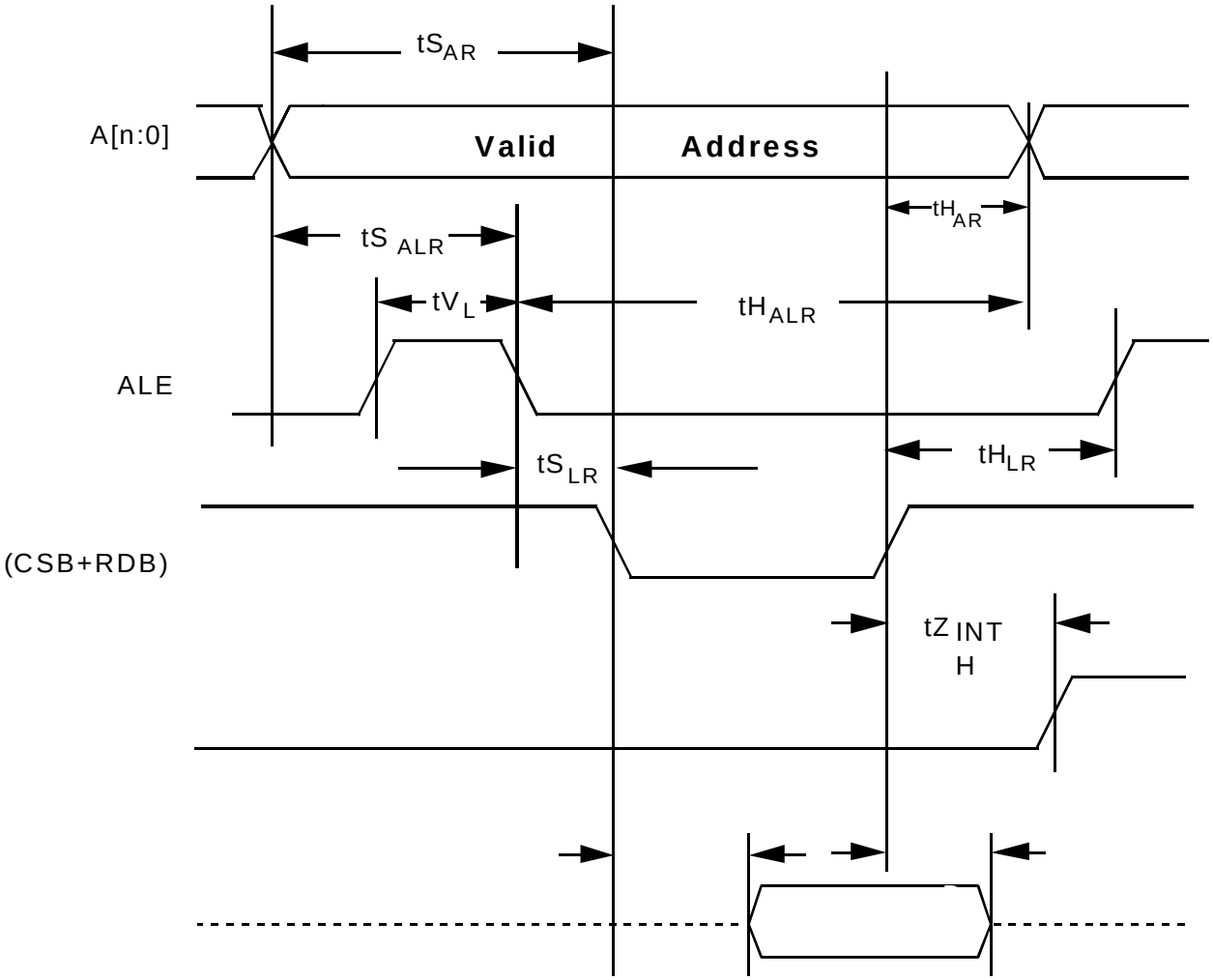
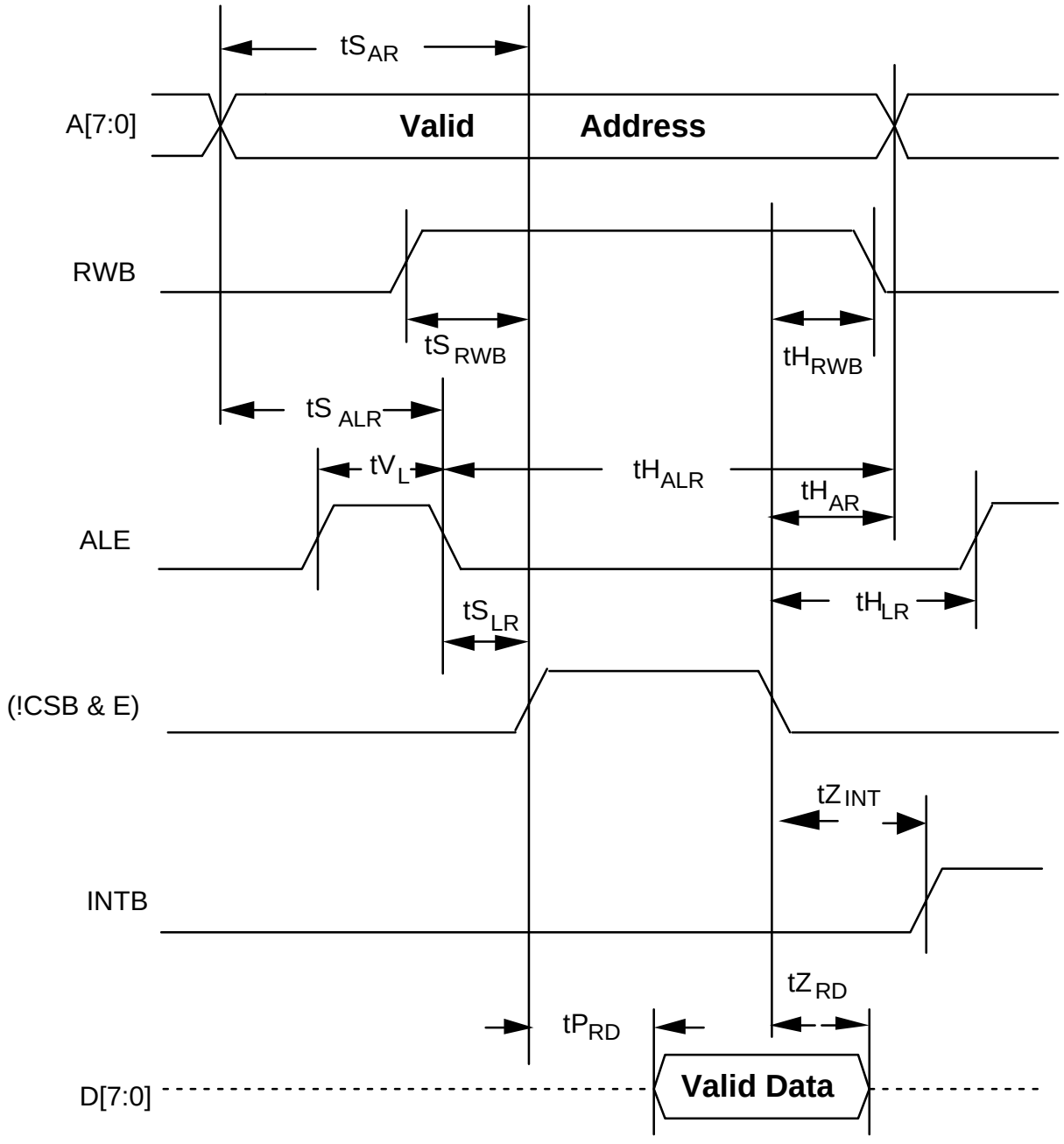


Figure 39 - Microprocessor Interface Read Timing (Motorola Mode)



Notes on Microprocessor Interface Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[7:0]).

3. In Intel mode, a valid read cycle is defined as a logical OR of the CSB and the RDB signals.

   In Motorola mode, a valid read cycle is defined as a logical AND of the E signal, the RDB signals and the inverted CSB signal.

4. Microprocessor Interface timing applies to normal mode register accesses only.

5. In non-multiplexed address/data bus architectures, ALE should be held high, parameters tS_{ALR}, tH_{ALR}, tV_L, and tS_{LR} are not applicable.

6. Parameters tH_{AR} and tS_{AR} are not applicable if address latching is used.

7. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

8. When a hold time is specified between an input and a clock, the hold time is the in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Table 9 - Microprocessor Interface Write Access (Figure 40, Figure 41)

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	25		ns
tS_{DW}	Data to Valid Write Set-up Time	20		ns
tS_{ALW}	Address to Latch Set-up Time	20		ns
tH_{ALW}	Address to Latch Hold Time	20		ns
tV_L	Valid Latch Pulse Width	20		ns
tS_{LW}	Latch to Write Set-up	0		ns
tH_{LW}	Latch to Write Hold	20		ns
tH_{DW}	Data to Valid Write Hold Time	20		ns
tH_{AW}	Address to Valid Write Hold Time	20		ns
tV_{WR}	Valid Write Pulse Width	40		ns

Symbol	Parameter	Min	Max	Units
tS_{RWB}	RWB to Write Set-up Time	25		ns
tH_{LW}	RWB to Write Hold Time	20		ns

Figure 40 - Microprocessor Interface Write Timing (Intel Mode)

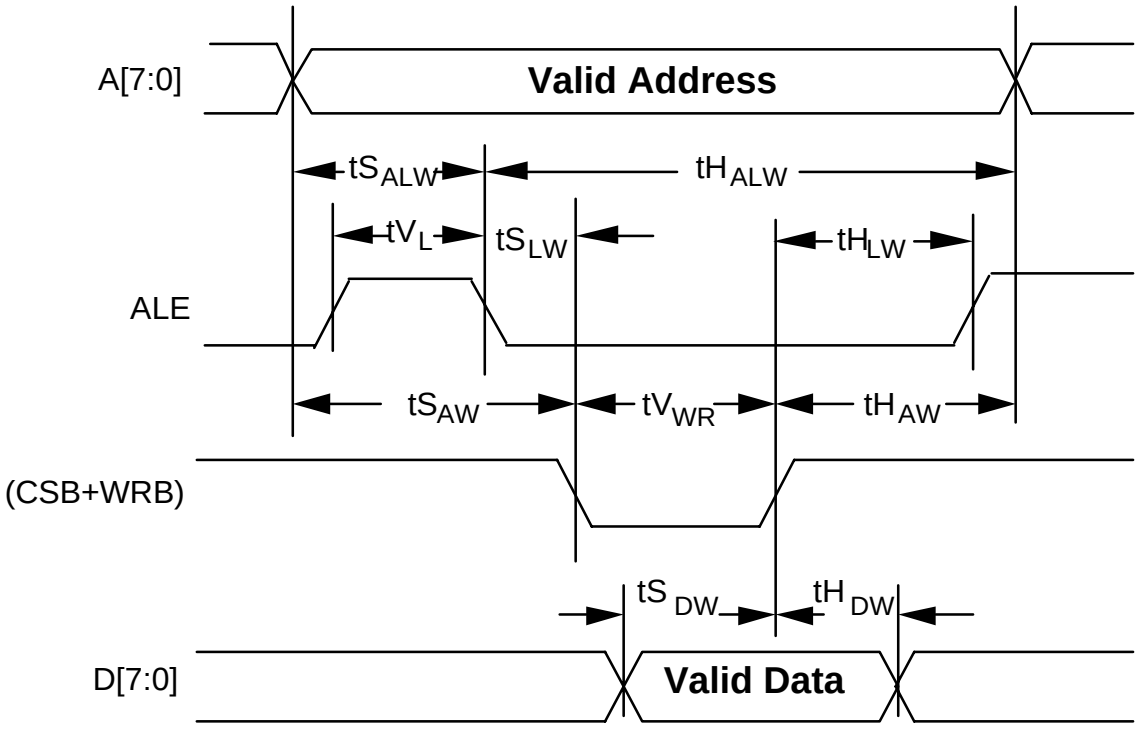
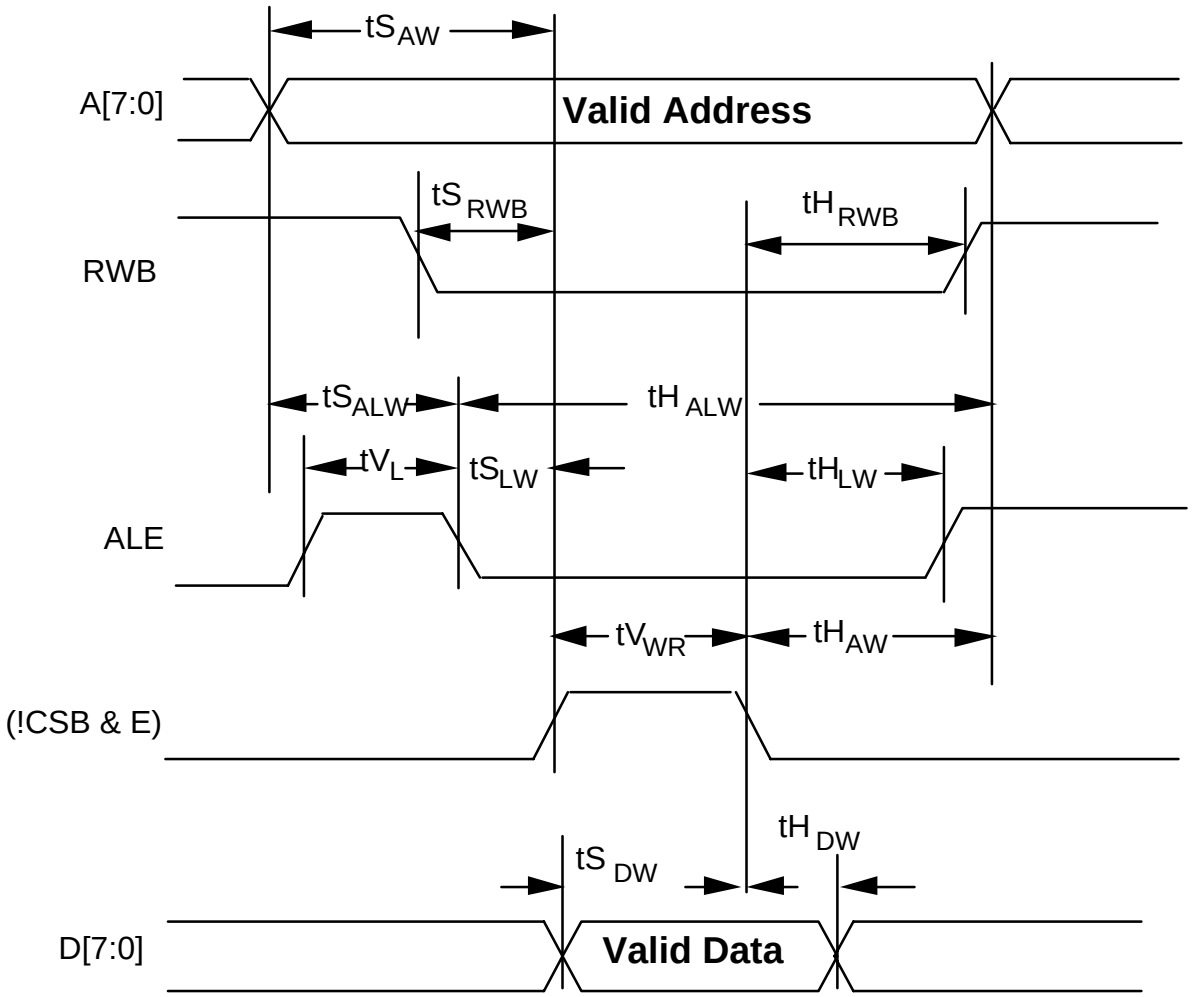


Figure 41 - Microprocessor Interface Write Timing (Motorola Mode)



Notes on Microprocessor Interface Write Timing:

1. In Intel mode, a valid write cycle is defined as a logical OR of the CSB and the WRB signals.

   In Motorola mode, a valid write cycle is defined as a logical AND of the E signal, the inverted WRB signal and the inverted CSB signal.

2. Microprocessor Interface timing applies to normal mode register accesses only.

3. In non-multiplexed address/data bus architectures, ALE should be held high, parameters tS_{ALW}, tH_{ALW}, tV_L, and tS_{LW} are not applicable.

4. Parameters tH_{AW} and tS_{AW} are not applicable if address latching is used.

5. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

17 SPTX TIMING CHARACTERISTICS

(T_A = -40°C to +85°C, V_{DD} = 5 V ±10%)

Table 10 - Receive Line Input Timing (Figure 42)

Symbol	Parameter	Min	Max	Units
	PICLK and RCK Freq. (Nominally 19.44MHz)		20	MHz
	PICLK and RCK Freq. (Nominally 6.48MHz)		7	MHz
	PICLK and RCK Duty Cycle	40	60	%
tS_{PIN}	PIN[7:0] and RD[7:0] Set-up Time	5		ns
tH_{PIN}	PIN[7:0] and RD[7:0] Hold Time	3		ns
tS_{IFP}	IFP and RC1J1V1 Set-up Time	5		ns
tH_{IFP}	IFP and RC1J1V1 Hold Time	3		ns
tS_{RPL}	RPL Set-up Time	5		ns
tH_{RPL}	RPL Hold Time	3		ns
tS_{RDP}	RDP Set-up Time	5		ns
tH_{RDP}	RDP Hold Time	3		ns

Figure 42 - Receive Line Input Timing

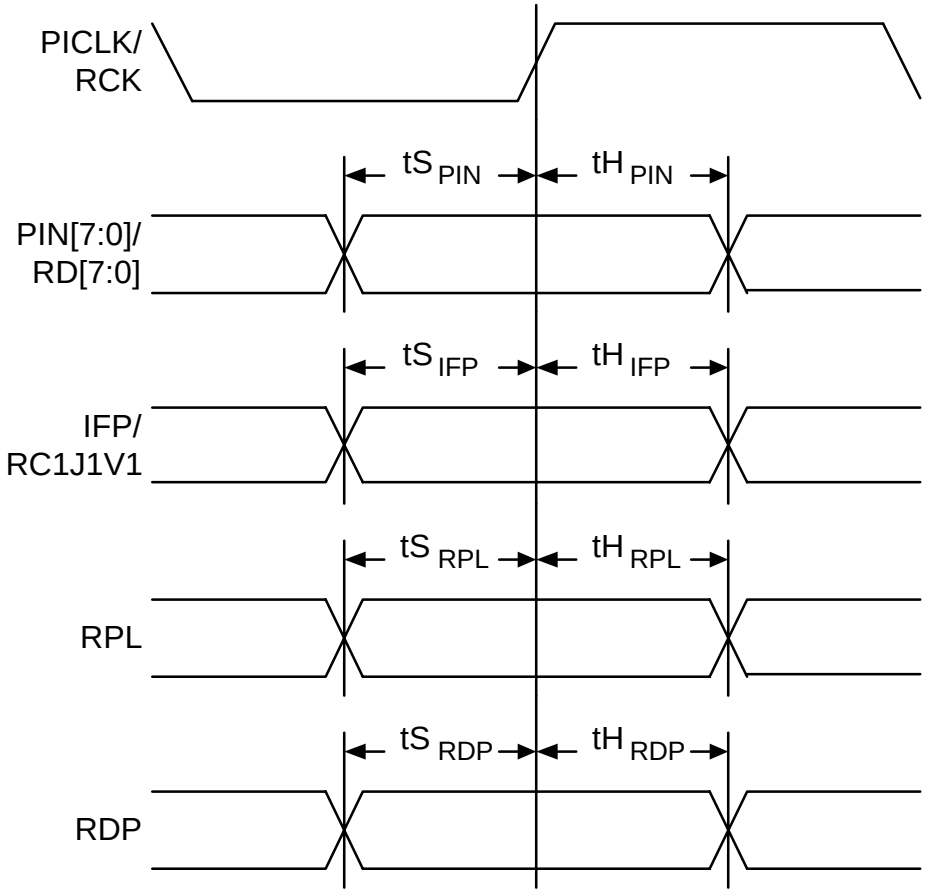


Table 11 - Receive Alarm Output Timing (Figure 43)

Symbol	Parameter	Min	Max	Units
tPLOP	PICLK High to LOP[3:1] Valid	5	40	ns
tPLOM	PICLK High to LOM[3:1] Valid	5	40	ns
tPPAIS	PICLK High to PAIS[3:1] Valid	5	40	ns
tPPFERF	PICLK High to PFERF[3:1] Valid	5	40	ns

Figure 43 - Receive Alarm Output Timing

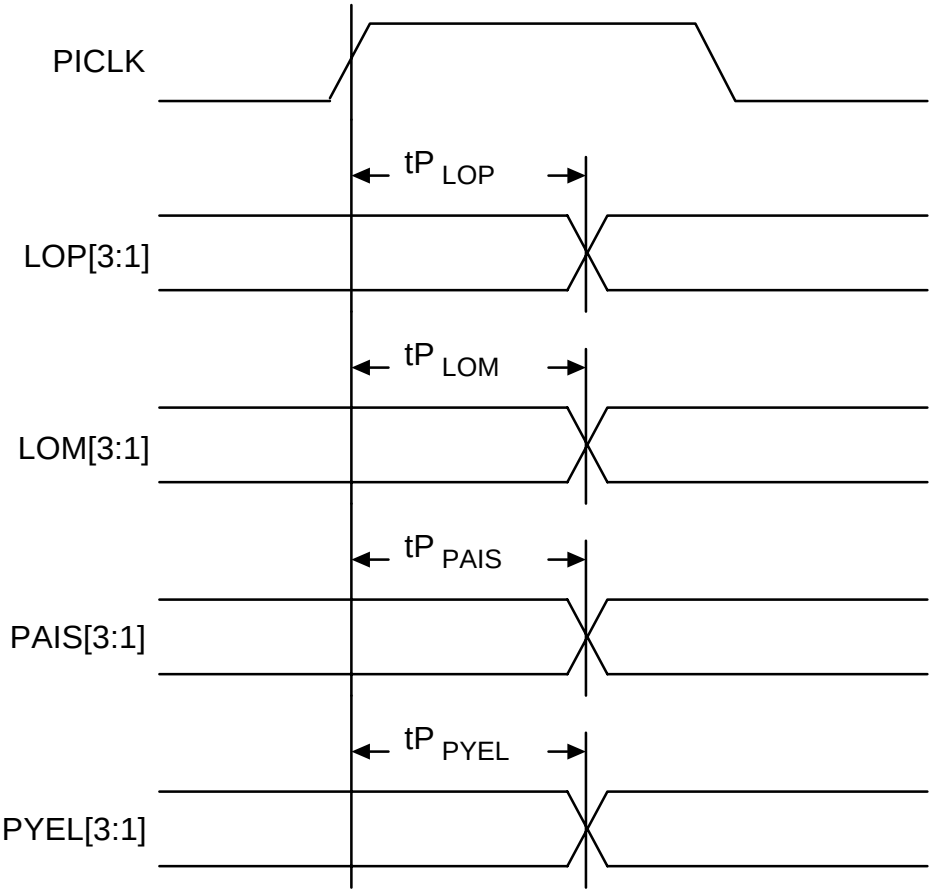


Table 12 - Receive Overhead and Alarm Port Output Timing (Figure 44)

Symbol	Parameter	Min	Max	Units
tP_{RPOHFP}	RPOHCK[3:1] Low to RPOHFP[3:1] Valid	-10	40	ns
tP_{RPOH}	RPOHCK[3:1] Low to RPOH[3:1] Valid	-10	40	ns
tP_{BIPE}	RPOHCK[3:1] Low to BIPE[3:1] Valid	-10	40	ns
tP_{RAD}	RPOHCK[3:1] Low to RAD Valid	-10	40	ns

Figure 44 - Receive Overhead and Alarm Port Output Timing

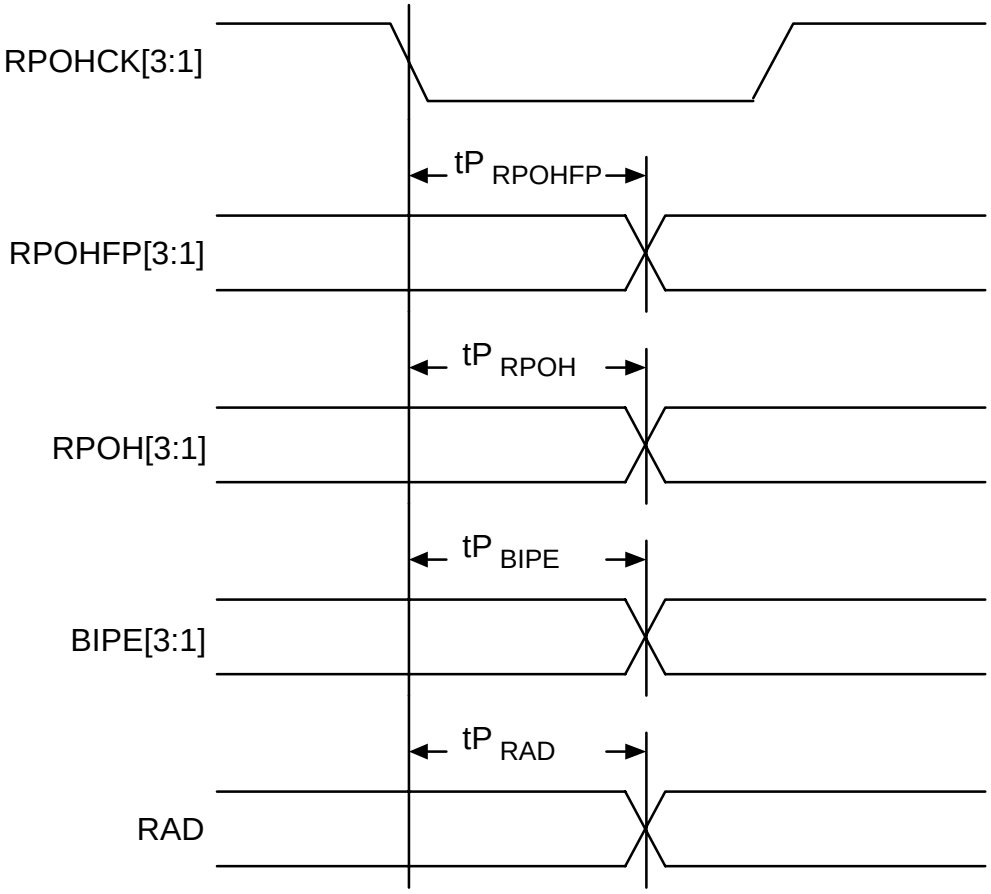


Table 13 - Receive Tandem Connection Input Timing (Figure 45)

Symbol	Parameter	Min	Max	Units
tS_{RTCEN}	RTCEN[3:1] Set-up Time	20		ns
tH_{RTCEN}	RTCEN[3:1] Hold Time	20		ns
tS_{RTCOH}	RTCOH[3:1] Set-up Time	20		ns
tH_{RTCOH}	RTCOH[3:1] Hold Time	20		ns

Figure 45 - Receive Tandem Connection Input Timing

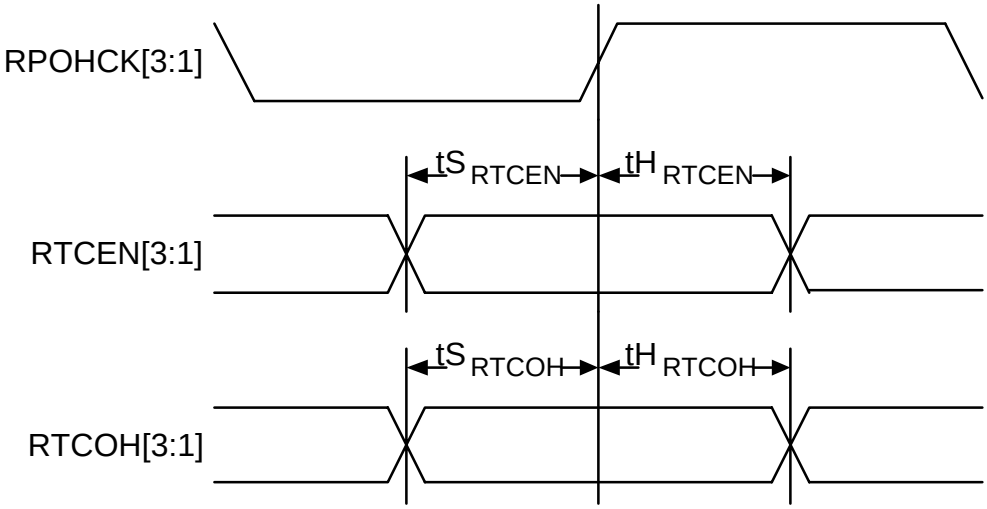


Table 14 - DROP BUS Input Timing (Figure 46)

Symbol	Parameter	Min	Max	Units
	DCK Freq. (Nominally 19.44MHz)		20	MHz
	DCK Freq. (Nominally 6.48MHz)		7	MHz
	DCK Duty Cycle	40	60	%
tS_{DFP}	DFP Set-up Time	5		ns
tH_{DFP}	DFP Hold Time	3		ns

Figure 46 - DROP Bus Input Timing

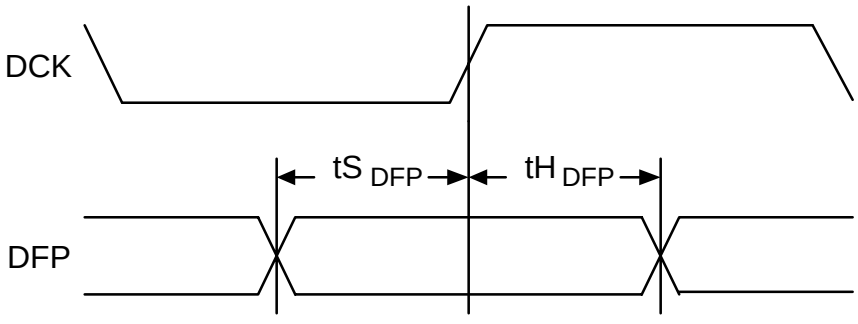


Table 15 - DROP Bus Output Timing (Figure 47)

Symbol	Parameter	Min	Max	Units
tP_{DD}	DCK High to DD[7:0] Valid	5	25	ns
tP_{DC1}	DCK High to DC1J1V1 Valid	5	25	ns
tP_{DPL}	DCK High to DPL Valid	5	25	ns
tP_{DDP}	DCK High to DDP Valid	5	25	ns

Figure 47 - DROP Bus Output Timing

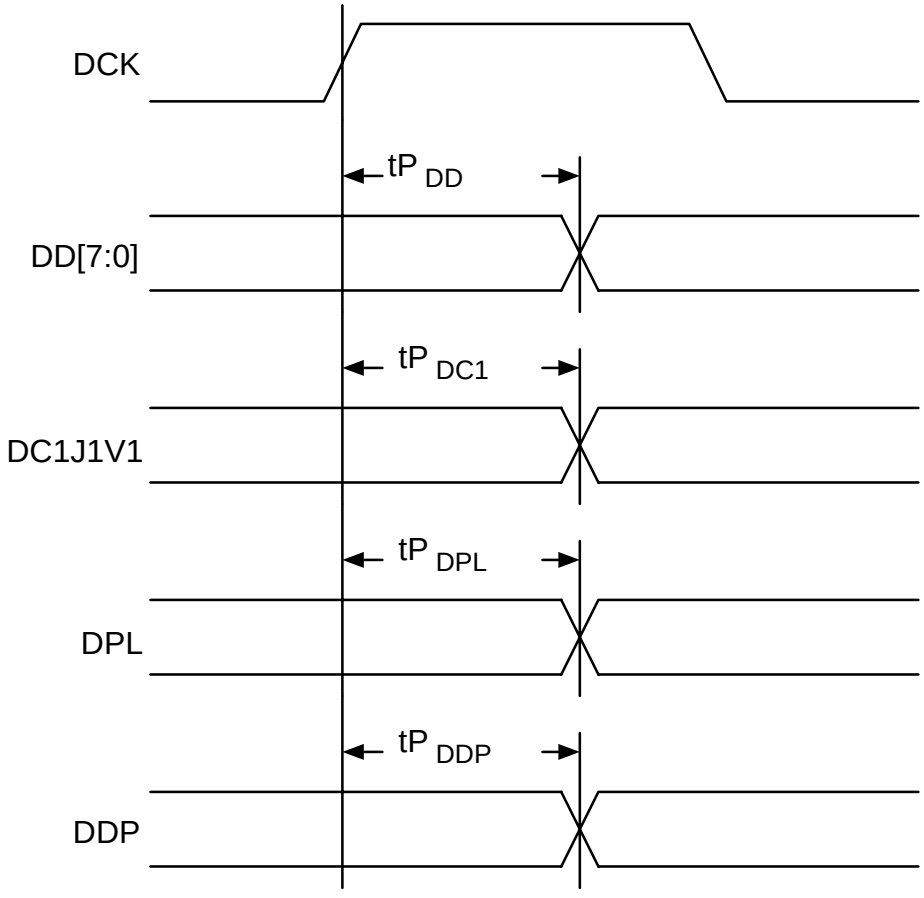


Table 16 - GENERATED BUS Input Timing (Figure 48)

Symbol	Parameter	Min	Max	Units
tS_{GFP}	GFP Set-up Time	5		ns
tH_{GFP}	GFP Hold Time	3		ns
tS_{GMFP}	GMFP Set-up Time	5		ns
tH_{GMFP}	GMFP Hold Time	3		ns

Figure 48 - GENERATED Bus Input Timing

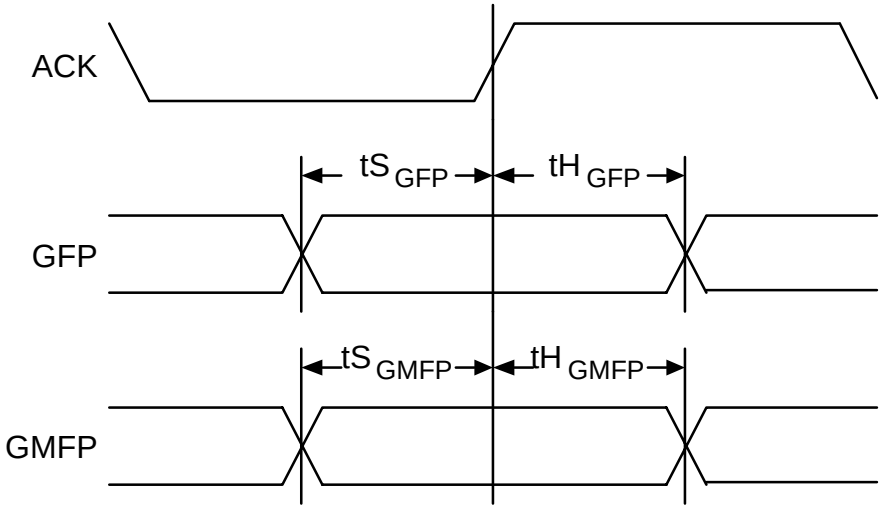


Table 17 - GENERATED Bus Output Timing (Figure 49)

Symbol	Parameter	Min	Max	Units
tP_{GD}	ACK High to GD[1:0] Valid	4	25	ns
tP_{GC1}	ACK High to GC1J1V1 Valid	4	25	ns
tP_{GPL}	ACK High to GPL Valid	4	25	ns
tP_{GDP}	ACK High to GDP Valid	4	25	ns

Figure 49 - GENERATED Bus Output Timing

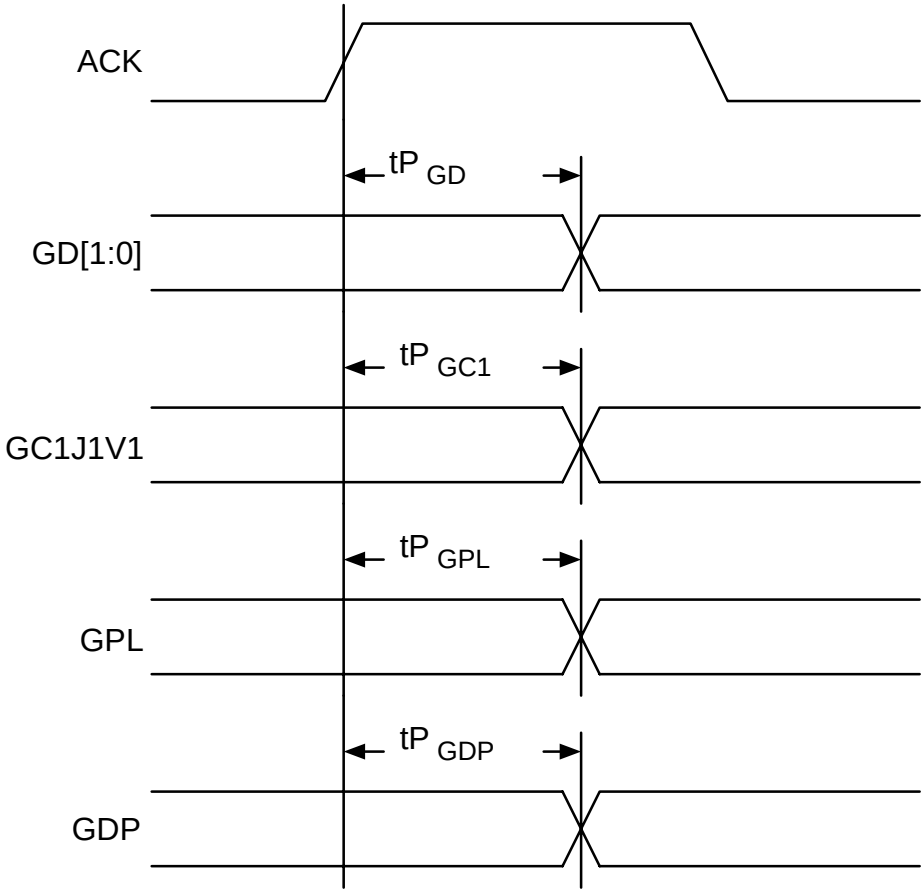


Table 18 - ADD BUS Input Timing (Figure 50)

Symbol	Parameter	Min	Max	Units
	ACK Freq. (Nominally 19.44MHz)		20	MHz
	ACK Freq. (Nominally 6.48MHz)		7	MHz
	ACK Duty Cycle	40	60	%
tS_{AD}	AD[7:0] and RD[7:0] Set-up Time	5		ns
tH_{AD}	AD[7:0] and RD[7:0] Hold Time	3		ns
tS_{AC1}	AC1J1V1 Set-up Time	5		ns
tH_{AC1}	AC1J1V1 Hold Time	3		ns

Symbol	Parameter	Min	Max	Units
tS_{APL}	APL Set-up Time	5		ns
tH_{APL}	APL Hold Time	3		ns
tS_{ADP}	ADP Set-up Time	5		ns
tH_{ADP}	ADP Hold Time	3		ns

Figure 50 - ADD Bus Input Timing

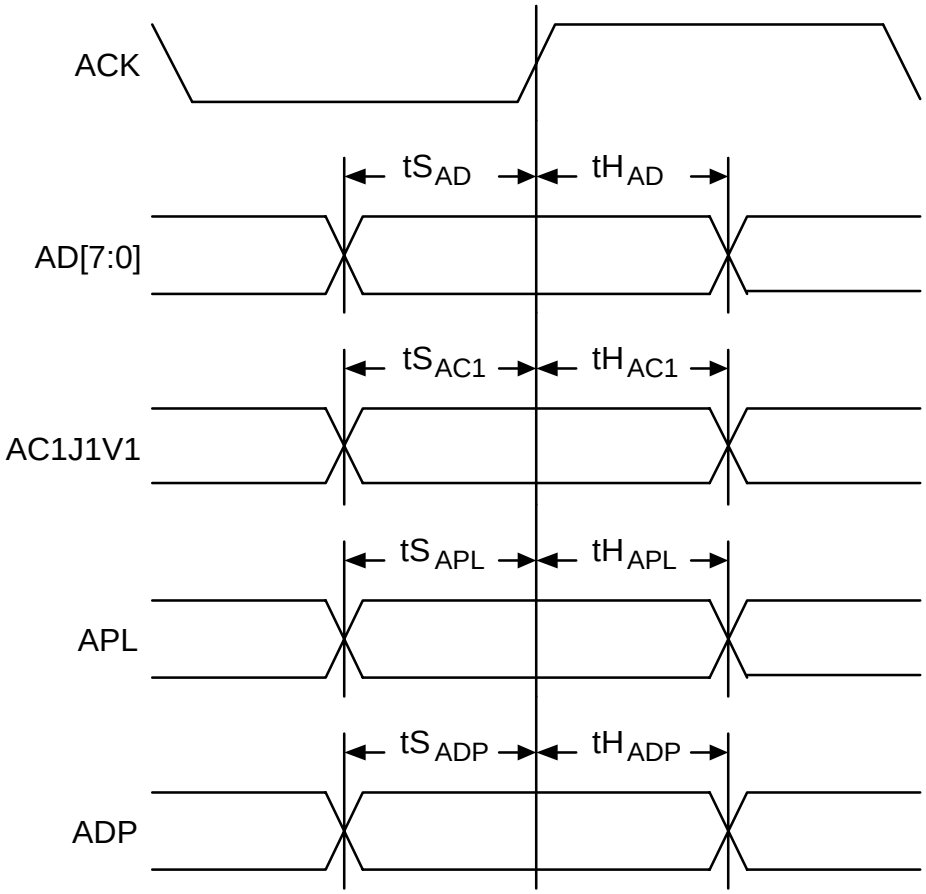


Table 19 - Transmit Overhead Input Timing (Figure 51)

Symbol	Parameter	Min	Max	Units
tS_{TPOH}	TPOH[3:1] Set-up Time	20		ns

Symbol	Parameter	Min	Max	Units
tH_{TPOH}	TPOH[3:1] Hold Time	20		ns
tS_{TPEN}	TPOHEN[3:1] Set-up Time	20		ns
tH_{TPEN}	TPOHEN[3:1] Hold Time	20		ns

Figure 51 - Transmit Overhead Input Timing

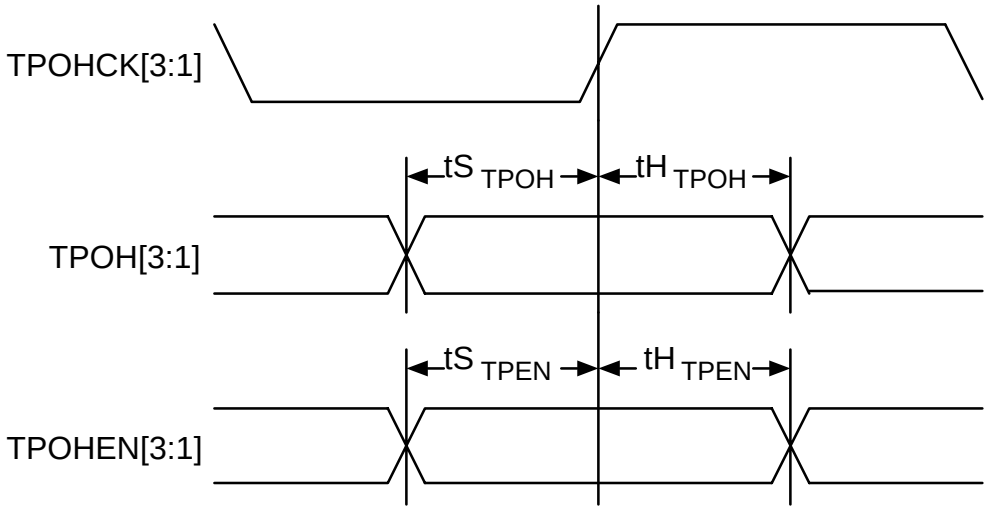


Table 20 - Transmit Overhead Output Timing (Figure 52)

Symbol	Parameter	Min	Max	Units
tP_{TPOHFP}	TPOHCK[3:1] Low to TPOHFP[3:1] Valid	-10	40	ns

Figure 52 - Transmit Overhead Output Timing

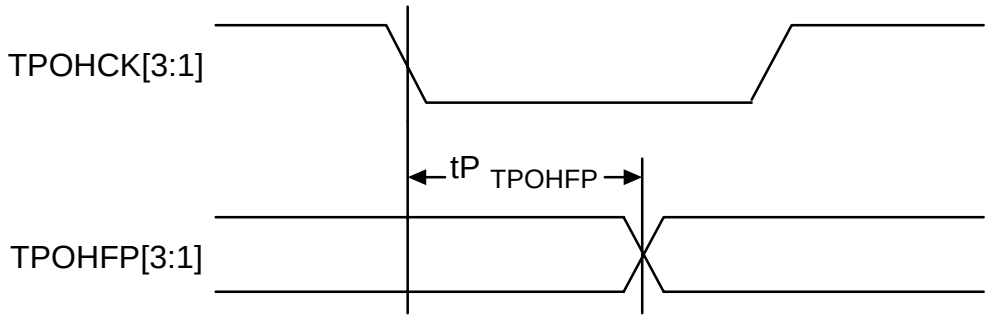


Table 21 - Transmit Alarm Port Input Timing (Figure 53)

Symbol	Parameter	Min	Max	Units
tS_{TAD}	TAD[3:1] Set-up Time	20		ns
tH_{TAD}	TAD[3:1] Hold Time	20		ns
tS_{TAFP}	TAFP[3:1] Set-up Time	20		ns
tH_{TAFP}	TAFP[3:1] Hold Time	20		ns

Figure 53 - Transmit Alarm Port Input Timing

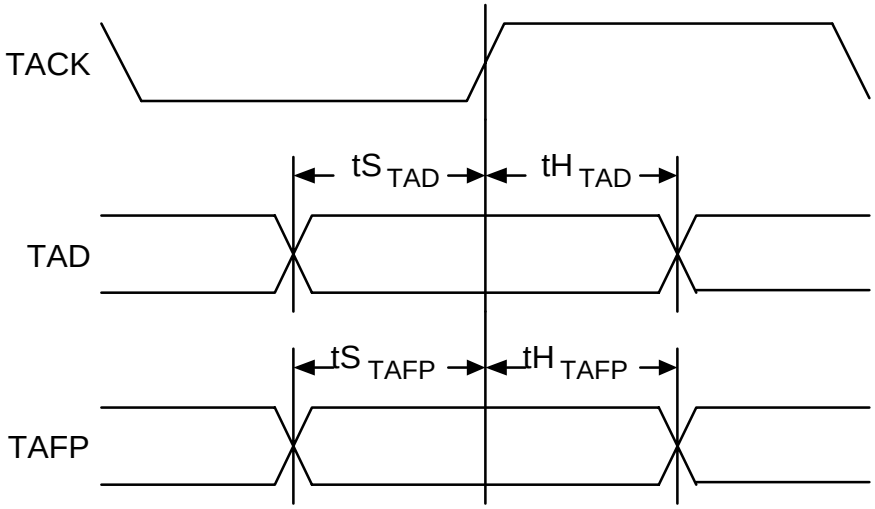


Table 22 - Transmit Stream Input Timing (Figure 54)

Symbol	Parameter	Min	Max	Units
	TCK Freq. (Nominally 19.44MHz)		20	MHz
	TCK Freq. (Nominally 6.48MHz)		7	MHz
	TCK Duty Cycle	40	60	%
tS_{TFP}	TFP Set-up Time	5		ns
tH_{TFP}	TFP Hold Time	3		ns
tS_{TPAIS}	TPAIS[3:1] Set-up Time	5		ns
tH_{TPAIS}	TPAIS[3:1] Hold Time	3		ns

Figure 54 - Transmit Stream Input Timing

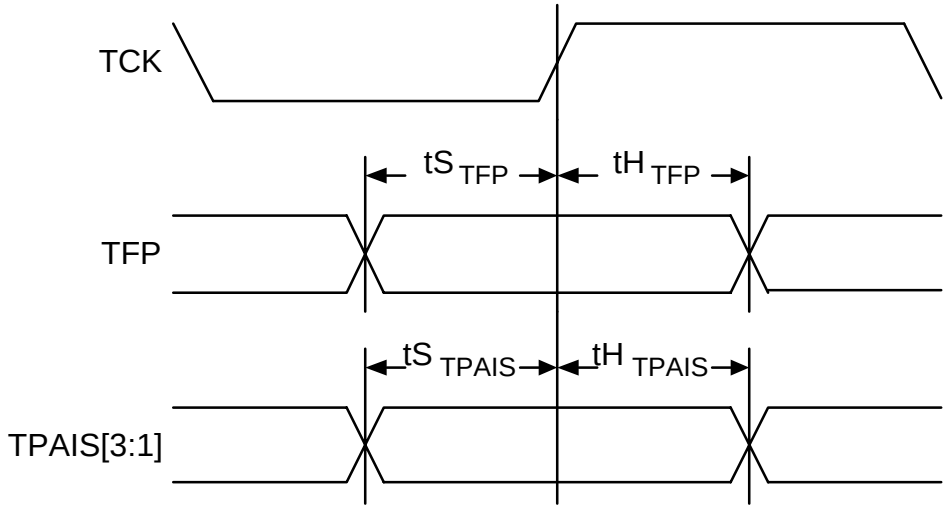
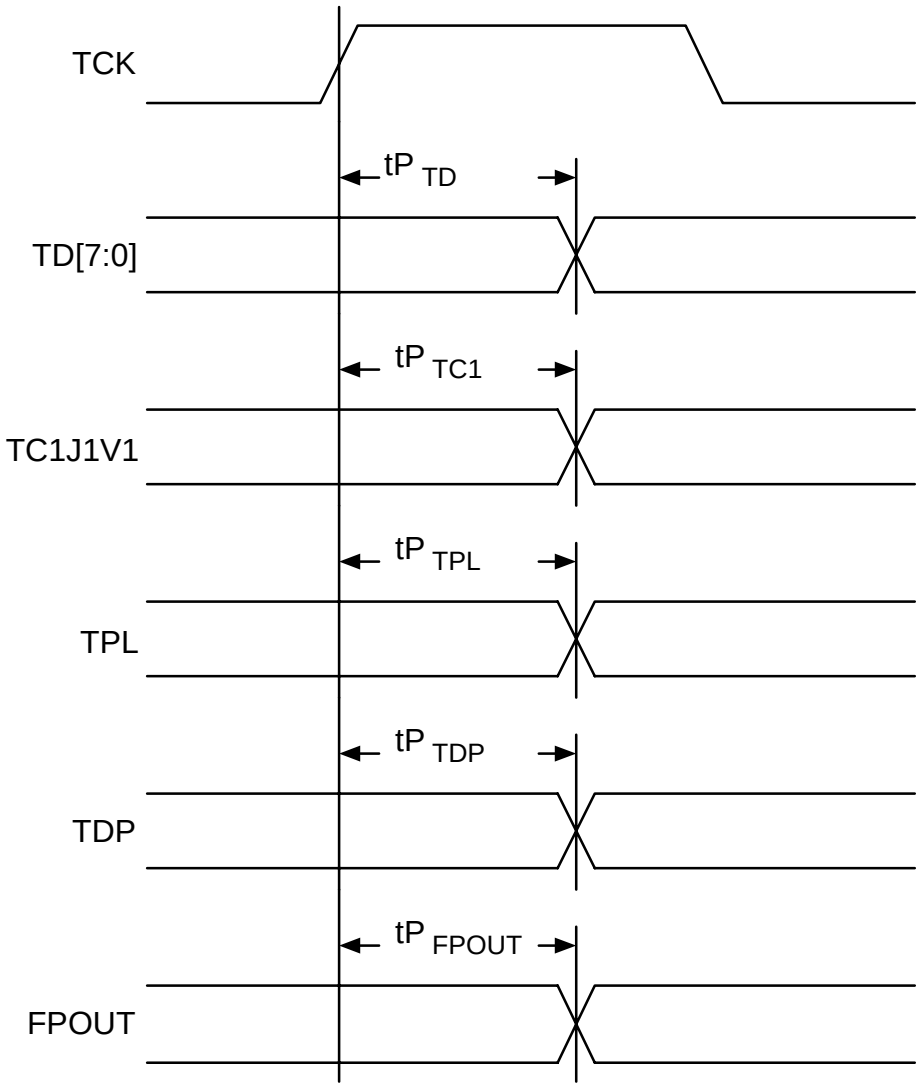


Table 23 - Transmit Stream Output Timing (Figure 55)

Symbol	Parameter	Min	Max	Units
tP_{TD}	TCK High to TD[7:0] Valid	5	25	ns
tP_{TC1}	TCK High to TC1J1V1 Valid	5	25	ns
tP_{TPL}	TCK High to TPL Valid	5	25	ns
tP_{TDP}	TCK High to TDP Valid	5	25	ns
tP_{FPOUT}	TCK High to FPOUT Valid	5	25	ns

Figure 55 - Transmit Stream Output Timing



Notes on Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

3. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

4. Output propagation delays are specified with a 50 pF load on the outputs.

18 ORDERING AND THERMAL INFORMATION

Table 24 - Ordering Information

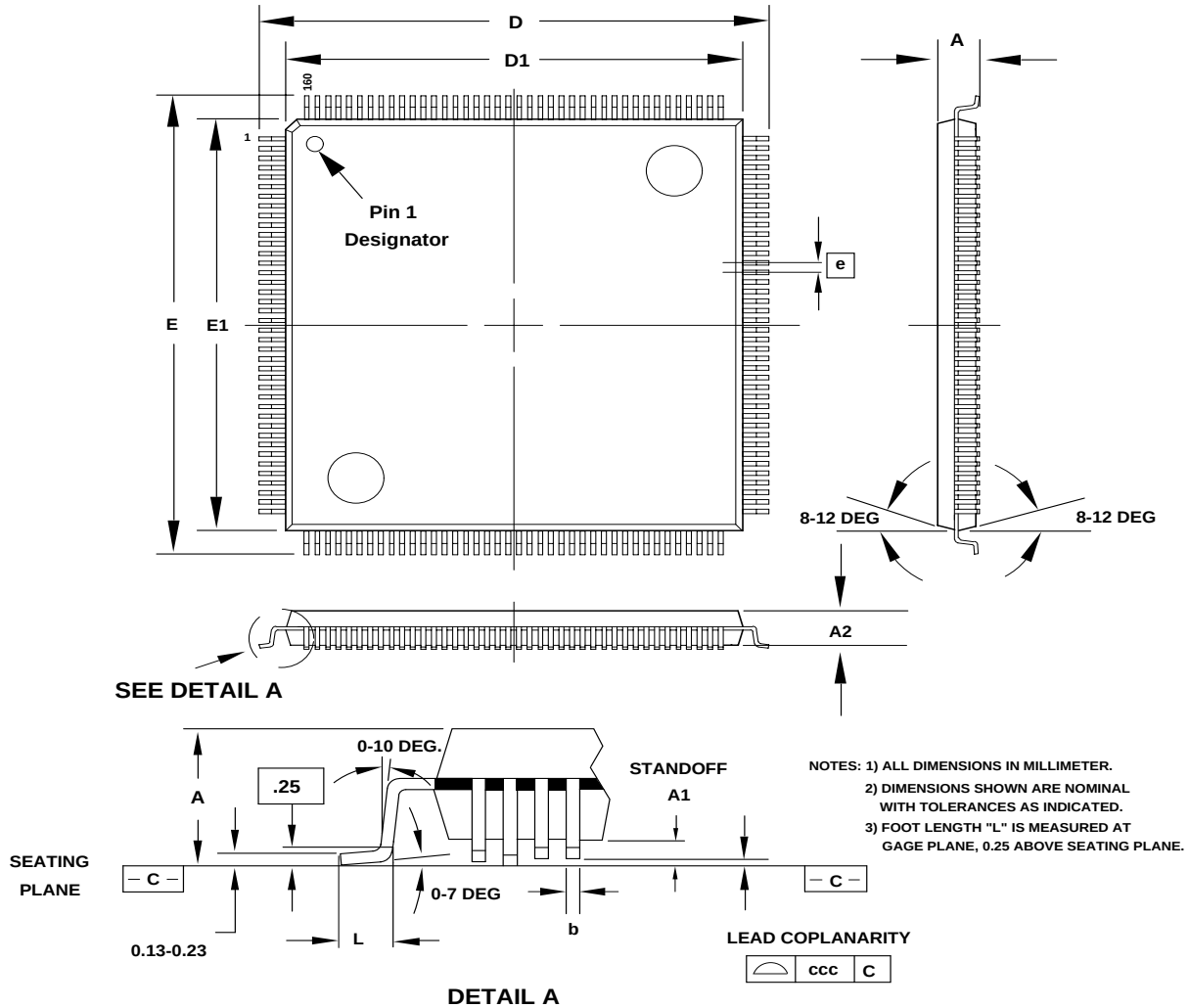
PART NO.	DESCRIPTION
PM5344-RI	160 Pin Copper Leadframe Plastic Quad Flat Pack (PQFP)

Table 25 - Thermal Information

PART NO.	AMBIENT TEMPERATURE	Theta Ja	Theta Jc
PM5344-RI	-40°C to 85°C	42 °C/W	14 °C/W

19 MECHANICAL INFORMATION

Figure 56 - 160 Pin Copper Leadframe Plastic Quad Flat Pack (R Suffix):



PACKAGE TYPE: 160 PIN METRIC PLASTIC QUAD FLATPACK-MQFP											
BODY SIZE: 28 x 28 x 3.49 MM											
Dim.	A	A1	A2	D	D1	E	E1	L	e	b	ccc
Min.	3.42	0.25	3.17	30.95	27.85	30.95	27.85	0.73		0.22	
Nom.			3.42	31.20	28.00	31.20	28.00	0.88	0.65		
Max.	4.07	0.39	3.68	31.45	28.10	31.45	28.10	1.03		0.38	0.10

NOTES

NOTES

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PMC-930531 (R6) ref PMC-920518 (P10) Issue date: July 1998