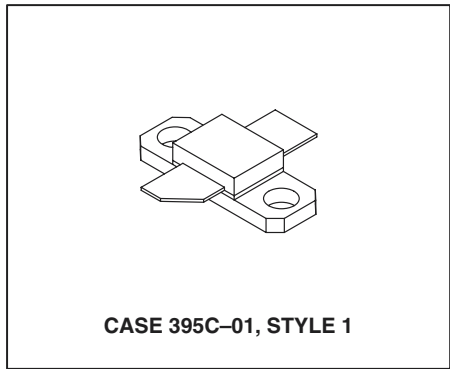


The RF Line
NPN Silicon
RF Power Transistor

MRF6404

30 W, 1.88 GHz
RF POWER TRANSISTOR
NPN SILICON



The MRF6404 is designed for 26 volts microwave large signal, common emitter, class AB linear amplifier applications operating in the range 1.8 to 2.0 GHz.

- Specified 26 Volts, 1.88 GHz Characteristics
Output Power — 30 Watts
Gain — 7.5 dB Min @ 30 Watts
Efficiency — 38% Min @ 30 Watts
- Characterized with Series Equivalent Large-Signal Parameters from 1.8 to 2.0 GHz
- To be used in Class AB for DCS1800 and PCS1900/Cellular Radio
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	24	Vdc
Collector-Emitter Voltage	V_{CES}	60	Vdc
Emitter-Base Voltage	V_{EBO}	4	Vdc
Collector-Current — Continuous	I_C	10	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	125 0.71	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (1)	$R_{\theta JC}$	1.4	$^\circ\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage ($I_C = 50\text{ mA}$, $I_B = 0$)	$V_{(BR)CEO}$	24	29	—	Vdc
Emitter-Base Breakdown Voltage ($I_E = 10\text{ mAdc}$)	$V_{(BR)EBO}$	4	5	—	Vdc
Collector-Base Breakdown Voltage ($I_C = 50\text{ mAdc}$)	$V_{(BR)CES}$	60	68	—	Vdc
Collector-Base Breakdown Voltage ($I_C = 50\text{ mAdc}$, $R_{BE} = 75\ \Omega$)	$V_{(BR)CER}$	40	56	—	Vdc
Collector Cutoff Current ($V_{CE} = 30\text{ V}$, $V_{BE} = 0$)	I_{CES}	—	—	10	mA
ON CHARACTERISTICS					
DC Current Gain ($I_C = 1\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$)	h_{FE}	20	50	120	—

(1) Thermal resistance is determined under specified RF operating condition.

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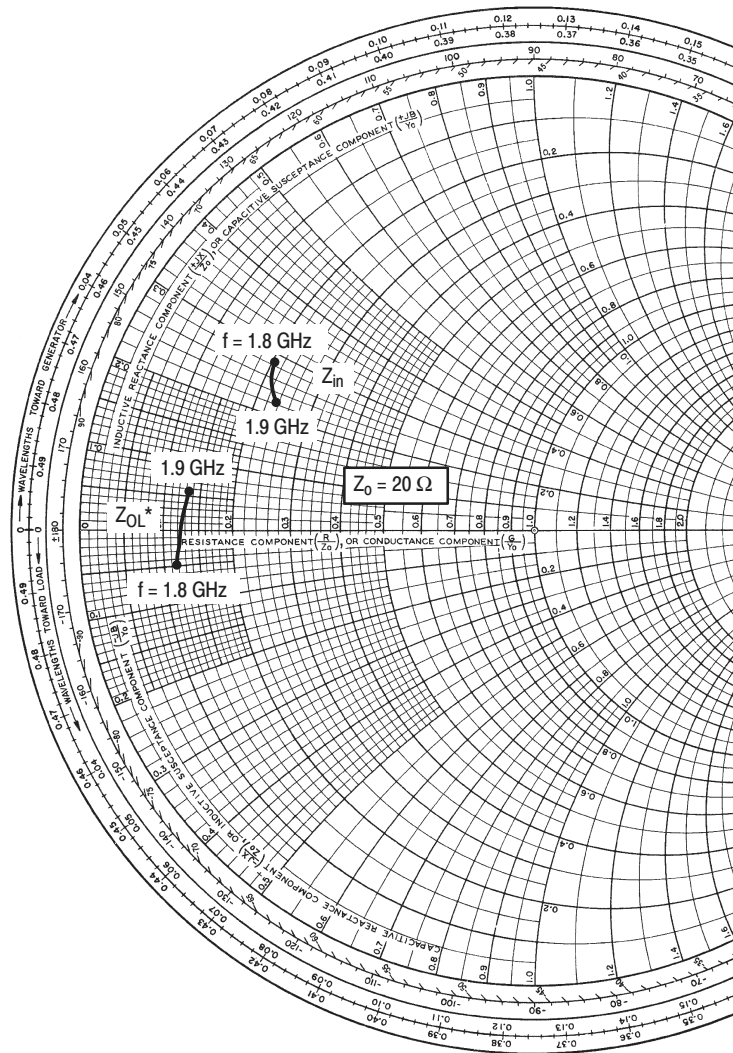
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ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Output Capacitance ($V_{CB} = 26\text{ V}$, $I_E = 0$, $f = 1\text{ MHz}$) For information only. This part is collector matched.	C_{ob}	30	38	—	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain ($V_{CC} = 26\text{ V}$, $P_{out} = 30\text{ W}$, $I_{CQ} = 150\text{ mA}$, $f = 1.88\text{ GHz}$)	G_{pe}	7.5	8.5	—	dB
Common-Emitter Amplifier Power Gain ($V_{CC} = 26\text{ V}$, $P_{out} = 28\text{ W}$, $I_{CQ} = 150\text{ mA}$) ($f = 1.99\text{ GHz}$)	G_{pe}	7	8	—	dB
Collector Efficiency ($V_{CC} = 26\text{ V}$, $P_{out} = 30\text{ W}$, $f = 1.88\text{ GHz}$) ($V_{CC} = 26\text{ V}$, $P_{out} = 28\text{ W}$, $f = 1.99\text{ GHz}$)	η	38 35	43 40	— —	%
Output Power at 1 dBc ($V_{CC} = 26\text{ V}$, $f = 1.88\text{ GHz}$) ($V_{CC} = 26\text{ V}$, $f = 1.99\text{ GHz}$)	P_{1dBc}	30 28	35 33	— —	Watts
Output Mismatch Stress: VSWR = 3:1 (all phase angles) ($V_{CC} = 26\text{ Vdc}$, $P_{out} = 25\text{ W}$, $I_{CQ} = 150\text{ mA}$, $f = 1.88\text{ GHz}$)	Ψ	No Degradation in Output Power			

ARCHIVE INFORMATION

ARCHIVE INFORMATION



DCS EVALUATION

f (GHz)	Z_{in} (Ω)	Z_{OL}^* (Ω)
1.8	$4.3 + j6.1$	$2.7 - j1.0$
1.85	$4.6 + j5.3$	$2.9 + j0.3$
1.9	$4.8 + j5.0$	$3.0 + j1.2$

Z_{OL}^* : Conjugate of optimum load impedance into which the device operates at a given output power, voltage, current and frequency.

Figure 1. Input and Output Impedances with Circuit Tuned for Maximum Gain
 @ $V_{CC} = 26\text{ V}$, $I_{CQ} = 150\text{ mA}$, $P_{out} = 30\text{ W}$

TYPICAL CHARACTERISTICS

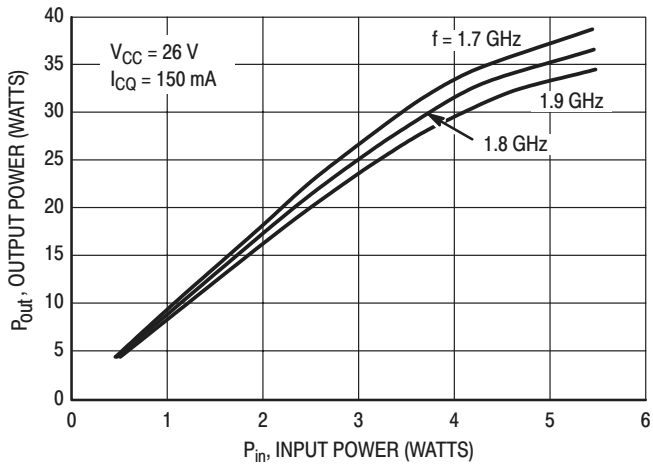


Figure 2. Output Power versus Input Power

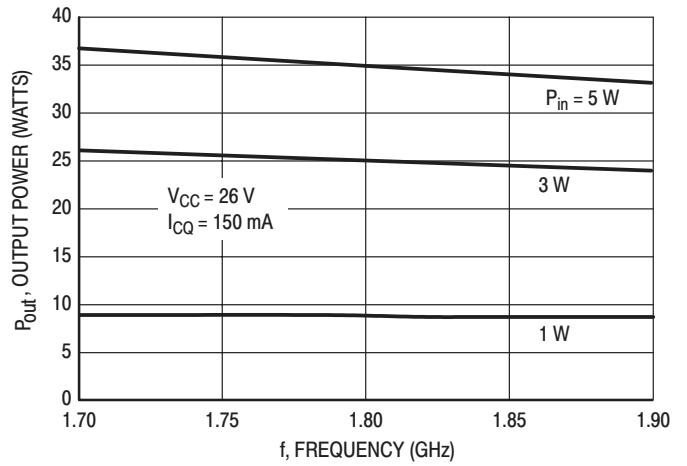


Figure 3. Output Power versus Frequency

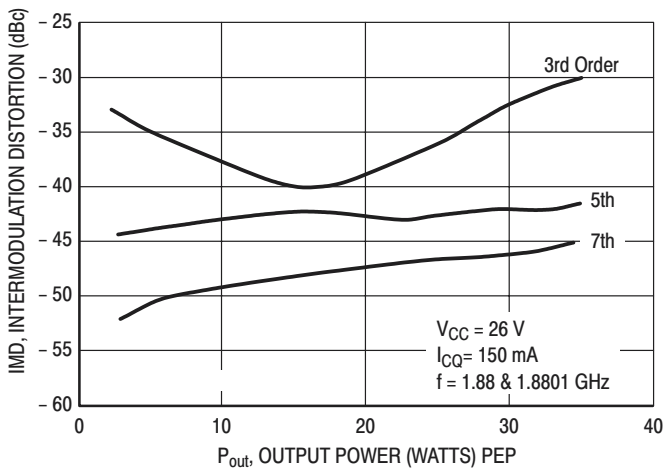


Figure 4. Intermodulation versus Output Power

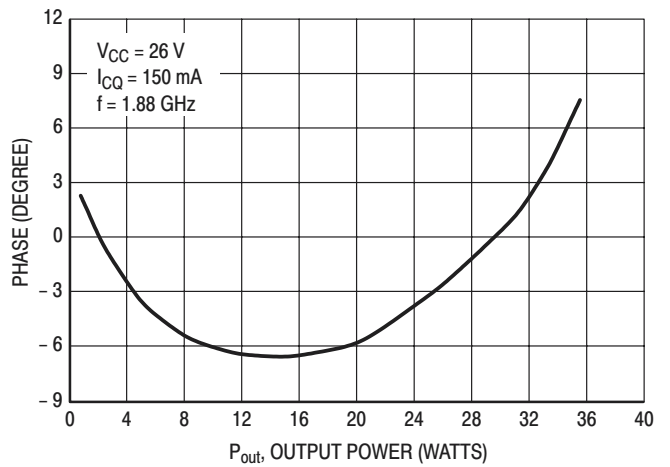
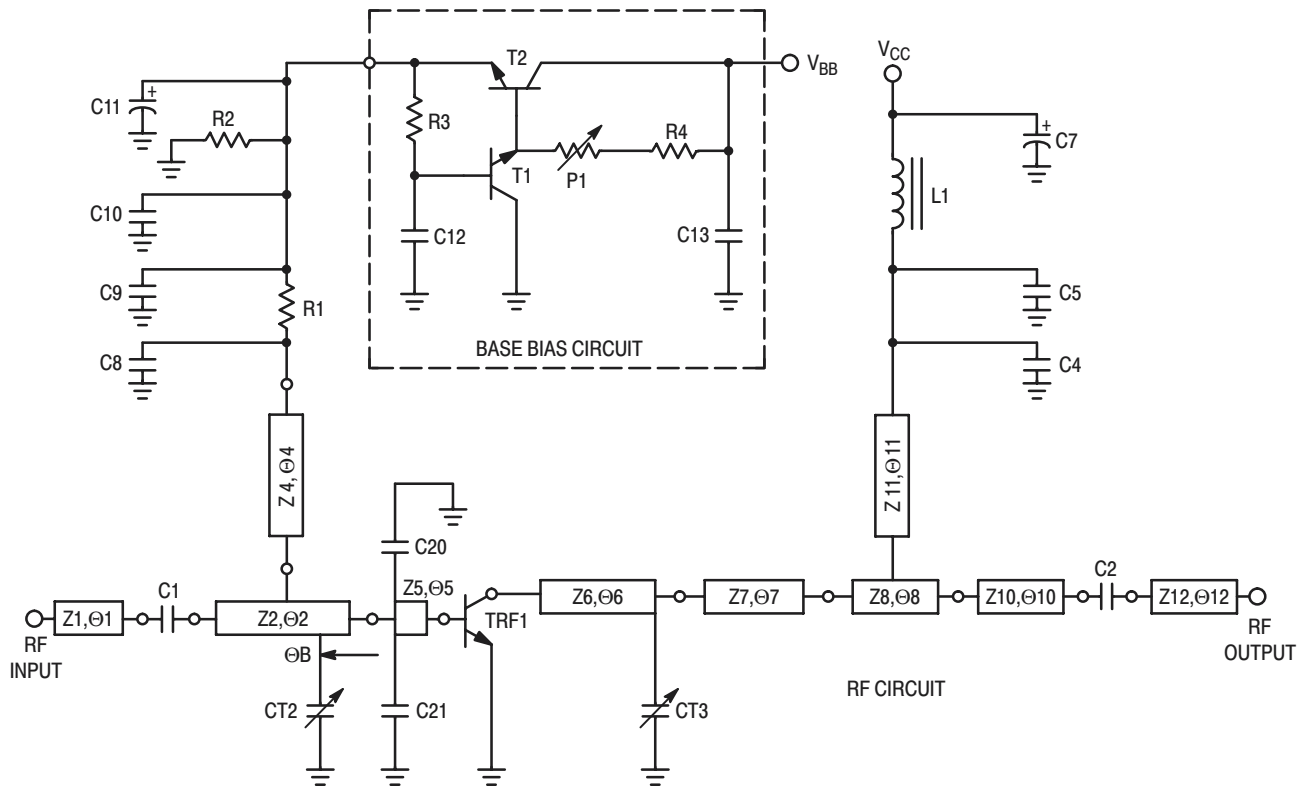


Figure 5. AM/PM Conversion



Base Bias Circuit

- C12, C13 15 nF, Chip Capacitor, Vitramon (0805 A153 JXB)
- P1 1 K Ω , Trimmer
- R3 47 Ω , Chip Resistor, 0805
- R4 330 Ω , Chip Resistor, 0805
- T1,T2 Motorola MJD 31C

Decoupling Base Bias Circuit

- C4 68 pF, Chip Capacitor, ATC 100A
- C5, C9 330 pF, Chip Capacitor, Vitramon (0805 A331 JXB)
- C7, C11 4.7 μ F, 63 V, Electrolytic Capacitor
- C8 68 pF, Chip Capacitor, ATC 100A
- C10 15 nF, Chip Capacitor, Vitramon (0805 A153 JXB)
- R1 1.5 Ω , Chip Resistor, 0805
- R2 56 Ω , Chip Resistor, 1206

RF Circuit

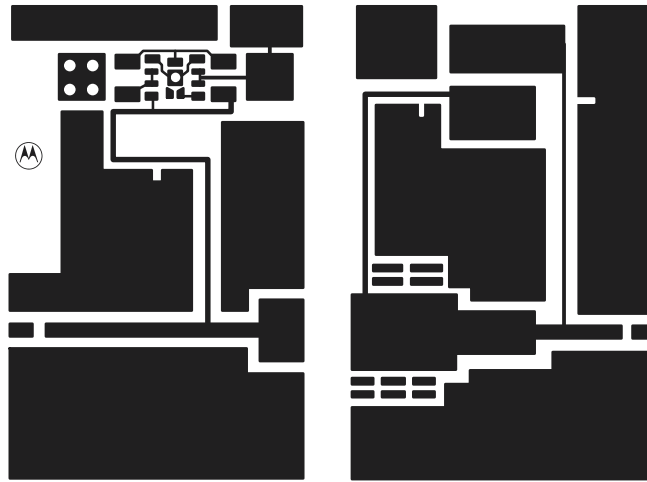
- C1, C2 68 pF, Chip Capacitor, ATC 100A
- C20, C21 1.3 pF, Chip Capacitor, ATC 100A
- CT2 Trimmer Capacitor, Gigatrim, Ref 37281
- CT3 Trimmer Capacitor, Gigatrim, Ref 37291
- TRF1 MRF6404

PC Board Material:
 $\epsilon_r = 2.55$, H = 0.508 mm, T = 0.035 mm

All Electrical Lengths Are Referenced from λ_g @ f = 1.9 GHz

- Z1 : 50 Ω θ_1 : 10 $^\circ$
- Z2 : 50 Ω θ_2 : 74.5 $^\circ$ θ_B : 16.5 $^\circ$
- Z4 : 74 Ω θ_4 : 68 $^\circ$
- Z5 : 12.8 Ω θ_5 : 21 $^\circ$
- Z6 : 10.4 Ω θ_6 : 49.5 $^\circ$
- Z7 : 18 Ω θ_7 : 36.5 $^\circ$
- Z8 : 45 Ω θ_8 : 20 $^\circ$
- Z10 : 50 Ω θ_{10} : 10 $^\circ$
- Z11 : 74 Ω θ_{11} : 74.5 $^\circ$
- Z12 : 50 Ω θ_{12} : 10 $^\circ$

Figure 6. 1.80–1.88 GHz Test Circuit Electrical Schematic and Components List



(Not to Scale)

Teflon[®] Glass 0.5 mm - Double Side 35 μm Cu.

Figure 7. 1.80–1.88 GHz PCN Test Circuit Photomaster

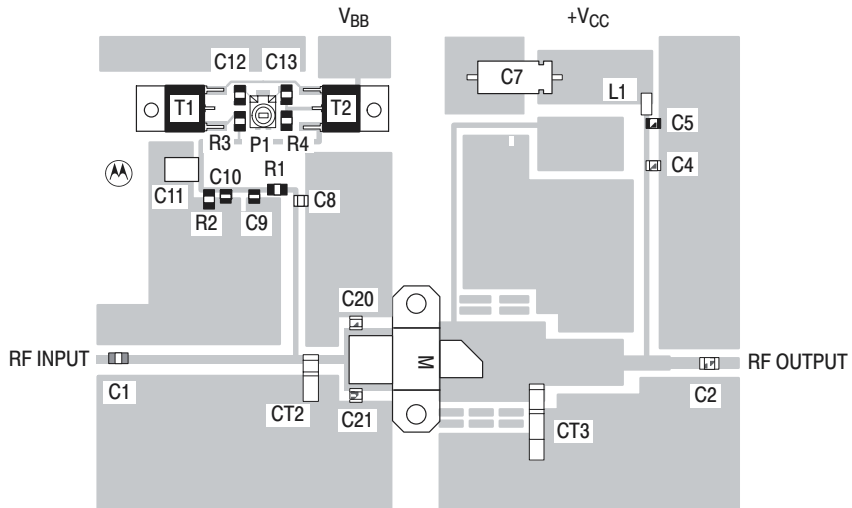
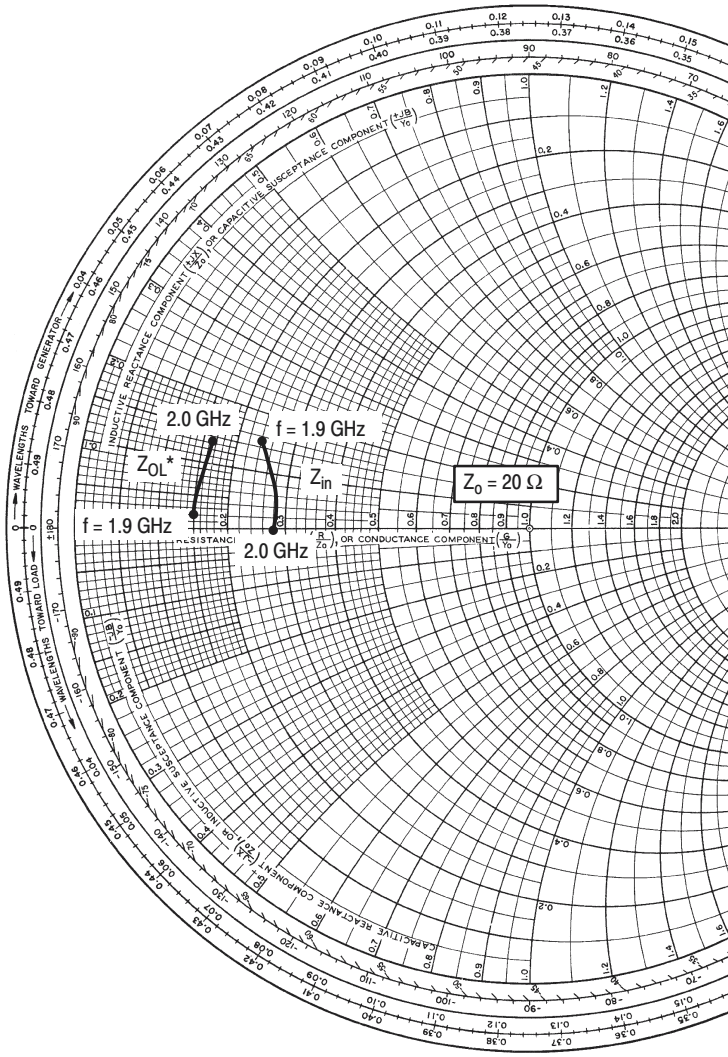


Figure 8. 1.80–1.88 GHz PCN Test Circuit Components Layout



PCS EVALUATION

f (GHz)	Z _{in} (Ω)	Z _{OL} * (Ω)
1.90	4.9 + j3.0	3.2 + j0.5
1.93	5.4 + j2.5	3.3 + j1.2
1.97	5.6 + j1.4	3.4 + j1.5
2.00	5.4 - j0.2	3.6 + j2.5

Z_{OL}*: Conjugate of optimum load impedance into which the device operates at a given output power, voltage, current and frequency.

**Figure 9. Input and Output Impedances with Circuit Tuned for Maximum Gain
@ V_{CC} = 26 V, I_{CQ} = 150 mA, P_{out} = 28 W**

TYPICAL CHARACTERISTICS

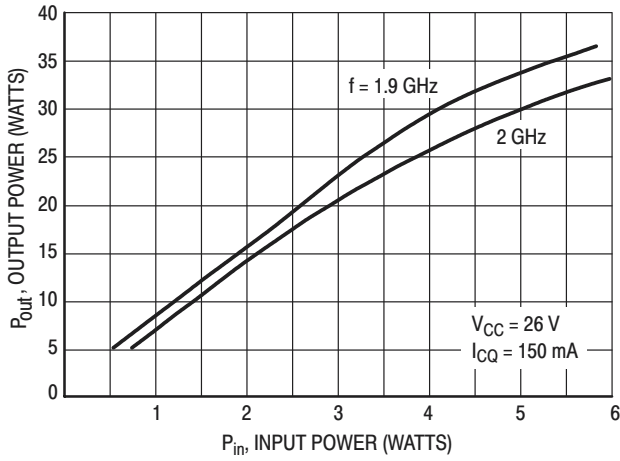


Figure 10. Output Power versus Input Power

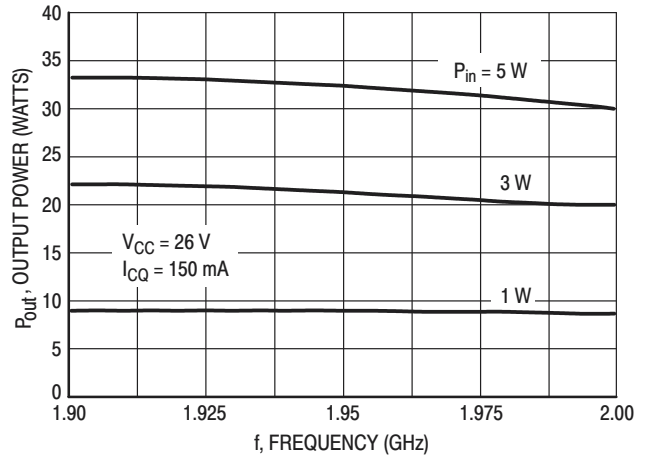


Figure 11. Output Power versus Frequency

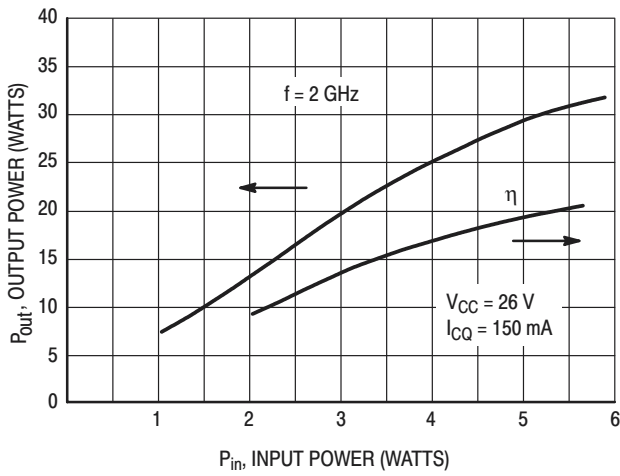


Figure 12. Output Power and Efficiency versus Input Power

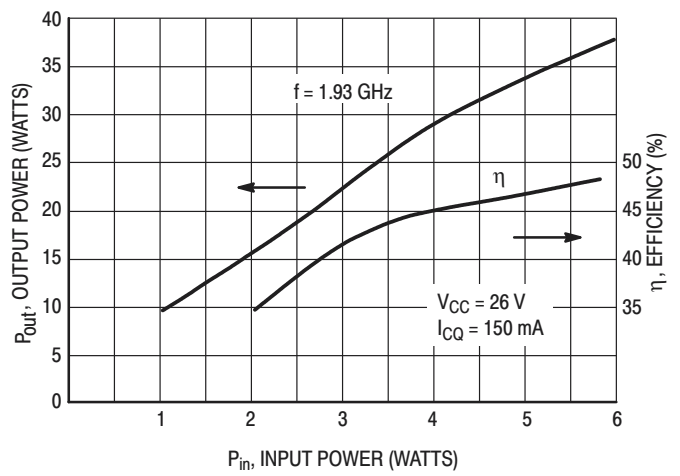


Figure 13. Output Power and Efficiency versus Input Power

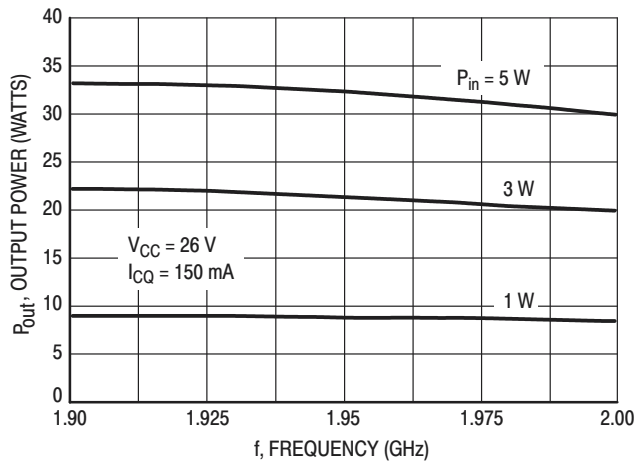
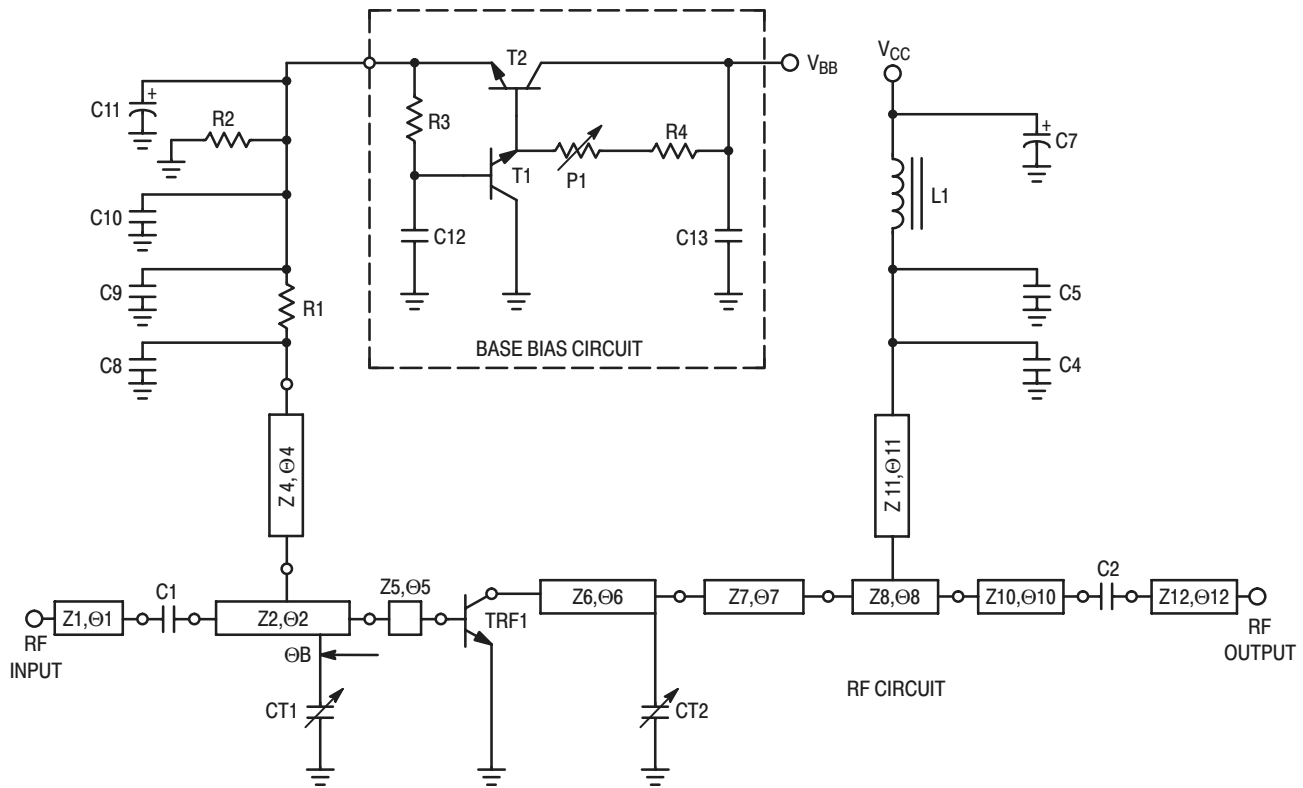


Figure 14. Output Power versus Frequency



Base Bias Circuit

C12, C13	15 nF, Chip Capacitor, Vitramon (0805 A153 JXB)
P1	1 K Ω , Trimmer
R3	47 Ω , Chip Resistor, 0805
R4	330 Ω , Chip Resistor, 0805
T1, T2	Motorola MJD 31C

Decoupling Base Bias Circuit

C4	68 pF, Chip Capacitor, ATC 100A
C5, C9	330 pF, Chip Capacitor, Vitramon (0805 A331 JXB)
C7, C11	4.7 μ F, 63 V, Electrolytic Capacitor
C8	68 pF, Chip Capacitor, ATC 100A
C10	15 nF, Chip Capacitor, Vitramon (0805 A153 JXB)
R1	1.2 Ω , Chip Resistor, 0805
R2	56 Ω , Chip Resistor, 1206

RF Circuit

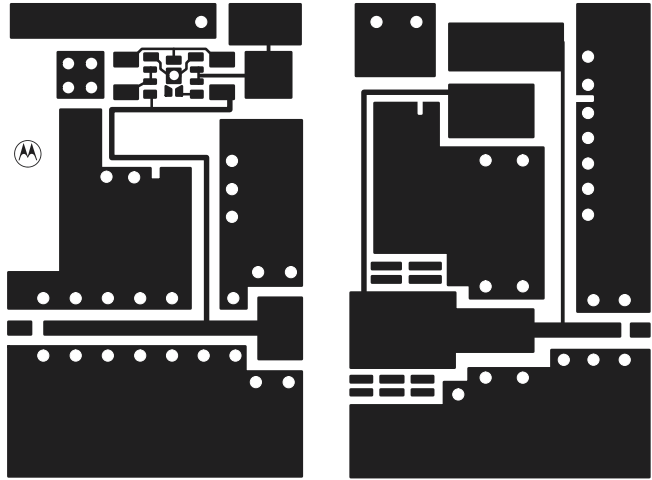
C1, C2	68 pF, Chip Capacitor, ATC 100A
C20, C21	1.3 pF, Chip Capacitor, ATC 100A
CT1, CT2	Trimmer Capacitor, Gigatrim, Ref 37271
TRF1	MRF6404

All Electrical Lengths Are Referenced from λ_g @ $f = 1.9$ GHz

Z1 : 50 Ω	$\Theta 1$: 10 $^\circ$
Z2 : 50 Ω	$\Theta 2$: 74.5 $^\circ$ ΘB : 16.5 $^\circ$
Z4 : 74 Ω	$\Theta 4$: 68 $^\circ$
Z5 : 12.8 Ω	$\Theta 5$: 21 $^\circ$
Z6 : 10.4 Ω	$\Theta 6$: 49.5 $^\circ$
Z7 : 18 Ω	$\Theta 7$: 36.5 $^\circ$
Z8 : 45 Ω	$\Theta 8$: 20 $^\circ$
Z10 : 50 Ω	$\Theta 10$: 10 $^\circ$
Z11 : 74 Ω	$\Theta 11$: 60 $^\circ$
Z12 : 50 Ω	$\Theta 12$: 10 $^\circ$

PC Board Material:
 $\epsilon_r = 2.55$, $H = 0.508$ mm, $T = 0.035$ mm

Figure 15. 1.9–2.0 GHz Test Circuit Electrical Schematic and Components List



(Not to Scale)

Teflon® Glass 0.5 mm – Double Side 35 μm Cu.

Figure 16. 1.9–2.0 GHz Test Circuit Photomaster

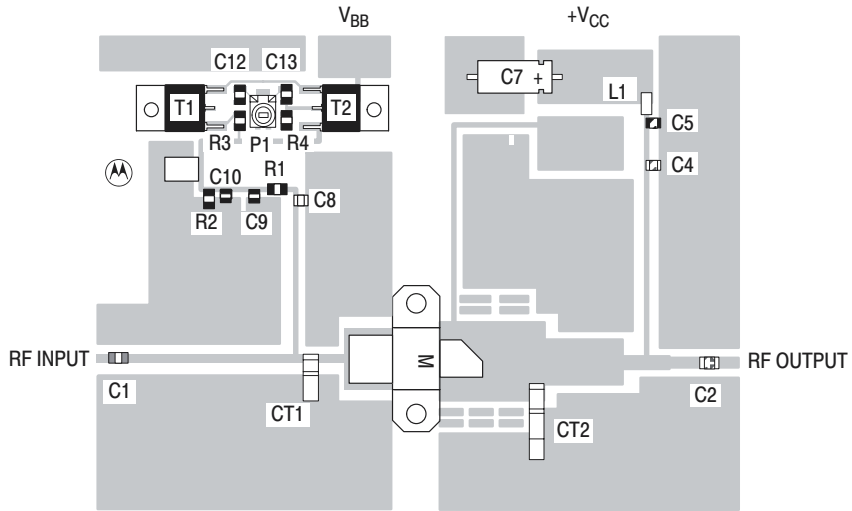
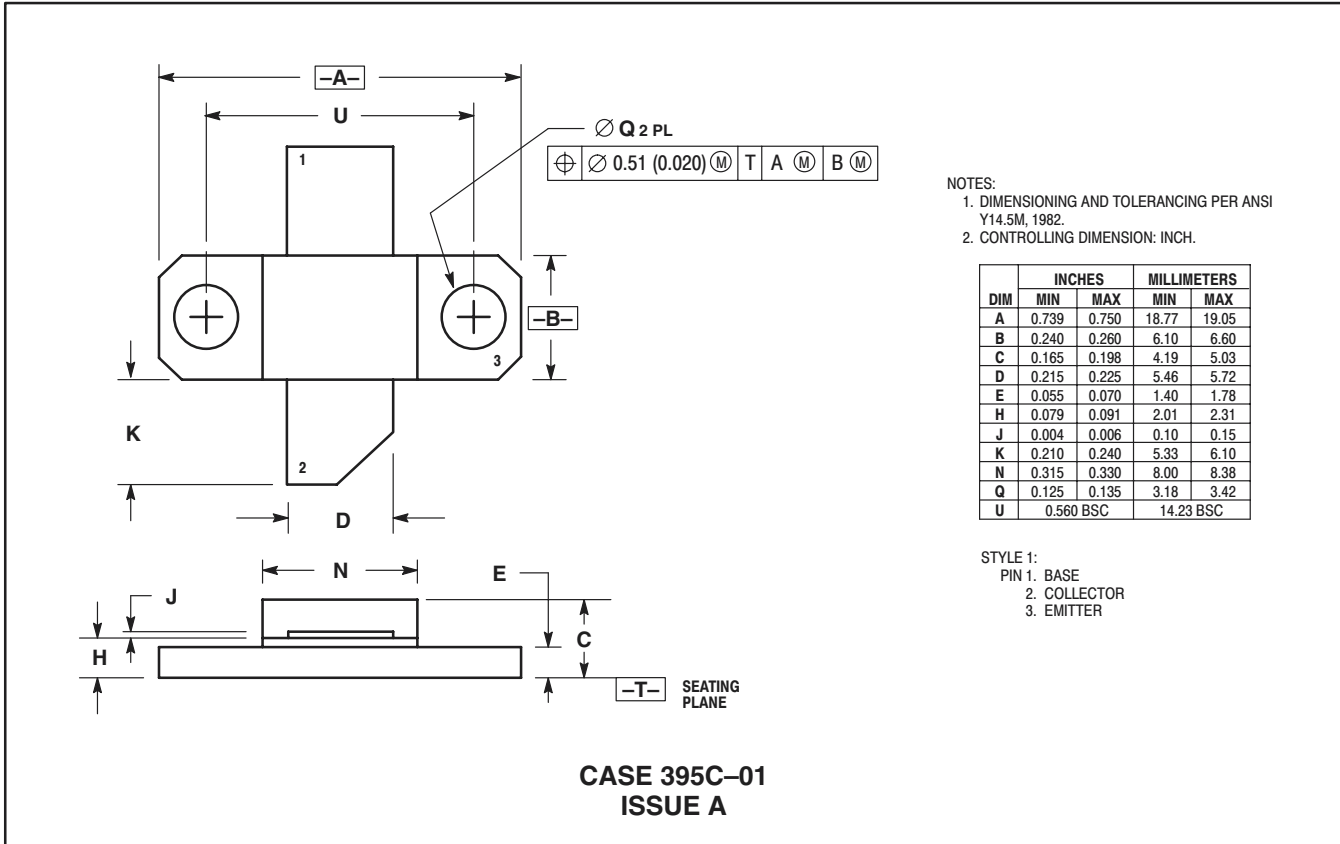


Figure 17. 1.9–2.0 GHz Test Circuit Components Layout

PACKAGE DIMENSIONS



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.739	0.750	18.77	19.05
B	0.240	0.260	6.10	6.60
C	0.165	0.198	4.19	5.03
D	0.215	0.225	5.46	5.72
E	0.055	0.070	1.40	1.78
H	0.079	0.091	2.01	2.31
J	0.004	0.006	0.10	0.15
K	0.210	0.240	5.33	6.10
N	0.315	0.330	8.00	8.38
Q	0.125	0.135	3.18	3.42
U	0.560 BSC		14.23 BSC	

- STYLE 1:
 PIN 1. BASE
 2. COLLECTOR
 3. EMITTER

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