M64092FP

SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR TV/VCR

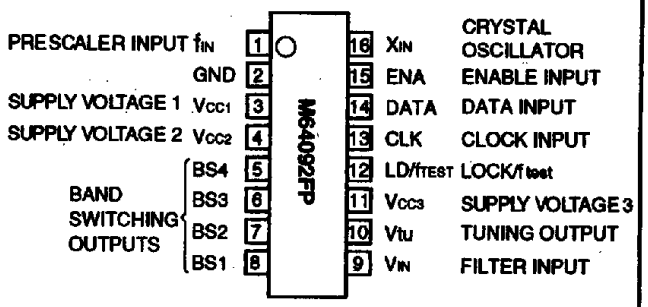
DESCRIPTION

The M64092FP is a semiconductor integrated circuit consisting of PLL frequency synthesizer for TV/VCR using Bi-CMOS process. It contains the prescaler with operating up to 1.0 GHz, 4 band drivers and tuning. Amp for direct tuning.

FEATURES

- 4 integrated PNP band drivers
  (Io=40mA, Vsat=0.2V typ @Vcc1 ~ 13.2V)
- Built-in Op. Amp for direct tuning voltage output (33V)
- Low power dissipation (Icc=24mA, Vcc=5V)
- Built-in prescaler with input amplifier (Fmax=1.0GHz)
- PLL lock/unlock status display output (Built-in pullup resistor)
- X'tal 4MHz is used to realize 3 type of tuning steps
  (Division ratio 1/512, 1/640, 1/1024)
- Serial data input (3 wire bus)
- Software compatible with M5493X series
- Aoutomatic switching of tuning step according to the number of data bits
  (62.5kHz at 18bits, 31.25kHz at 19bits)

PIN CONFIGURATION (TOP VIEW)



Outline 16P2S-A

APPLICATION

TV, VCR tuners

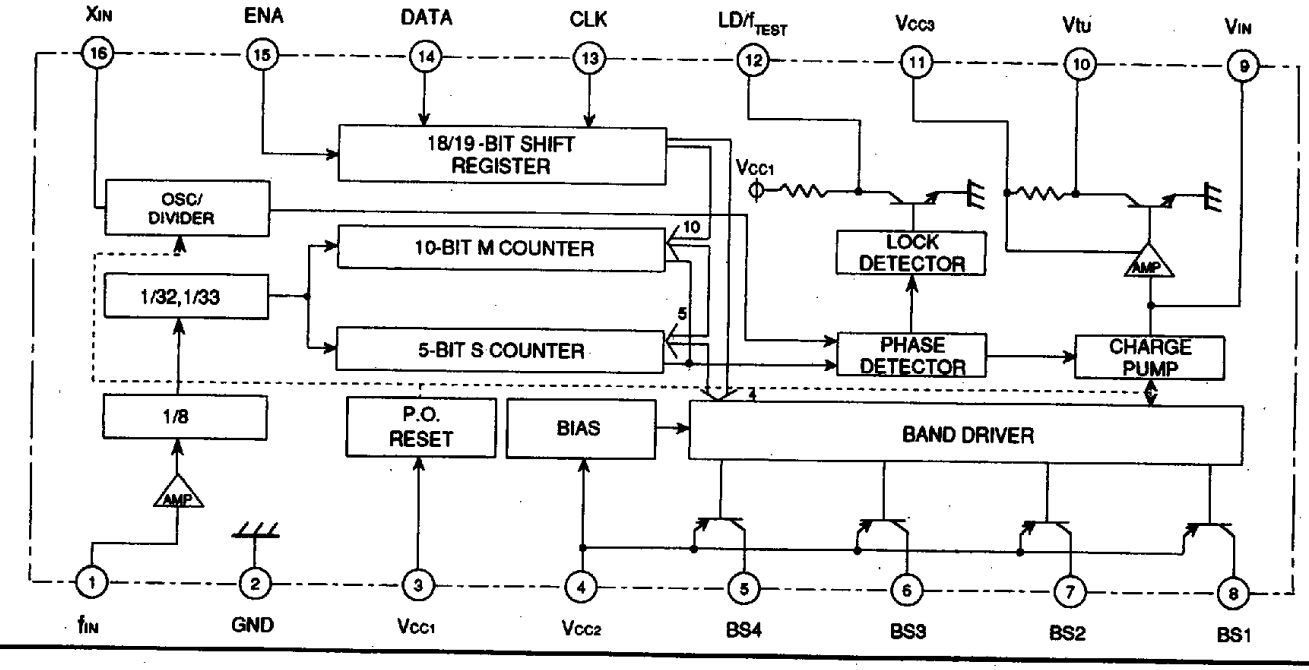
RECOMMENDED OPERATING CONDITION

Supply voltage range ..... 4.5 ~ 5.5V
Rated supply voltage 5.0V

FUNCTION

- 1/32, 1/33 dual-modulus prescaler
- 4MHz crystal oscillator, reference divider
- Programmable divider
  (10-bit M counter, 5-bit S counter)
- Tri-state phase comparator
- Lock detector
- Band switch driver
- Op. Amp for direct tuning

BLAOCK DIAGRAM



DESCRIPTION OF PIN

Pin No.	Symbol	Pin name	Function
①	f_{IN}	Prescaler input	Input for the VCO frequency.
②	GND	GND	Ground to 0V.
③	V_{CC1}	Power supply voltage 1	Power supply voltage terminal. 5.0V ± 0.5V.
④	V_{CC2}	Power supply voltage 2	Power supply for band switching, 5 ~ 13.2V.
⑤ ⑥ ⑦ ⑧	BS4 BS3 BS2 BS1	Band switching outputs	PNP open collector method is used. When the band switching data is "H", the output is ON. When it is "L", the output is OFF.
⑨	V_{IN}	Filter input (Charge pump output)	This is the output terminal for the LPF input and charge pump output. When the phase of the programmable divider output (F1/N) is ahead compared to the reference frequency (fref), the "source" current state becomes active. If it is behind, the "sink" current becomes active. If the phases are the same, the high impedance state becomes active.
⑩	V_{tu}	Tuning output	This supplies the tuning voltage.
⑪	V_{CC3}	Power supply voltage 3	Power supply voltage for tuning voltage 30 ~ 35V
⑫	LD/ f_{TEST}	Lock detect/ Test port	When 18/19 bit data is input, lock detector is output. When 27 bit data is input, lock detector is output, the programmable freq. Divider output and reference freq. Output is selected by the test mode.
⑬	CLOCK	Clock/input	Data is read into the shift register when the clock signal falls.
⑭	DATA	Data/input	Input for band SW and programmable frequency divider set up.
⑮	ENABLE	Enable input	This is normally at a "L". When this is at "H", data and clock signals are received. Data is read into the latch when the enable signal after the 18th signal of the clock signal falls or when the 19th pulse of the clock signal falls.
⑯	X_{IN}	This is connected to the crystal oscillator.	4.0MHz crystal oscillator is connected.

AB SOLUTE MAXIMUM RATINGS (Ta=-20℃ ~ +75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC1}	Supply voltage 1		6.0	V
V_{CC2}	Supply voltage 2		14.4	V
V_{CC3}	Supply voltage 3		36.0	V
V_I	Input voltage	Not to exceed Vcc1	6.0	V
V_O	Output voltage	LD output	6.0	V
V_{BSOFF}	Voltage applied when the band output is OFF		14.4	V
I_{BSON}	Band output current	per 1 band output circuit	50.0	mA
t_{BSON}	ON the time when the band output is ON	50mA per 1 band output circuit 3 circuits are on at same time.	10	sec
P_d	Power dissipation	Ta = 75℃	450	mW
T_{opr}	Operating temperature		−20~+75	℃
T_{stg}	Storage temperature		−40~+125	℃

RECOMMENDED OPERATING CONDITIONS (Ta=-20℃ ~ +75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC1}	Supply voltage 1		4.5~5.5	V
V_{CC2}	Supply voltage 2		5.0~13.2	V
V_{CC3}	Supply voltage 3		30~35	V
f_{opr1}	Operating frequency(1)	Crystal oscillation circuit	4.0	MHz
f_{opr2}	Operating frequency(2)		80~1000	MHz
I_{BDL}	Band output current 5~8	Normally 1 circuit is on. 2 circuits on at the same time is max. It is prohibited to have 3 or more circuits turned on at the same time.	0~40	mA

ELECTRICAL CHARACTRISTICS (Ta=-20℃ ~ +75℃, unless otherwise noted)

Symbol	Parameter		Test pin	Test conditions	Limits			Unit
					Min.	Typ.	Max.	
V_{IH}	Input terminal	"H" input voltage	13~15		3.0	—	V_{CC1} +0.3	V
V_{IL}		"L" input voltage	13~15		—	—	1.5	V
I_{IH}		"H" input current	13~15	V_{CC1}=5.5V V_I=4.0V	—	—	10	uA
I_{IL}		"L" input current	13~15	V_{CC1}=5.5V V_I=0.4V	—	−2	−10	uA
V_{OH}	Lock output	"H" output voltage	12	V_{CC1}=5.5V	5.0	—	—	V
V_{OL}		"L" output voltage	12	V_{CC1}=5.5V	—	0.3	0.5	V
V_{BS}	Band SW	Output voltage	5~8	V_{CC2}=12V I_O=−40mA	11.6	11.8	—	V
I_{OLK2}		Leak current	5~8	V_{CC2}=12V Band SW OFF	—	—	1	uA
V_{tOH}	Tuning output	"H" output voltage	10	V_{CC3}=33V	32.5	—	—	V
V_{tOL}		"L" output voltage	10	V_{CC3}=33V	—	0.2	0.4	V
I_{OH}	Charge pump	"H" output current	9	V_{CC1}=5.0V V_O=1V	—	±250	±470	uA
I_{OL}		"L" output current	9	V_{CC1}=5.0V V_O=1V	—	±50	±130	uA
I_{CPLK}		Leak current	9	V_{CC1}=5.5V V_O=2.5V	—	—	±50	nA
I_{CC1}	Supply current 1		2	V_{CC1}=5.5V	—	24	34	mA
I_{CC2A}	Supply current 2	4 circuits OFF	4	V_{CC2}=12V	—	—	0.5	mA
I_{CC2B}		1 circuit ON, 1 circuits ON, Output open	4	V_{CC2}=12V	—	6.0	9.0	mA
I_{CC2C}		1 circuit ON, Output current 40mA	4	V_{CC2}=12V I_O=−40mA	—	46.0	49.0	mA
I_{CC3}	Supply current 3		11	V_{CC3}=33V Output ON	—	3.6	5.5	mA

The typical values are at Vcc = 5.0V, Ta = 25℃

SWITCHING CHARACTERISTICS (Ta=-20℃ ~ +75℃, unless otherwise noted)

Symbol	Parameter	Test pin	Test conditions		Limits			Unit
					Min.	Typ.	Max.	
f_{opr2}	Prescaler operating frequency	1	V_{CC1}=4.5~5.5V V_{IN}=V_{INmin}~V_{INmax}		80	—	1000	MHz
V_{IN}	Operating input voltage	1	V_{CC1}=4.5~5.5V	80~100MHz	−24	—	4	dBm
				100~200MHz	−27	—	4	
				200~800MHz	−30	—	4	
				800~1000MHz	−27	—	4	
t_{PWC}	Clock pulse width	13	V_{CC1}=4.5~5.5V		1	—	—	us
$t_{SU(D)}$	Data setup time	14			2	—	—	us
$t_{H(D)}$	Data hold time	14			1	—	—	us
$t_{SU(E)}$	Enable setup time	15			3	—	—	us
$t_{H(E)}$	Enable hold time	15			3	—	—	us
t_{INT}	Enable data interval time	15 14			1	—	—	us
t_r	Rise time	13 14 15			—	—	1	us
t_f	Fall time	13 14 15			—	—	1	us
t_{bt}	Next enable prohibit time	15			5	—	—	us
t_{bcl}	Next clock prohibit time	13 15			5	—	—	us

METHOD OF SETTING DATA

The frequency demultiplying ratio uses 15bits. Setting up the band switching output uses 4bits.

The test mode data uses 8bits. The total bits used is 27bits. Data is read in when the enable signal is "H" and the clock signal falls.

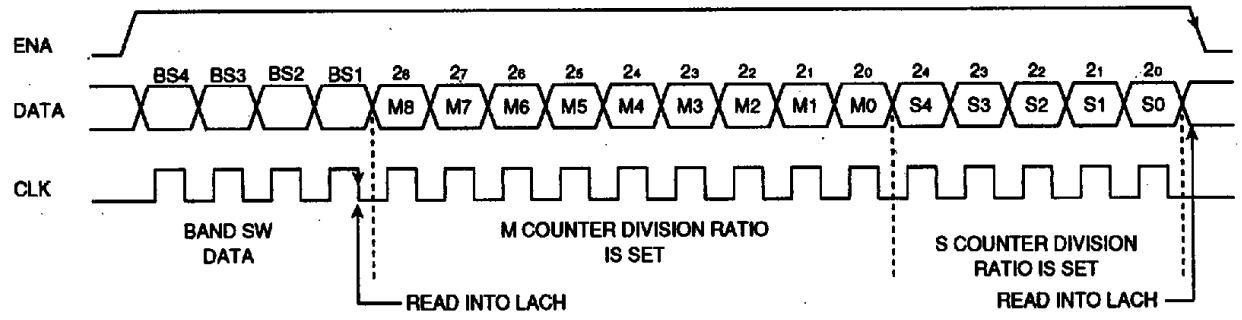
The band switching data is read in at the 4th pulse of the clock signal. The program mable counter data is read into the latch by the fall of the enable signal after the 18th pulse of the clock signal or the fall of the 19th pulse of the clock signal. When the enable signal goes to "L" before the 18th pulse of the enable signal, only the band SW data is updated and other data is ignored.

The shift register is equipped with the 18/19 bit automatic decision function. When the 18th bit data is used, the M9 bit of the program counter is reset and the 1/512 division of the reference frequency is set. In case of the 19th bit, 1/1024 division of the reference frequency is set.

(1)Transfer of the 18th bit data

Data is latched by the fall of the enable signal after the 18th clock signal. At this time, the division of the 1/512 of reference frequency is used.

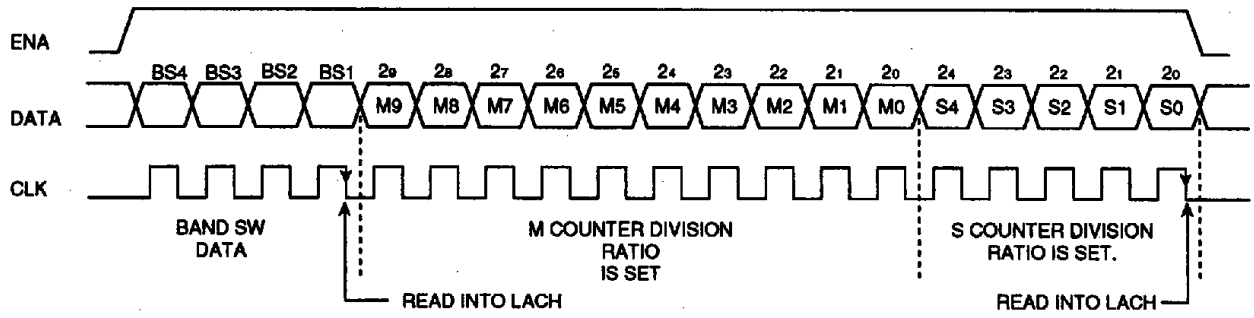
When the enable signal is "H" and the clock signal is input 19 pulses or more, it is considered the 19th bit data and the division of 1/1024 of the reference frequency is set. 18 bits data transmission is not completed till power supply is spent once again when division ratio is established once by 1/1024.



(2)Transfer of the 19th bit data

The data is latched at the 19th pulse of the clock signal. At this time, 1/1024 frequency division ratio is used. Clock signals after the above are invalid.

(It is necessary to have the ENA to fall between the 19th and the 20th bits by all means for the first data transfer after the power is turned ON.)



HOW TO SET THE DIVIDING RATIO OF THE PROGRAM-MABLE DIVIDER

(1)Transfer of the 18th bit data

Total division N is given by the following formulas in addition to the prescaler used in the previous stage.

$N=8 \cdot (32M+S)$ M : 9bit main counter division

S : 5bit swallow counter division

The M and S counters are binary the possible ranges of division are as follows.

$32 \leqq M \leqq 511$

$0 \leqq S \leqq 31$

Therefore, the range of division N is 8,192 ~ 131,064.

The tuning frequency fvco is given in the following equations.

$f_{VCO}=f_{REF} \times N$

$=7.8125 \times 8 \times (32M+S)$

$=62.5 \times (32M+S)$ [kHz]

Therefore, the tuning frequency range is 64MHz ~ 1023.9375MHz

(2)Transfer of the 19th bit data

Total divition N is given by the following formulas in addition to the prescaler used in the previous stage.

$N=8 \cdot (32M+S)$ M : 10bit main counter division

S : 5bit swallow counter division

The M and S counters are binary the possible ranges of division are as follows.

$32 \leqq M \leqq 1023$

$0 \leqq S \leqq 31$

Therefore, the range of division N is 8,192 ~ 262,136.

The tuning frequency fvco is given in the following equations.

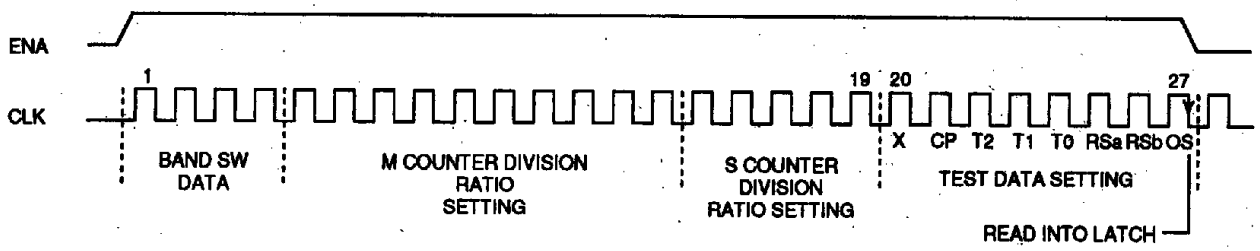
$$fvco = f_{REF} \times N$$
$$= 3.90625 \times 8 \times (32M + S)$$
$$= 31.25 \times (32M + S)\ [kHz]$$

Therefore, the tuning frequency range is 32MHz ~ 1023.96875MHz

TEST MODE DATA SET UP METHOD

The data for the test mode uses 20 ~ 27bits. Data is latched when the 27th clock signal falls.

(1)When transferring 3-wire 27 bit data



(2)Test mode bit set up

X : Random, normal 0

CP : Set up the charge pump current value

T0, T1, T2 : Set up test modes

RSa, RSb : Set the frequency division of the reference frequency

OS : Set up the tuning amplifier

Setting up the output current value of the charge pump of the phase comparator

CP	Charge pump current	Mode
0	50uA	Normal
1	250uA	Test

Setting up for the test mode

T2	T1	T0	Charge pump	12 pin output	Mode
0	0	X	Normal operation	LD	Normal operation
0	1	X	High impedance	LD	Test mode
1	1	0	Sink	LD	Test mode
1	1	1	Source	LD	Test mode
1	0	0	High impedance	f_{REF}	Test mode
1	0	1	High impedance	$f_{I/N}$	Test mode

Set up for the reference frequency division ratio

RSa	RSb	Division ratio
1	1	1/512
0	1	1/1024
X	0	1/640

Set up the tuning amplifier

OS	Tuning voltage output	Mode
0	ON	Normal
1	OFF	Test

Power on reset operation (Initial state the power is turned ON)

BS4 ~ BS1 : OFF

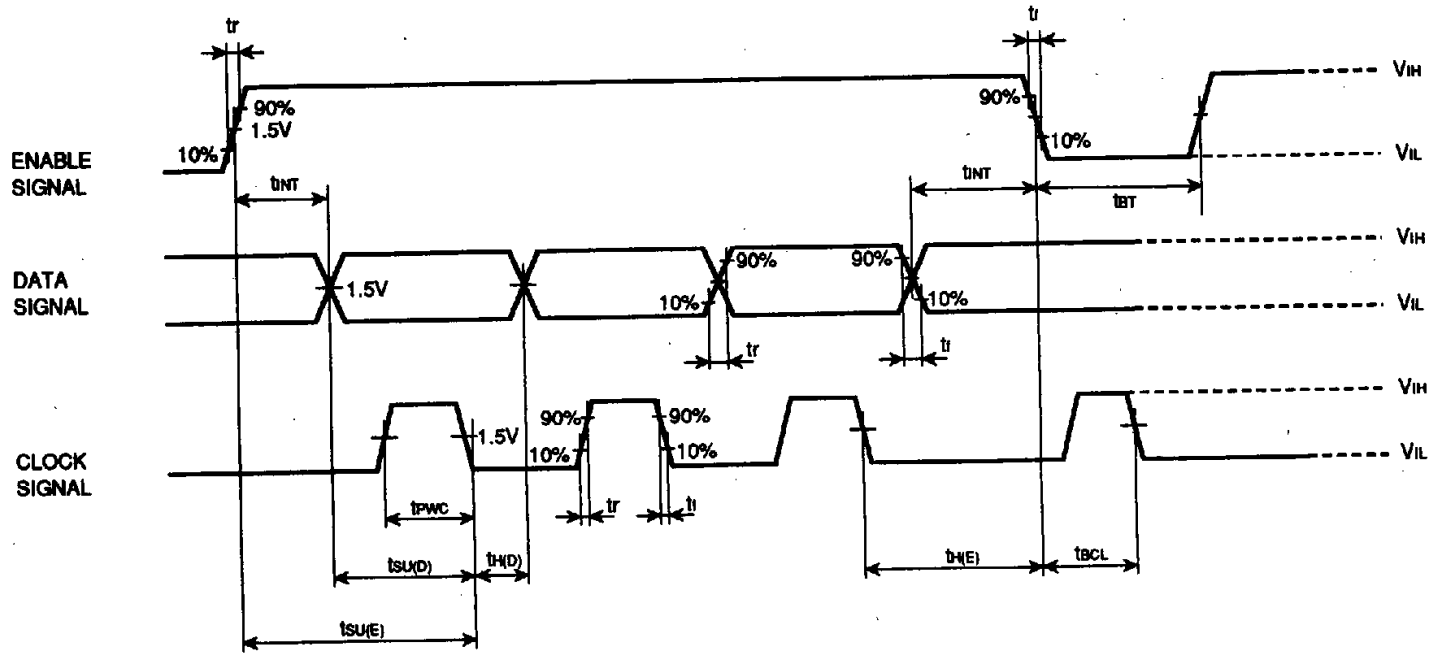
Charge pump : High impedance

Tuning amplifier : OFF

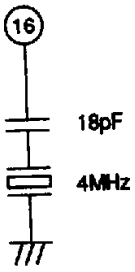
Charge pump current : 250 μA

Frequency division ratio : 1/512

TIMING DIAGRAM

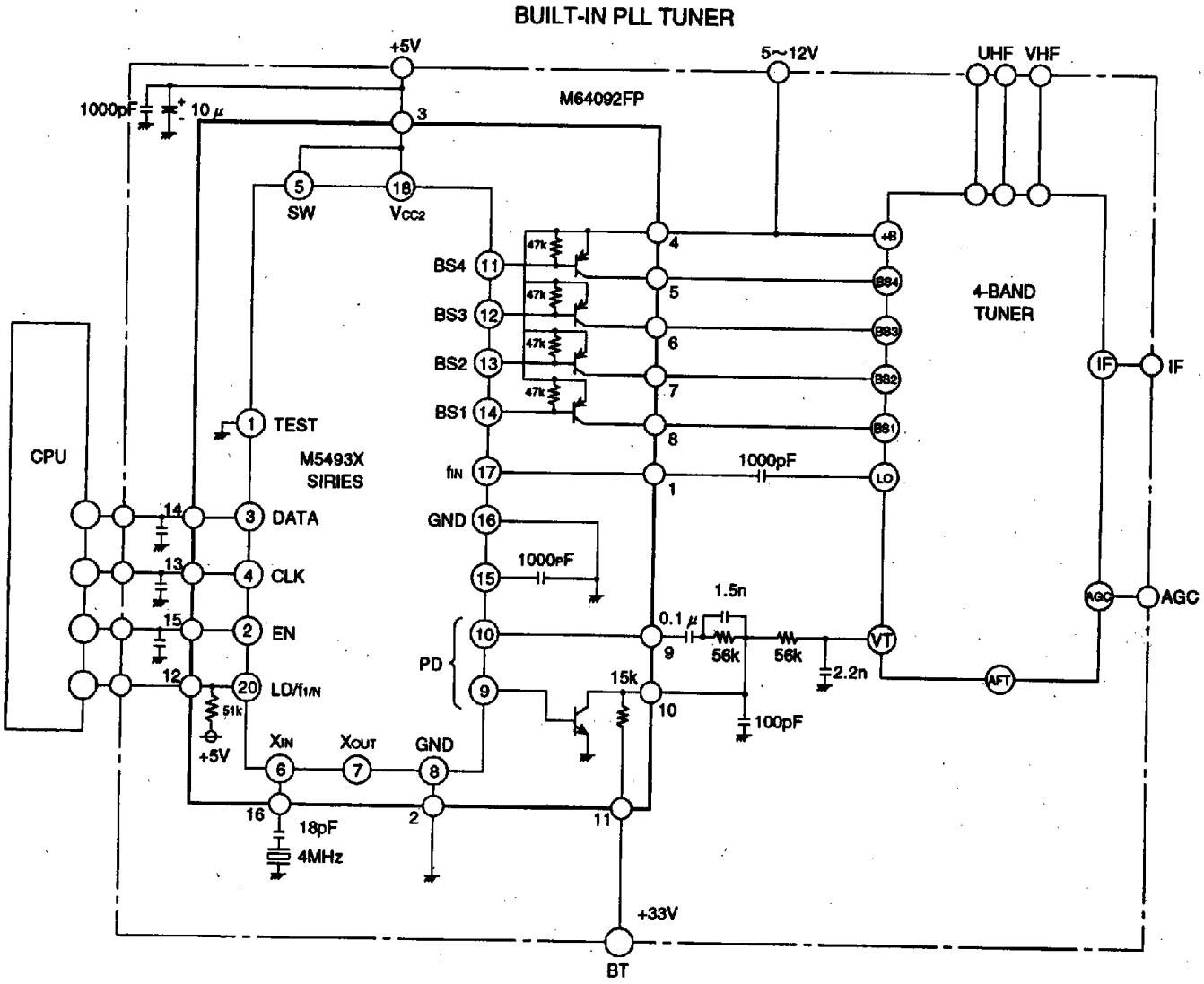


CRYSTAL OSCILLATOR CONNECTION DIAGRAM



Crystal oscillator characteristics
Actual resistance : less than 100 Ω
Load capacitance : 20 pF

APPLICATION EXAMPLE



Units Resistance:Ω
Capacitance:F