SONY

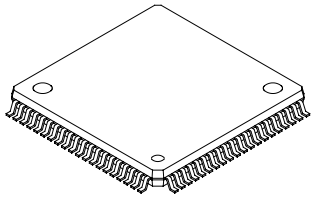
CXB1451Q

VGA/SVGA/XGA digital data serial transmitter

Features

- 1 chip transmitter for serial transmission of 18bit color VGA/SVGA/XGA picture
- On chip differential cable driver
- TTL/CMOS compatible interface
- Support 1 pixel/shiftclock mode & 2 pixel/shiftclock mode
- +3.3V single power supply
- Low power consumption
- 80pin Plastic QFP Package (Body size: 14mm × 14mm)

80 pin QFP (Plastic)



Block Digagram & Pin out

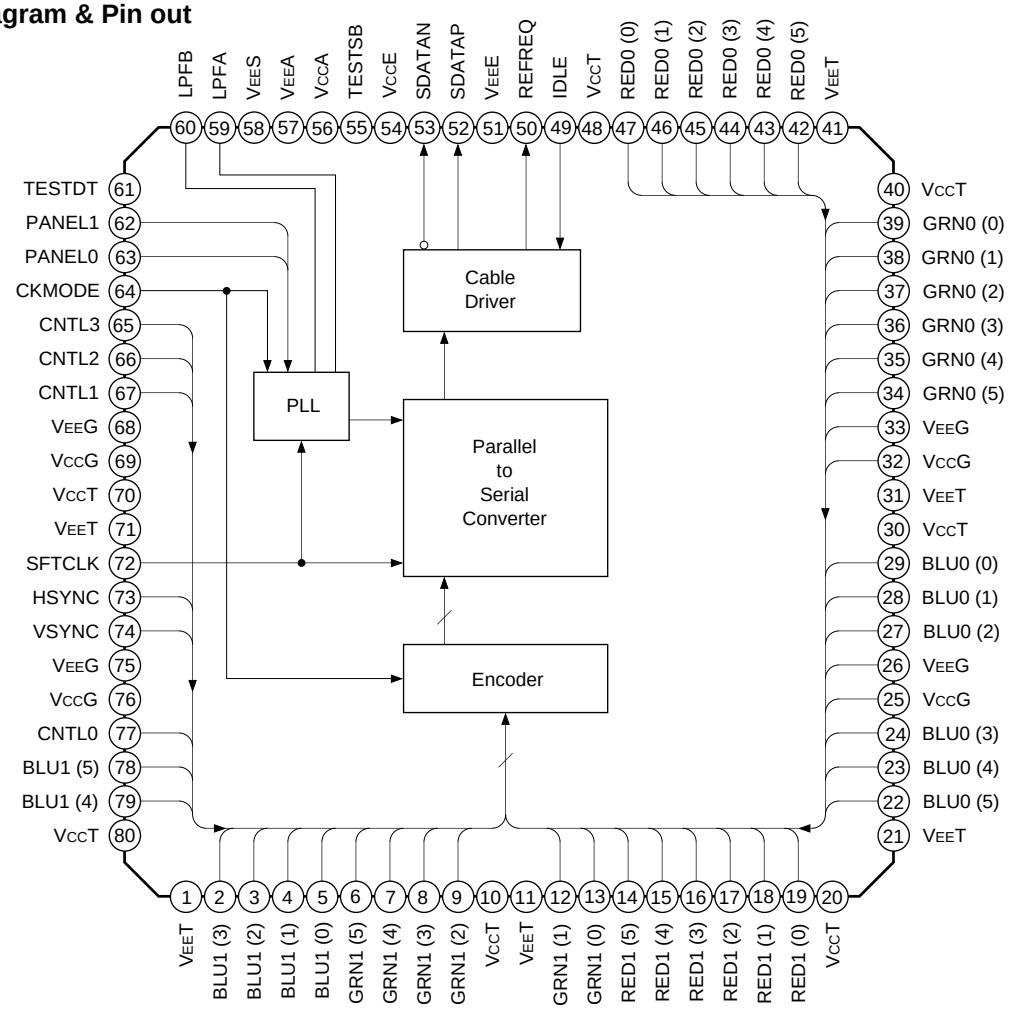


Fig. 1. Block Diagram & Pin out

E97913A1Z-PS

Pin List

Power/Ground

Pin Name	Pin Number	Descriptions
V_{CC}T	10, 20, 30, 40, 48, 70, 80	TTL power surpply , should be connected to 3.3V ± 5%
V_{EE}T	1, 11, 21, 31, 41, 71	TTL ground, connected to 0V
V_{CC}G	25, 32, 69, 76	Logical core power surpply, connected to 3.3V ± 5%
V_{EE}G	26, 33, 68, 75	Logical core ground, connected to 0V
V_{CC}E	54	Serial driver power surpply, connected to 3.3V ± 5%
V_{EE}E	51	Serial driver ground, connected to 0V
V_{CC}A	56	Analog power surpply, connected to 3.3V ± 5%
V_{EE}A	57	Analog ground, connected to 0V
V_{EE}S	58	Analog substrate, connected to 0V

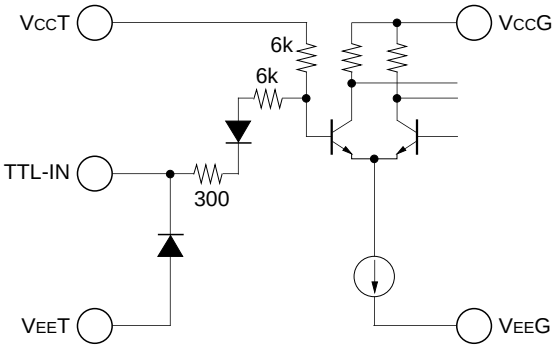
Digital Signals

Pin Name	Pin Number	Type	Descriptions
SFTCLK	72	TTL in	Shift clock, for the data fetch at rising or falling edge
RED1 (5 to 0) GRN1 (5 to 0) BLU1 (5 to 0)	14, 15, 16, 17, 18, 19 6, 7, 8, 9, 12, 13 78, 79, 2, 3, 4, 5	TTL in	Pixel data input in 1 pixcel/sftclk mode 2nd pixel data input in 2 pixel/sftclk mode
RED0 (5 to 0) GRN0 (5 to 0) BLU0 (5 to 0)	42, 43, 44, 45, 46, 47 34, 35, 36, 37, 38, 39 22, 23, 24, 27, 28, 29	TTL in	Ignored in 1 pixcel/sftclk mode 1st pixel data input in 2 pixel/sftclk mode
HSYNC	73	TTL in	Hsync data
VSYNC	74	TTL in	Vsync data
CNTL (3 to 0)	65, 66, 67, 77	TTL in	Control data
PANEL (1, 0)	62, 63	TTL in	Panel mode select switch
CKMODE	64	TTL in	Clock mode select switch
IDLE	49	TTL in	Idle mode select switch
SDATAP/N	52, 53	Tx	Serial Output & Refclk request input
REFREQ	50	TTL out	Refclk request detect flag

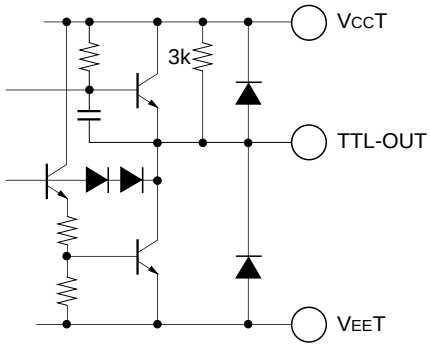
Special

Pin Name	Pin Number	Descriptions
TESTSB/DT	55, 61	SFTCLK polarity / TEST function control
LPFA/B	59, 60	External loop filter

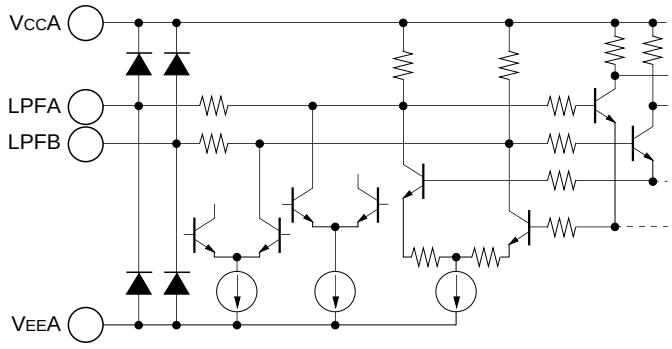
Equivalent I/O circuit



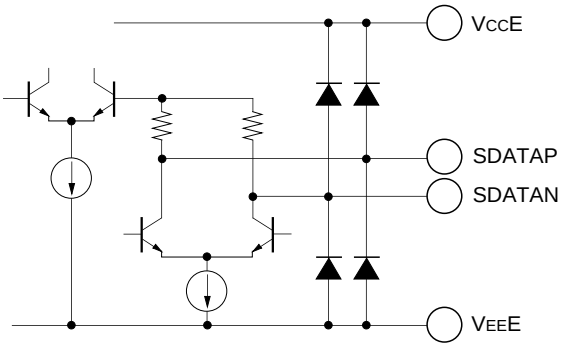
(a) TTL input equivalent circuit



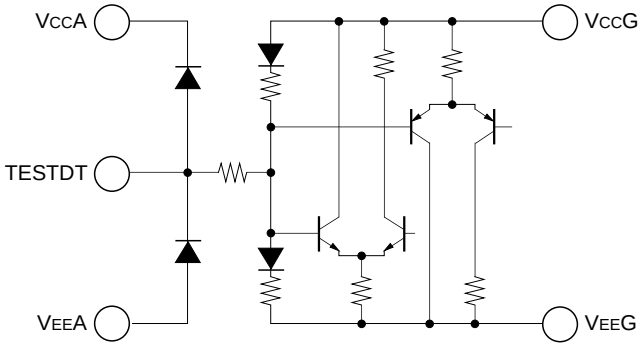
(b) TTL output equivalent circuit



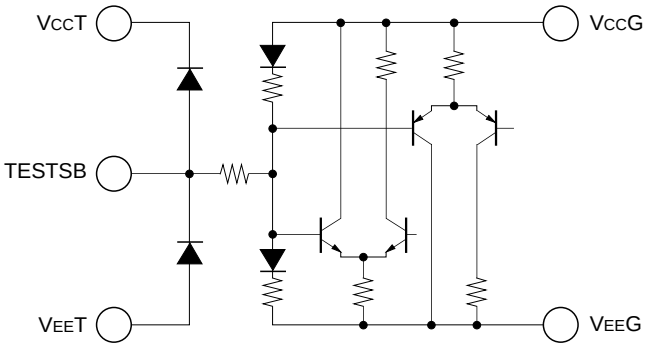
(c) LPFA/B equivalent circuit



(d) SDATAP/N equivalent circuit



(e) TESTDT equivalent circuit



(f) TESTSB equivalent circuit

Electrical characteristics

Tab. 1. Absolute Maximum Rating

Description	Symbol	Min.	Typ.	Max.	Unit	Comments
Power supply voltage	V_{CC}	–0.3		4	V	
TTL DC input voltage	V_I_T	–0.5		5.5	V	
TTL output current (High)	I_{OH}_T	–20		0	mA	
TTL output current (Low)	I_{OL}_T	0		20	mA	
Serial output pin voltage	Vsdout	–0.5		V_{CC} + 0.5	V	
Ambient temperature	Ta	–55		70	°C	Under bias
Storage temperature	Tstg	–65		150	°C	

Tab. 2. Recommended Operating Conditions

Description	Symbol	Min.	Typ.	Max.	Unit	Comments
Power supply voltage (Include V_{CC}T5)	V_{CC}	3.135	3.3	3.465	V	
Ambient temperature	Ta	0		70	°C	

Tab. 3. DC Characteristics (Under the recommended conditons. See Tab. 2)

Description	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input HIGH voltage (TTL)	V_{IH}_T	2		5.5	V	
Input LOW voltage (TTL)	V_{IL}_T	–0.5		0.8	V	
Input HIGH current (TTL)	I_{IH}_T			20	µA	$V_{IN} = V_{CC}$
Input LOW current (TTL)	I_{IL}_T	–400			µA	$V_{IN} = 0$
Output HIGH voltage (TTL)	V_{OH}_T	2.3			V	I_{OH} = –0.2mA
Output LOW voltage (TTL)	V_{OL}_T			0.4	V	I_{OL} = 4mA
Output HIGH current (SDATA)	I_{OH}_SD	–0.1	0	+0.1	mA	See Fig. 2
Output LOW current (SDATA)	I_{OL}_SD	14.7	16	17.3	mA	
Input HIGH voltage (SDATA)	V_{IH}_SD	V_{CC} – 0.6			V	Common mode voltage
Input LOW voltage (SDATA)	V_{IL}_SD			V_{CC} – 0.7	V	
Supply current	I_{CC}	165 175	215 225	265 275	mA mA	XGA, Outputs open SVGA/VGA, Outputs open

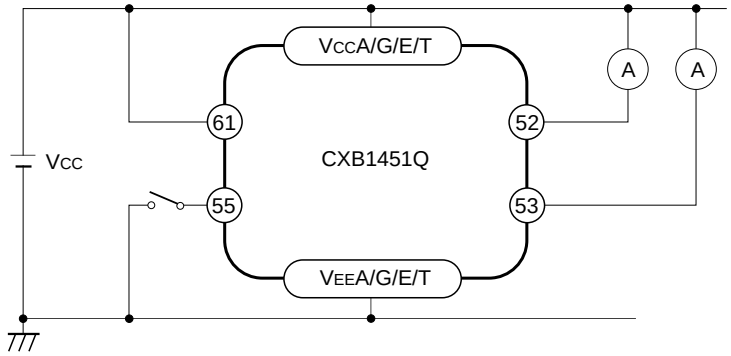


Fig. 2. I_{OH}_SD and I_{OL}_SD DC measurement

Tab. 4. AC Characteristics (Under the recommended conditons. See Tab. 5)

Description	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input TTL rise time	Tir	0.7		4.8	ns	0.8V to 2.0V
Input TTL fall time	Tir	0.7		4.8	ns	2.0V to 0.8V
SFTCLK frequency	Fsftclk	20.0 10.0 38.0 19.0 60.0 30.0	25.0 12.5 40.0 20.0 65.0 32.5	28.0 14.0 48.0 24.0 68.0 34.0	MHz MHz MHz MHz MHz MHz	VGA, 1 pixel/sftclk mode VGA, 2 pixel/sftclk mode SVGA, 1 pixel/sftclk mode SVGA, 2 pixel/sftclk mode XGA, 1 pixel/sftclk mode XGA, 2 pixel/sftclk mode
SFTCLK duty factor	Dsftclk	40		60	%	Vth = 1.4V
Pixel/Sync/Cntl setup to SFTCLK	Tsetup	4.0			ns	XGA 1 pixel/sftclk mode @65MHz See Fig. 4
Pixel/Sync/Cntl hold to SFTCLK	Thold	1.0			ns	
SDATA rise time	Tor			400	ps	20 to 80%, C_L = 2pF See Fig. 3
SDATA fall time	Tof			400	ps	
CLOCK mode assert time	TAclk		130		ns	
CLOCK mode deassert time	TDclk		10		ns	
IDLE mode assert time	TAidle		150		ns	
IDLE mode deassert time	TDidle		350		ns	
PLL lockin time	Tlockin		0.1		ms	

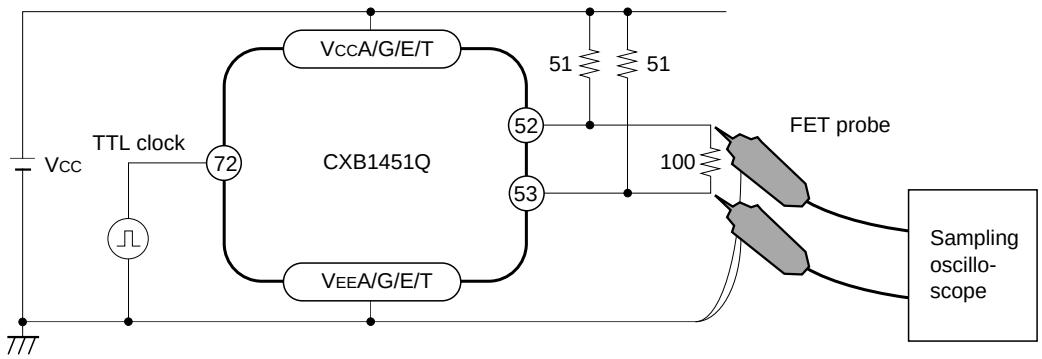


Fig. 3. SDATA waveform measurement

Timing Chart

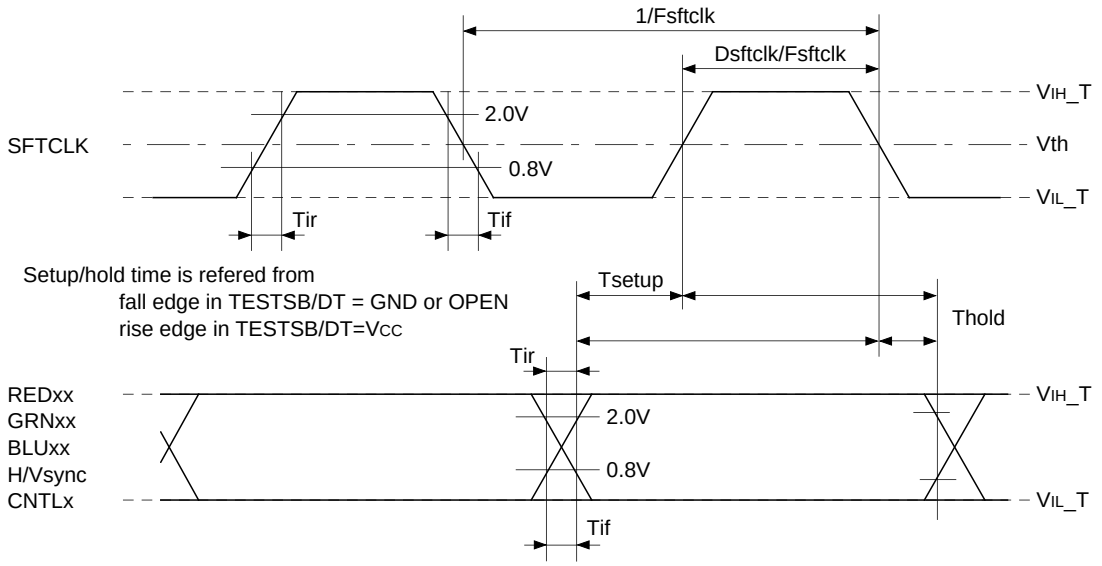


Fig. 4. TTL input timing

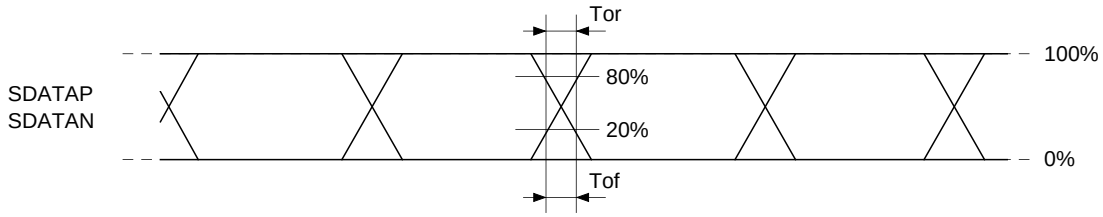


Fig. 5. Serial output timing

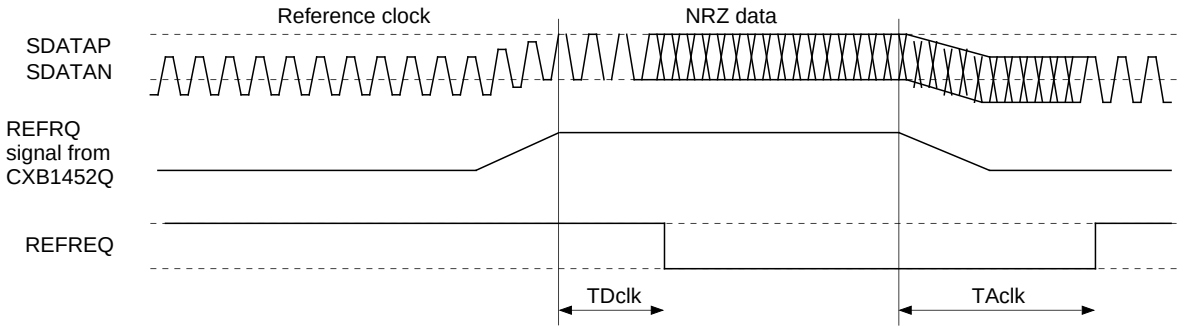


Fig. 6. Refclk request timing

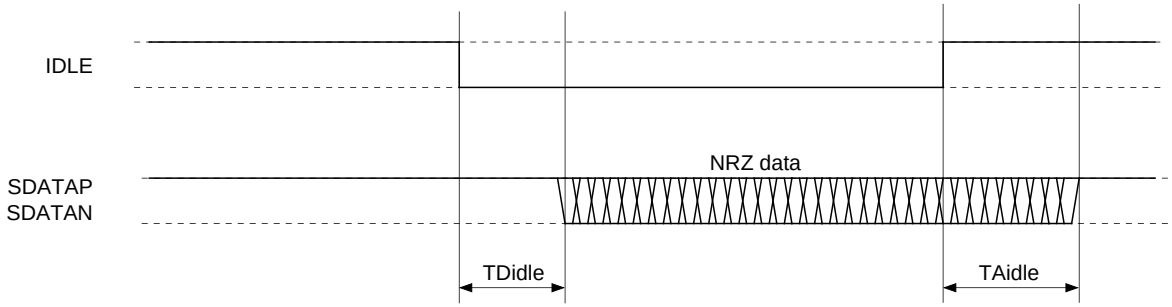


Fig. 7. Idle mode timing

Operation mode

CXB1451Q supports 3 panel mode and 2 clock mode switched by the PANEL (1, 0) and CKMODE pin according to the Tab. 5 & 6. The supporting clock rate are summarized in Tab. 7. These pins are open High TTL inputs.

Tab. 5. Panel Mode select

PANEL1	PANEL0	Supporting panel size & color
L	L	VGA (640 × 480) 18bit color
L	H	SVGA (800 × 600) 18bit color
H	L	XGA (1024 × 768) 18bit color
H	H	not supported

Tab. 6. Clock Mode select

CKMODE	Supporting clock mode
L	2 pixel/ShiftClock (2ppc)
H	1 pixel/ShiftClock (1ppc)

Tab. 7. Operation Mode

Panel Mode	Clock Mode	Color	Shift Clock	Dot Clock	Serial rate
VGA	1 pixel/SftClk	18bit	25MHz	25MHz	600Mbps
	2 pixel/SftClk	18bit	12.5MHz	25MHz	600Mbps
SVGA	1 pixel/SftClk	18bit	40MHz	40MHz	960Mbps
	2 pixel/SftClk	18bit	20MHz	40MHz	960Mbps
XGA	1 pixel/SftClk	18bit	65MHz	65MHz	1560Mbps
	2 pixel/SftClk	18bit	32.5MHz	65MHz	1560Mbps

TESTSB/TESTDT pins select the trigger edge of SFTCLK and test mode according to Tab. 8.

Tab. 8. SFTCLK polarity & TEST mode

		TESTSB		
		GND	OPEN	V_{CC}
TESTDT	GND	Transmitter operation trigger = falling edge		Fabricator reserved TEST mode
	OPEN			
	V_{CC}	SDATAP = H SDATAN = L	SDATAP = L SDATAN = H	Trigger = rising edge

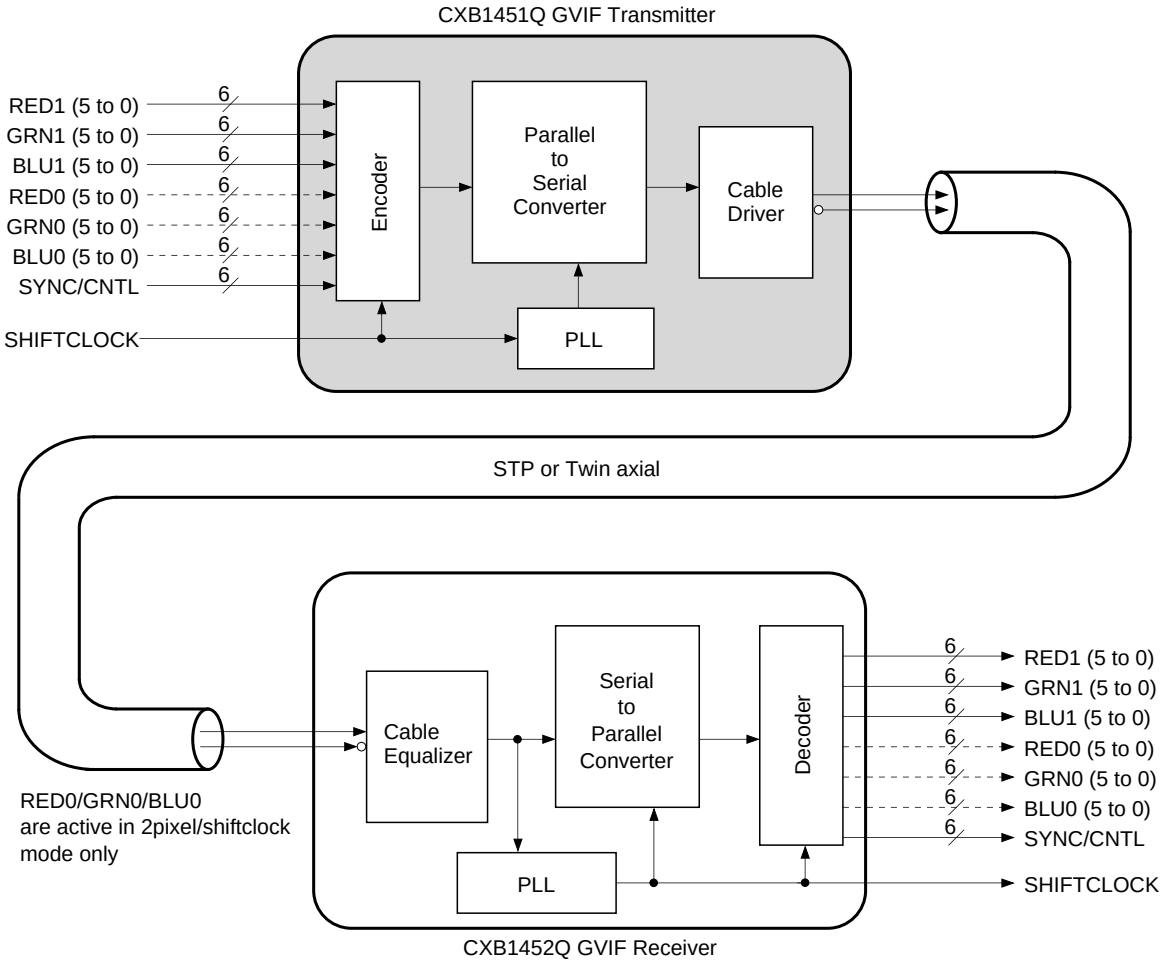
IDLE pin disable differential signal transmission from SDATAP/N pins. It's open High TTL input. Transmission is disabled when IDLE = High.

Applications

CXB1451Q GVIF transmitter is applied to the digital RGB signal transmittion for

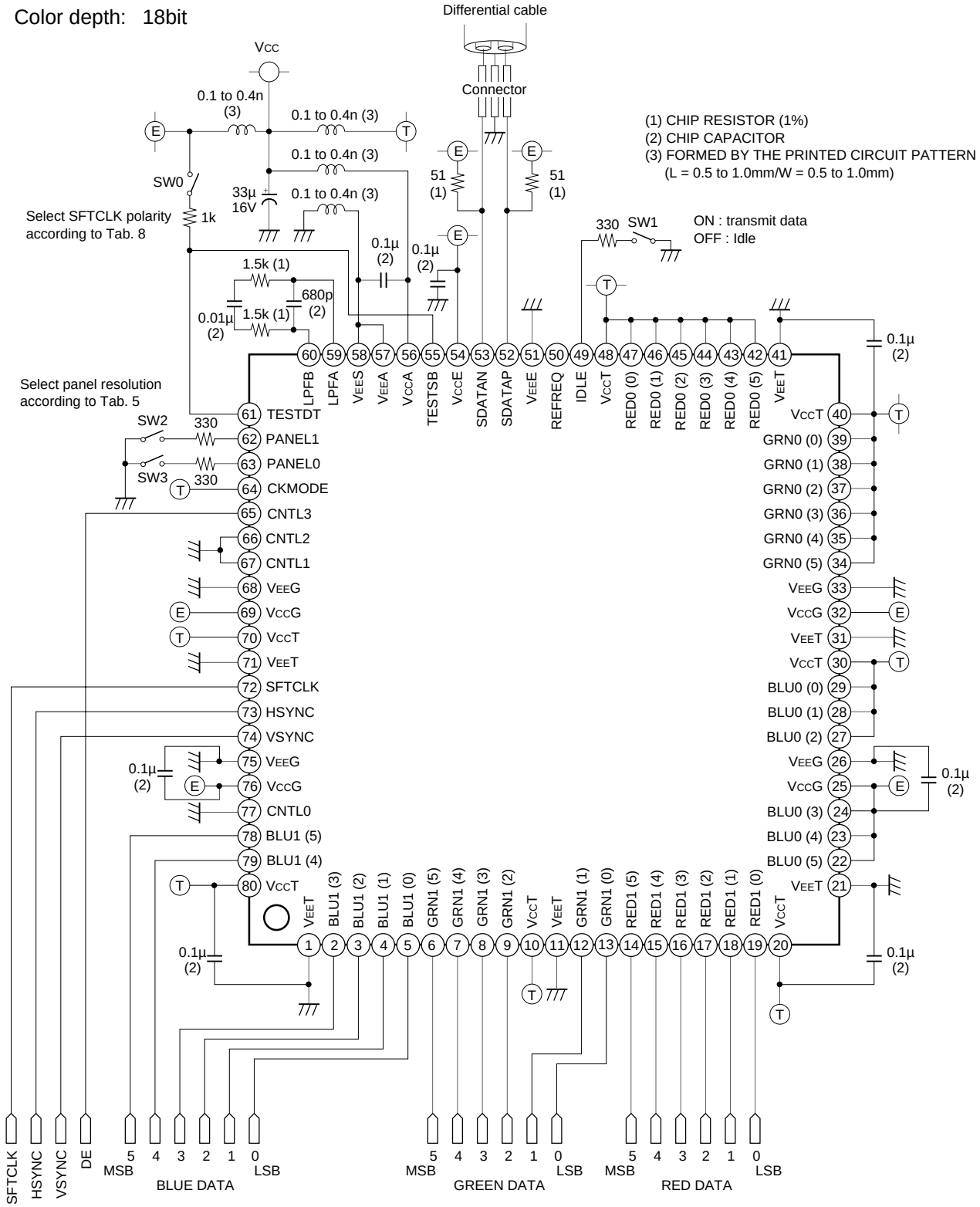
P/C with LCD monitor
Video on demand system
Monitoring system
Graphical controller
Projector
Digital TV monitor

with GVIF receiver, CXB1452Q.



Application Cicuit (A)

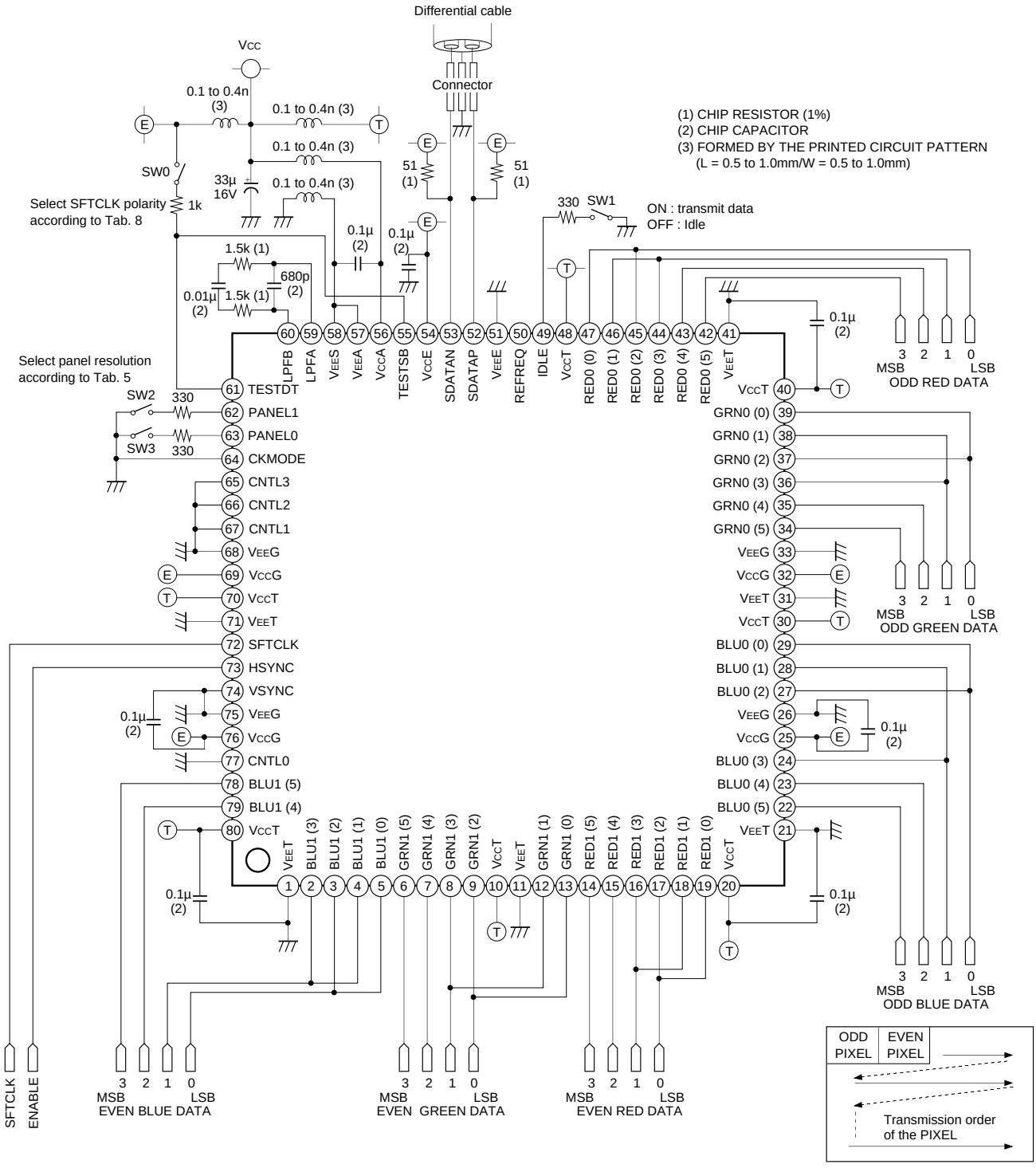
Clock mode: 1 pixel/sftclk (1ppc)
Picture sync: H/V sync & DE
Color depth: 18bit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Cicuit (B)

Clock mode: 2 pixel/sftclk
Picture sync: ENABLE only
Color depth: 12bit



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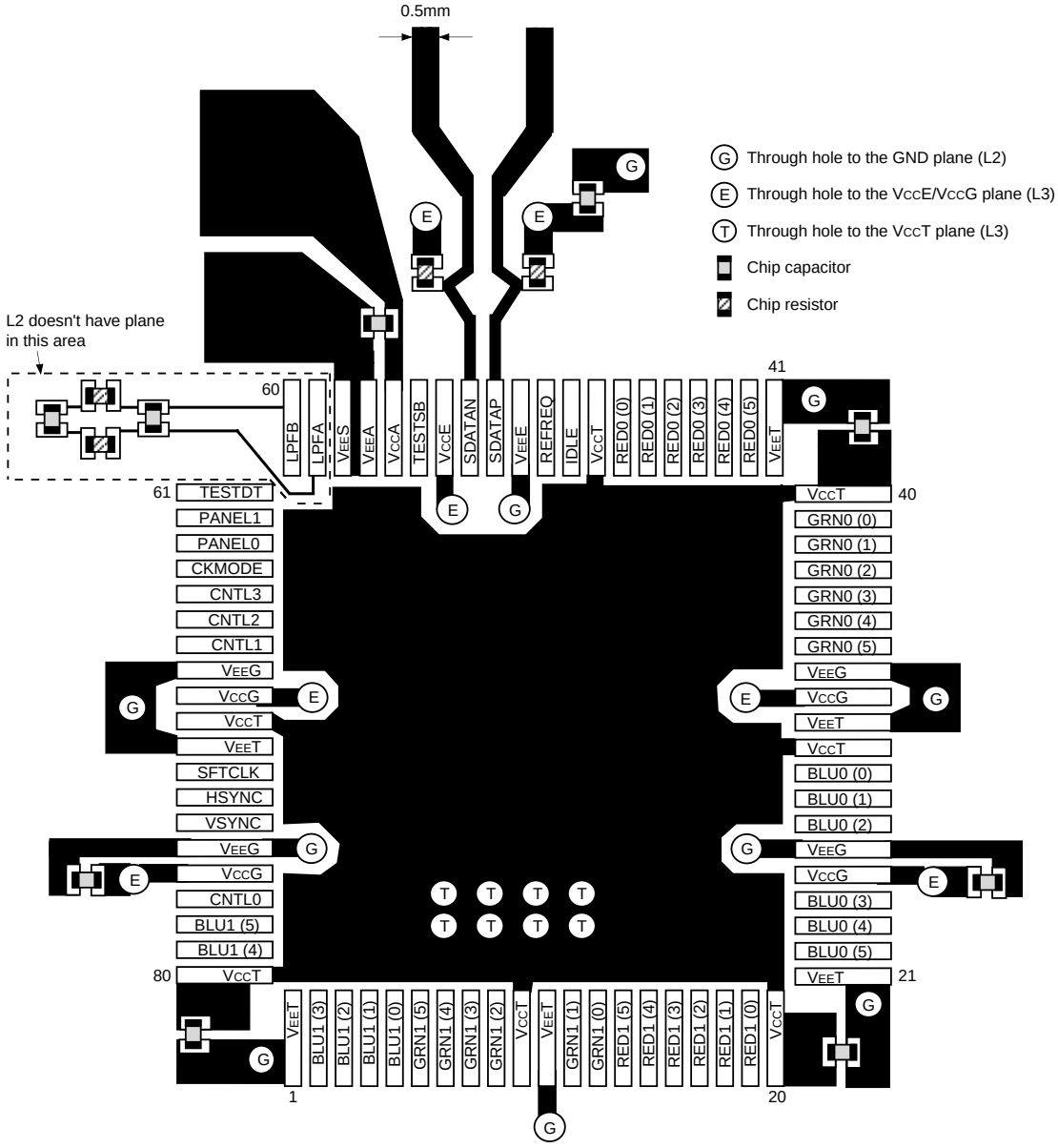
Recommended Printed Circuit Board Structure

L1: Cu plate (18µm) + solder coat
I1: Adhesive Sheet (0.3mm ± 0.09mm)
L2: Cu plate (36µm)
I2: Fiber-glass epoxy core (0.8mm)
L3: Cu plate (36µm)
I3: Adhesive Sheet (0.3mm)
L4: Cu plate (18µm) + solder coat

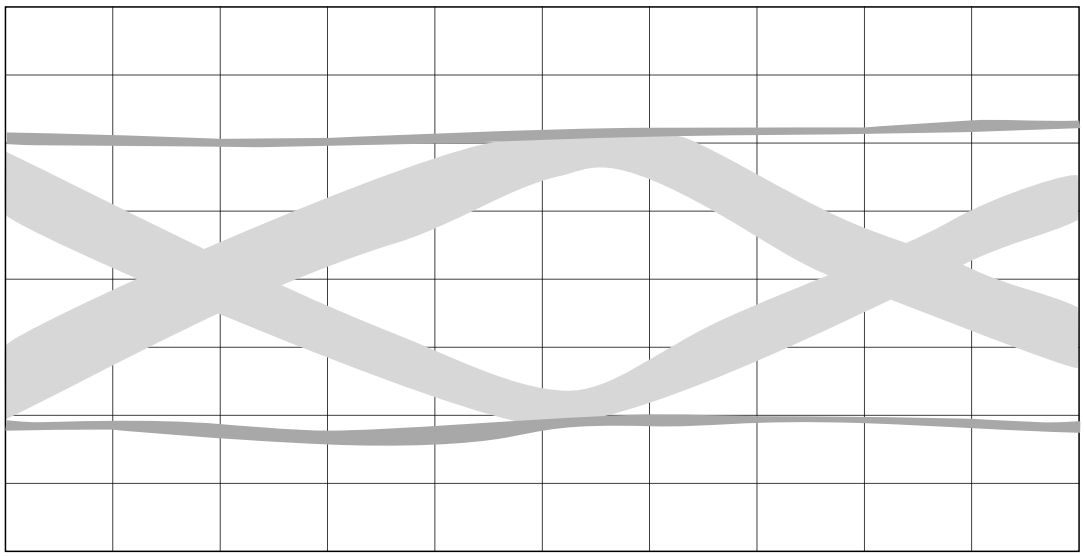
Recommended Printed Circuit Board Pattern

SDATAP/SDATAN pins to the connector path W = 0.50mm (Z0 = 50Ω)
other path W = 0.25mm

POWER and special signal routing example



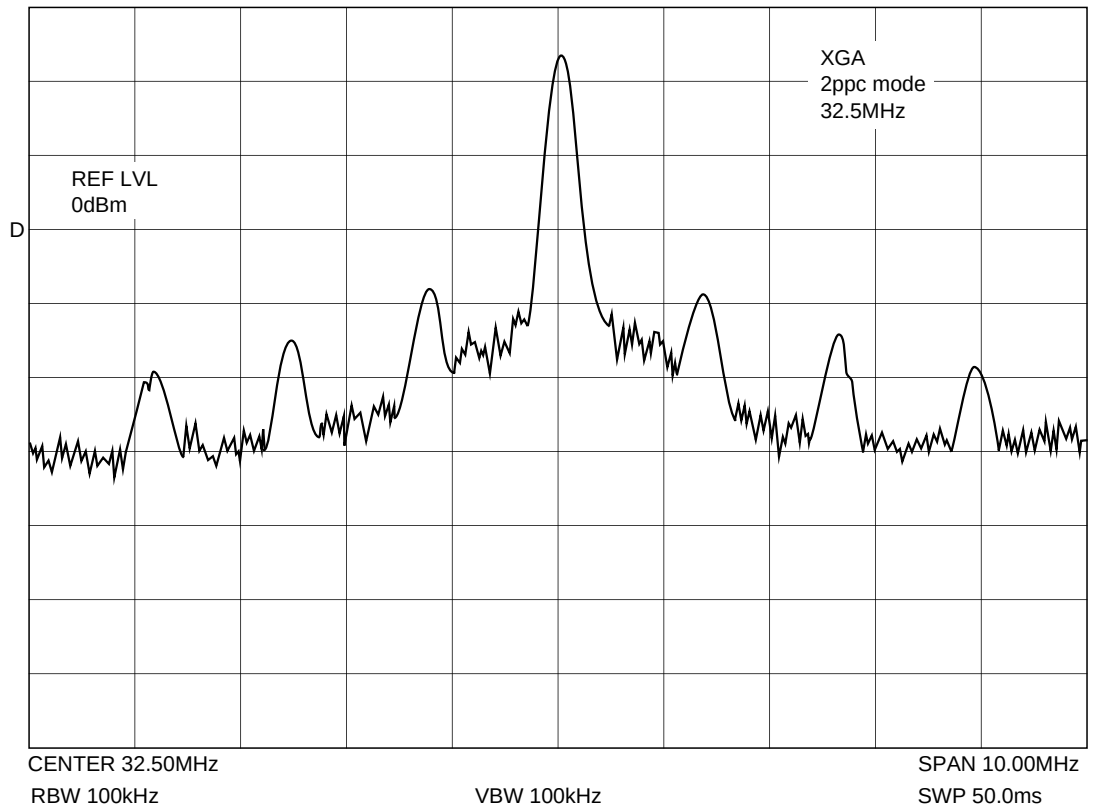
1.56Gb/s SDATAP Output waveform



Ch. 1 = 100.0mVolts/div
Timebase = 100ps/div

Offset = –92.00mVolts
Delay = 40.6820ns

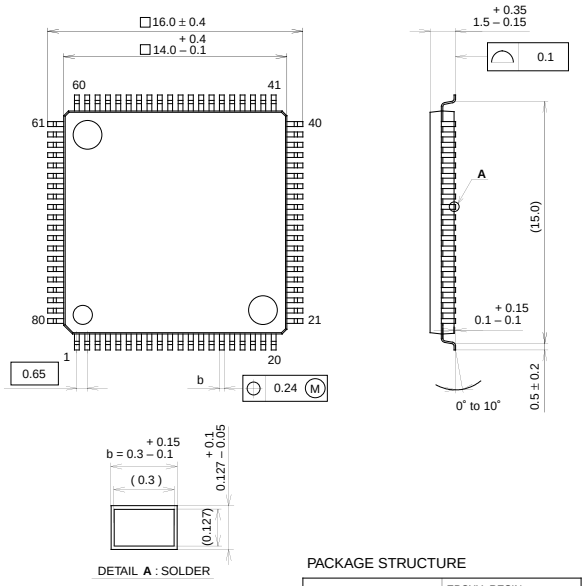
SFTCLK Jitter tolerance: example power spectrum available for transmission



Package Outline

Unit: mm

80PIN QFP (PLASTIC)



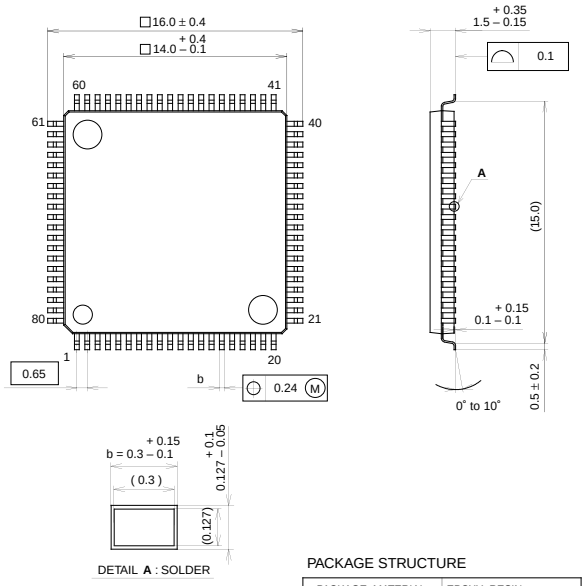
SONY CODE	QFP-80P-L03
EIAJ CODE	P-QFP80-14x14-0.65
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE MASS	0.6g

Kokubu Ass'y

80PIN QFP (PLASTIC)



SONY CODE	QFP-80P-L03
EIAJ CODE	P-QFP80-14x14-0.65
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE MASS	0.6g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	42 ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm