Features

- **Organized as 2M x 8 bits**
- **Single 3.3V Power Supply**
- **Stacks of 16 SRAM 128K x 865609E Die**
- **Access Time: 40 ns**
- **Very Low Power Consumption**
  - **Active: 100 mW (Typ)**
  - **Standby: 1 mW (Typ)**
- **TTL-Compatible Inputs and Outputs**
- **Die Designed on 0.35 Micron Process**
- **Latch-up Immune**
- **100 Krads (TM1019.5)**
- **Wide Temperature Range 55°C to +125°C**
- **Built and Tested by 3D+, using 3D+ Die Stacking Technology**

Description

The AT61162E is a Rad Tolerant module, highly-integrated and very low-power CMOS static RAM organized as 2M x 8 bits. It is organized with 16 banks of 1 Mbit. Each bank has a 8-bit interface and is selected with 16 specific $\overline{CS}$: 0 - 15. Banks are selectable by pairs with 8 specific BS: 0 - 7.

This module takes full benefit of the 3D+ cube technology, and it is assembled and tested by 3D+, using Atmel 65609E 1-Mbit SRAM die: it is built with 8 layers, each one housing 2 dies. 10 nF decoupling capacitors are embedded for each memory die.

This module brings the solution to applications where fast computing is as mandatory as low power consumption, for example: space electronics, portable instruments, or embarked systems.

AT61162E is processed according to the methods of the latest revision of the MIL PRF 38535, QML N (QML Q counterpart for plastic).

The package is a 64 gull wing pins dual in line, 11 mm wide, 28 mm long and 14.3 mm height and 0.8 mm pin pitch.

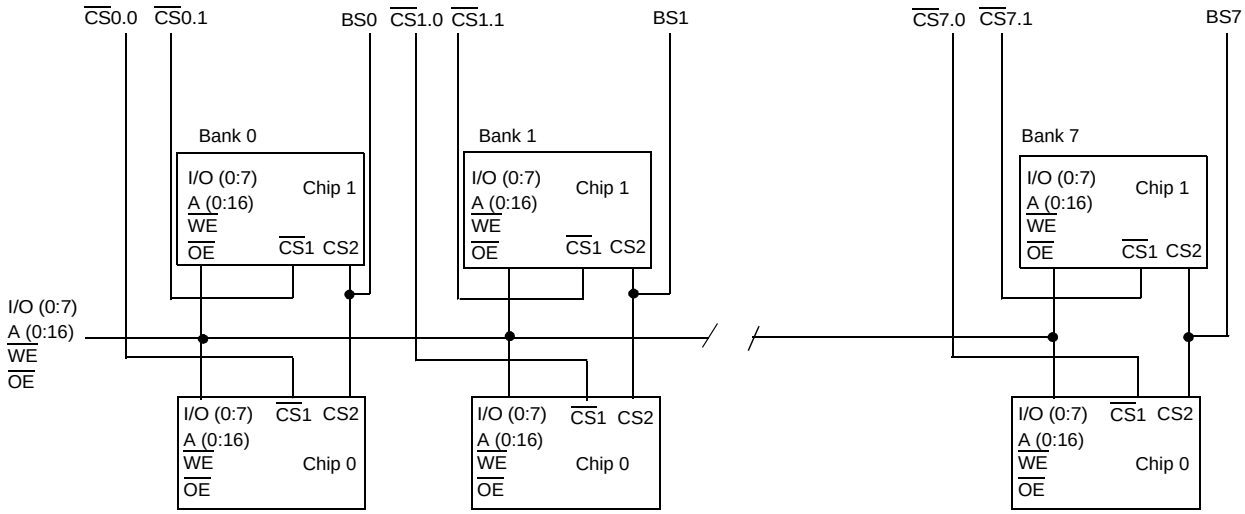
Rad Hard 2-Mbit x 8 SRAM Cube

AT61162E

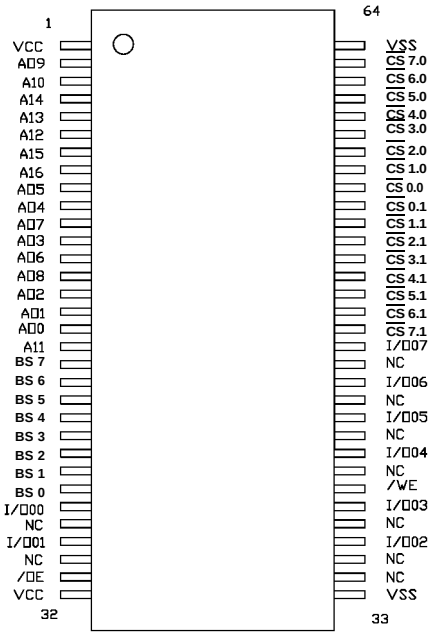
Preliminary

Rev. 4157C–AERO–06/03

Block Diagram



Pin Configuration



Pin Description

Pin Name	Function
AO - A16	Address Inputs
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CS}$ 0.0 - $\overline{CS}$ 7.1	Chip Select 1
BS0 - BS7	Chip Select 2
I/O0 - I/O7	Data Inputs/Outputs
V_{CC}	3.3V Power
GND	Ground
NC	No Connection

Truth Table

$\overline{CS}_{x.x}$	BS_x	$\overline{WE}$	$\overline{OE}$	Inputs/ Outputs	Mode
All $\overline{CS}$ H	–	–	–	Z	Deselect/ Power-down
–	All BS L	–	–	Z	Deselect/ Power-down
$\overline{CS}$ y.z: L Other $\overline{CS}$: H	BSy: H Other BS: –	H	L	Data out	Read (Bank y.z selected)
$\overline{CS}$ y.z: L $\overline{CS}$ y.z: H Other $\overline{CS}$: –	BSy: H Other BS: L				
$\overline{CS}$ y.z: L Other $\overline{CS}$: H	BSy: H Other BS: –	L	–	Data in	Write (Bank y.z selected)
$\overline{CS}$ y.z: L $\overline{CS}$ y.z: H Other $\overline{CS}$: –	BSy: H Other BS: L				
$\overline{CS}$ y.z: L Other $\overline{CS}$: H	BSy: H Other BS: –	H	H	Z	Output Disable
$\overline{CS}$ y.z: L $\overline{CS}$ y.z: H Other $\overline{CS}$: –	BSy: H Other BS: L				

Electrical Characteristics

Absolute Maximum Ratings*

Supply Voltage to GND Potential	0.5 to +5V
DC Input Voltage GND	GND -0.3 to V_{CC}0.3V
DC Output Voltage high-Z-State GND	GND -0.3 to V_{CC}+0.3V
Storage Temperature	-65 to +150°C
Output Current into Outputs (Low)	20 mA
Electro Statics Discharge Voltage (MIL STD 883D method 3015.3)	>1500V

*Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Range

	Operating Temperature	Operating Voltage
Military	-55°C to 125°C	3.3V ± 0.3V

Recommended DC Operating Conditions

Parameter	Description	Min	Typ	Max	Units
V_{CC}	Supply Voltage	3	3.3	3.6	V
Gnd	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	-	V_{CC}+0.3	V
V_{IL}	Input Low Voltage	GND-0.3	0.0	0.8	V

Capacitance

Parameter	Description	Min	Typ	Max	Unit
C_{IN}[1]	Input Low Voltage	-	-	8	pF
C_{OUT}[1]	Output High Voltage	-	-	8	pF

Note: 1. Guaranteed but not tested.

DC Parameters

Parameter	Description	Min	Typ	Max	Unit
I_{IX} (1)	Input Leakage Current	-16	-	16	µA
I_{OZ} (1)	Output Leakage Current	-16	-	16	µA
V_{OL} (2)	Output Low Voltage	-	-	0.4	V
V_{OH} (3)	Output High Voltage	2.4	-	-	V

1. Gnd < V_{IN} < V_{CC}, Gnd < V_{OUT} < V_{CC} Output Disabled.
2. V_{CC} min. IOL = 1 mA.
3. V_{CC} min. IOH = -0.5 mA.

Consumption

Symbol	Description	61162E-35	Unit	Value
ICCSB (1)	Standby Supply Current	40	mA	max
$ICCSB_1$ (2)	Standby Supply Current	32	mA	max
ICCOP (3)	Dynamic Operating Current	90	mA	max

1. $\overline{CS}_{0.0}$ - $\overline{CS}_{7.1} \geq V_{IH}$ or BS_0 - BS7 $\leq V_{IL}$ and $\overline{CS}_{0.0}$ - $\overline{CS}_{7.1} \leq V_{IL}$.
2. $\overline{CS}_{0.0} \geq V_{CC}$ - 0.3V or, BS_0 - BS7 < Gnd + 0.3V and $\overline{CS}_{0.0}$ - $\overline{CS}_{7.1} \leq 0.2V$
3. One bank active ($F = 1/T_{AVAV}$, I_{OUT} = 0 mA, $\overline{W} = \overline{OE} = V_{IH}$, V_{IN} = Gnd/V_{CC}, V_{CC} max.), other banks stand by TTL (note 1) or CMOS (note 2).

Write Cycle

Symbol	Parameter	61162E-40	Unit	Value
t_{AVAW}	Write cycle time	40	ns	min
t_{AVWL}	Address set-up time	0	ns	min
t_{AVWH}	Address valid to end of write	35	ns	min
t_{DVWH}	Data set-up time	35	ns	min
t_{E1LWH}	$\overline{CS}_1$ low to write end	35	ns	min
t_{E2HWH}	CS_2 high to write end	35	ns	min
t_{WLQZ}	Write low to high-Z (1)	20	ns	max
t_{WLWH}	Write pulse width	35	ns	min
t_{WHAX}	Address hold from to end of write	+3	ns	min
t_{WHDX}	Data hold time	0	ns	min
t_{WHQX}	Write high to low-Z (1)	0	ns	min

Note: 1. Parameters guaranteed, not tested, with output loading 5 pF (see 1b in Figure: AC Test Loads Waveforms).

Read Cycle

Symbol	Parameter	61162E-40	Unit	Value
t_{AVAV}	Read cycle time	40	ns	min
t_{AVQV}	Address access time	40	ns	max
t_{AVQX}	Address valid to low-Z	3	ns	min
t_{E1LQV}	Chip-select$_1$ access time	40	ns	max
t_{E1LQX}	$\overline{CS}_1$ low to low-Z (1)	3	ns	min
t_{E1HQZ}	$\overline{CS}_1$ high to high-Z (1)	20	ns	max
t_{E2HQV}	Chip-select$_2$ access time	40	ns	max
t_{E2HQX}	CS_2 high to low-Z (1)	3	ns	min
t_{E2LQZ}	CS_2 low to high-Z (1)	20	ns	max
t_{GLQV}	Output Enable access time	15	ns	max
t_{GLQX}	$\overline{OE}$ low to low-Z (1)	0	ns	min
t_{GHQZ}	$\overline{OE}$ high to high-Z (1)	10	ns	max

Note: 1. Parameters guaranteed, not tested, with output loading 5 pF (see 1b in page Figure: AC Test Loads Waveforms).

AC Parameters

AC Test Conditions

Input Pulse Levels: ..... GND to 3.0V

Input Rise/Fall Times: ..... 5 ns

Input Timing Reference Levels: 1.5V

Output Loading I_{OL}/I_{OH} (see figures 1a and 1b)..... +30 pF

AC Test Loads Waveforms

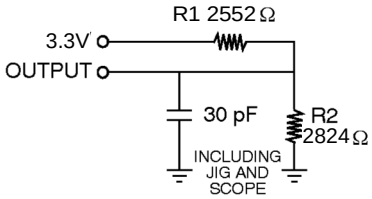


Figure 1a

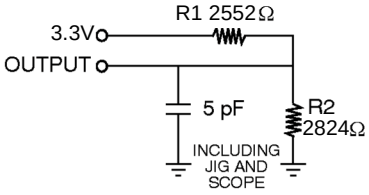


Figure 1b

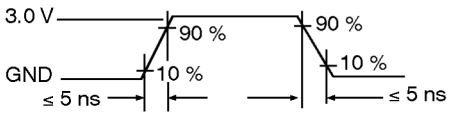
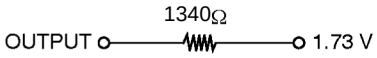


Figure 2

Equivalent to : THEVENIN EQUIVALENT

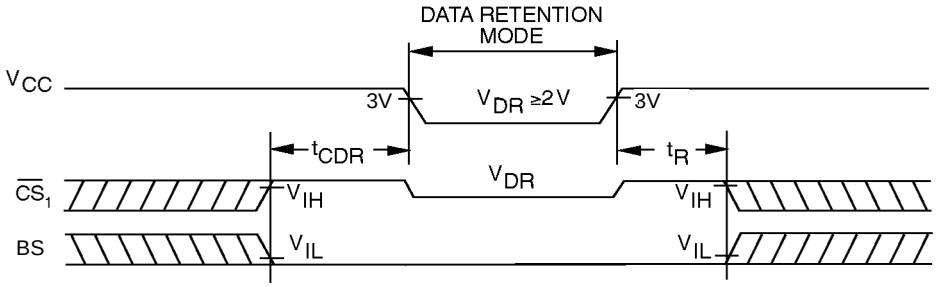


Data Retention Mode

Atmel CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules ensure data retention:

1. During data retention $\overline{CS}$ must be held high within V_{CC} to V_{CC} -0.2V or, chip select BS must be held down within GND to GND +0.2V.
2. Output Enable ($\overline{OE}$) should be held high to keep the RAM outputs high impedance, minimizing power dissipation.
3. During power up and power down transitions $\overline{CS}$ and $\overline{OE}$ must be kept between V_{CC} + 0.3V and 70% of V_{CC}, or with BS between GND and GND -0.3V.
4. The RAM can begin operation > TR ns after V_{CC} reaches the minimum operation voltages (3V).

Timing



Data Retention Characteristics

Parameter	Description	Min	Typical T_A = 25°C	Max	Unit
V_{CCDR}	V_{CC} for data retention	2.0	–	–	V
t_{CDR}	Chip deselect to data retention time	0.0	–	–	ns
t_R	Operation recovery time	t_{AVAV}(1)	–	–	ns
I_{CCDR1}(2)	Data retention current at 2.0V	–	0.160	16	mA

Notes: 1. T_{AVAV} = Read Cycle Time

2. All $\overline{CS}$ = V_{CC} or All BS = $\overline{CS}$ = GND, V_{IN} = Gnd/V_{CC}.

Figure 1. Write Cycle 1. $\overline{W}$ Controlled, $\overline{OE}$ High During Write

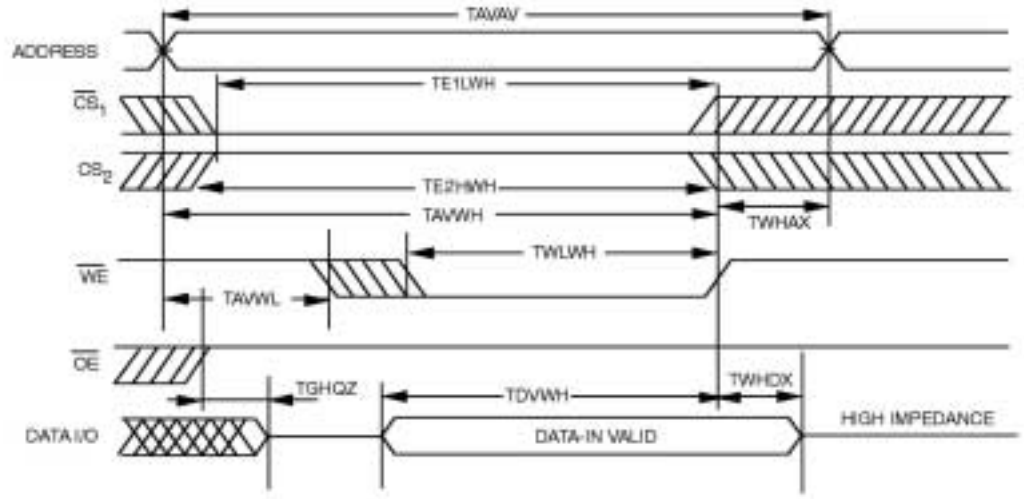


Figure 2. Write Cycle 2. $\overline{W}$ Controlled, $\overline{OE}$ Low

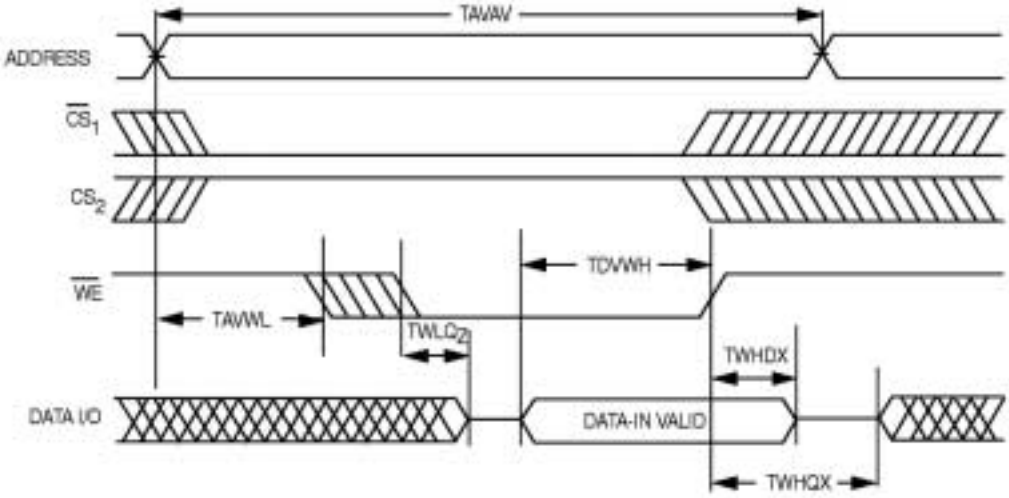
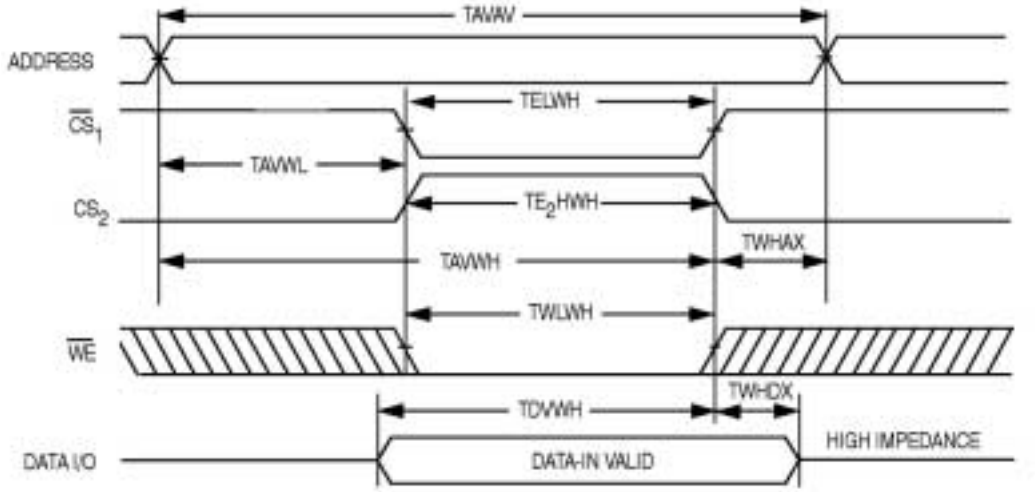


Figure 3. Write Cycle 3. $\overline{CS}1$ or CS2 Controlled



Note: The internal write time of the memory is defined by the overlap of CS_1 Low and CS_2 HIGH and $\overline{WE}$ LOW. Both signals must be activated to initiate a write and either signal can terminate a write by going in actived. The data input setup and hold timing should be referenced to the activated edge of the signal that terminates the write. Data out is high impedance if $\overline{OE} = V_{IH}$.

Figure 4. Read Cycle nb 1

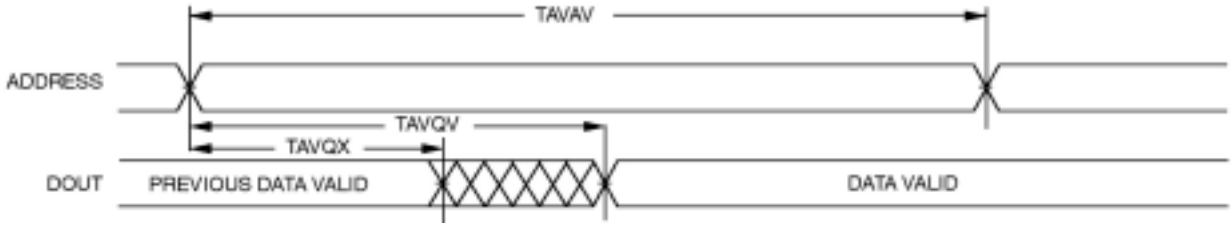


Figure 5. Read Cycle nb 2

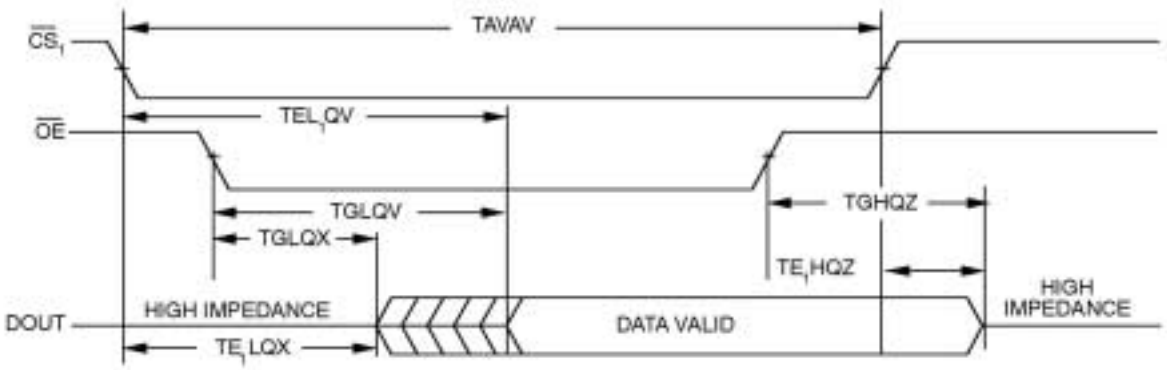
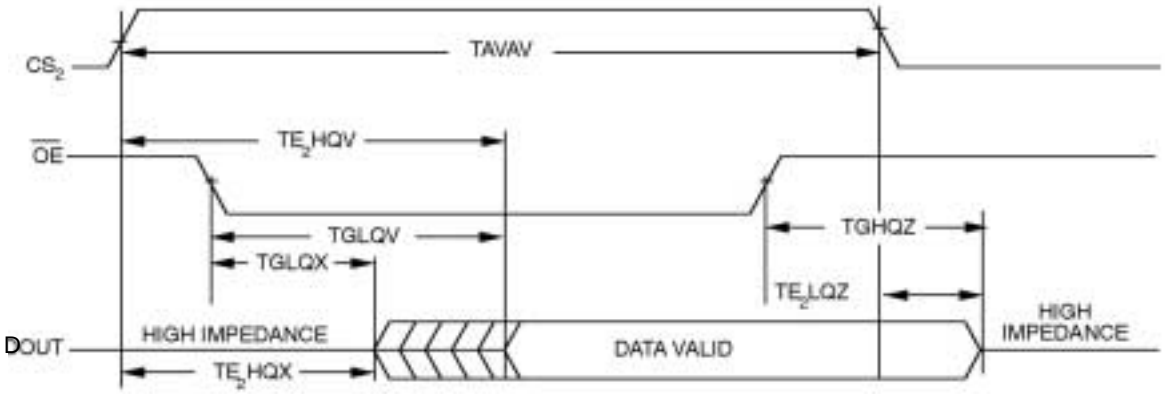


Figure 6. Read Cycle nb 3



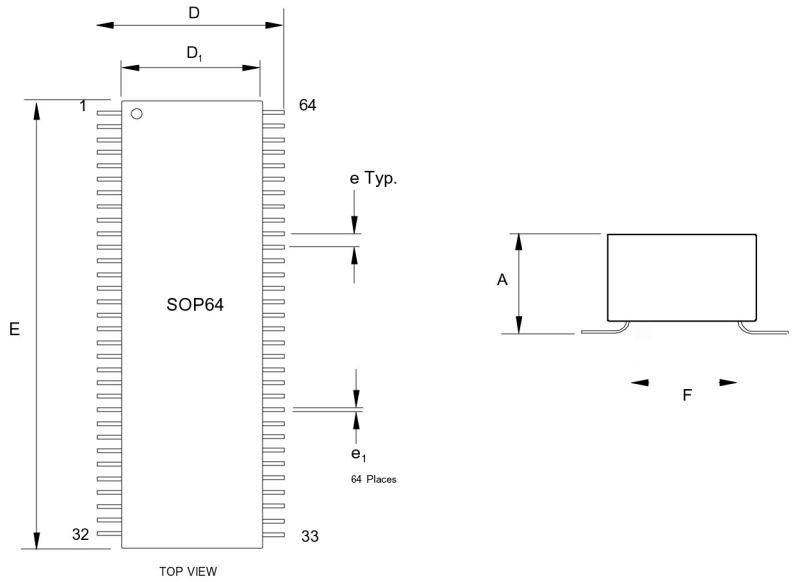
Test Tools

Supplier	Reference Number
ENPLAS	OTS - 64 - 0.8 - 04

Ordering Information

Reference Number	Temperature Range	Speed	Package	Quality Flow
AT61162E-PM40MMN	-55 to +125°C	40 ns	Cube 64 pins	QML N
AT61162E-PM40M-E	25°C	40 ns	Cube 64 pins	Engineering Samples

Package Drawing



Dimensions (mm)	Min	Max
A	14.0	14.60
D	13.60	13.80
D1	10.75	11.15
E	27.80	28.20
F	7.5	
e	0.80	
e1	0.35	

Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

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