



2Mx8 MONOLITHIC FLASH *ADVANCED**

FEATURES

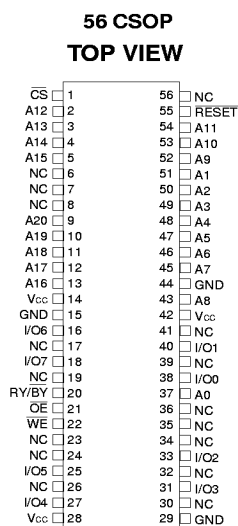
- Access Times of 90, 120, 150nS
- Packaging:
 - 56 lead, Hermetic Ceramic, 0.520" CSOP (Package 207). Fits standard 56 SSOP footprint.
- Sector Architecture
 - 32 equal size sectors of 64KBytes each
 - Any combination of sectors can be erased. Also supports full chip erase.
- 100,000 Write/Erase Cycles Minimum (0°C to 70°)
- Organized as 2Mx8
- Commercial, Industrial, and Military Temperature Ranges

- 5 Volt Read and Write. 5V ± 10% Supply.
- Low Power CMOS
- Data Polling and Toggle Bit feature for detection of program or erase cycle completion.
- Supports reading or programming data to a sector not being erased.
- RESET pin resets internal state machine to the read mode.
- Multiple Ground Pins for Low Noise Operation

** This data sheet describes a product that may or may not be under development, and is subject to change or cancellation without notice.*

Note: Programming information available upon request.

FIG. 1 PIN CONFIGURATION FOR WMF2M8-XOPX5



PIN DESCRIPTION

I/O0-7	Data Inputs/Outputs
A0-20	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
Vcc	Power Supply
GND	Ground
RY/BY	Ready/Busy
RESET	Reset

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Ratings	Unit
Voltage on Any Pin Relative to Vss	V _T	-2.0 to +7.0	V
Power Dissipation	P _T	8	W
Storage Temperature	T _{stg}	-65 to +125	°C
Short Circuit Output Current	I _{os}	100	mA

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.0	-	V _{CC} + 0.5	V
Input Low Voltage	V _{IL}	-0.5	-	+0.8	V
Operating Temperature (Mil.)	T _A	-55	-	+125	°C
Operating Temperature (Ind.)	T _A	-40	-	+85	°C

CAPACITANCE(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
Address Input capacitance	C _{AD}	V _{I/O} = 0 V, f = 1.0 MHz	9	pF
Output Enable capacitance	C _{OE}	V _{IN} = 0 V, f = 1.0 MHz	9	pF
Write Enable capacitance	C _{WE}	V _{IN} = 0 V, f = 1.0 MHz	9	pF
Chip Select capacitance	C _{CS}	V _{IN} = 0 V, f = 1.0 MHz	9	pF
Data I/O capacitance	C _{I/O}	V _{I/O} = 0 V, f = 1.0 MHz	12	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS - CMOS COMPATIBLE(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10	μA
Output Leakage Current	I _{LO}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10	μA
V _{CC} Active Current for Read (1)	I _{CC1}	$\overline{CS} = V_{IL}, \overline{OE} = V_{IH}, f = 5\text{MHz}$		40	mA
V _{CC} Active Current for Program or Erase (2)	I _{CC2}	$\overline{CS} = V_{IL}, \overline{OE} = V_{IH}$		60	mA
V _{CC} Standby Current	I _{CC3}	V _{CC} = 5.5, $\overline{CS} = V_{IH}, f = 5\text{MHz}, \overline{RESET} = V_{CC} \pm 0.3V$		0.25	mA
Output Low Voltage	V _{OL}	I _{OL} = 12.0 mA, V _{CC} = 4.5		0.45	V
Output High Voltage	V _{OH}	I _{OH} = -2.5 mA, V _{CC} = 4.5	0.85xV _{CC}		V
Low V _{CC} Lock-Out Voltage	V _{LKO}		3.2	4.2	V

NOTES:

1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (@ 5MHz). The frequency component typically is less than 2mA/MHz, with $\overline{OE}$ at V_{IH}.
2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
3. DC test conditions V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V


AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS - $\overline{WE}$ CONTROLLED

(V_{CC} = 5.0V, T_A = -55°C to +125°C)

Parameter	Symbol		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{AVAV}	t _{WC}	90		120		150		nS
Chip Select Setup Time	t _{ELWL}	t _{CS}	0		0		0		nS
Write Enable Pulse Width	t _{WLWH}	t _{WP}	45		50		50		nS
Address Setup Time	t _{AVWL}	t _{AS}	0		0		0		nS
Data Setup Time	t _{DVWH}	t _{DS}	45		50		50		nS
Data Hold Time	t _{WHDX}	t _{DH}	0		0		0		nS
Address Hold Time	t _{WLAX}	t _{AH}	45		50		50		nS
Write Enable Pulse Width High	t _{WHWL}	t _{WPH}	20		20		20		nS
Duration of Byte Programming Operation	t _{WHWH1}			1		1		1	mS
Sector Erase	t _{WHWH2}			15		15		15	Sec
Read Recovery Time before Write	t _{GHWL}		0		0		0		μS
V _{CC} Setup Time	t _{VCS}		50		50		50		μS
Chip Programming Time				100		100		100	Sec
Output Enable Hold Time (1)		t _{OEHL}	10		10		10		nS
Chip Erase Time				480		480		480	Sec
RESET Pulse Width		t _{RP}	500		500		500		nS

1. For Toggle and Data Polling.

AC CHARACTERISTICS – READ-ONLY OPERATIONS

(V_{CC} = 5.0V, T_A = -55°C to +125°C)

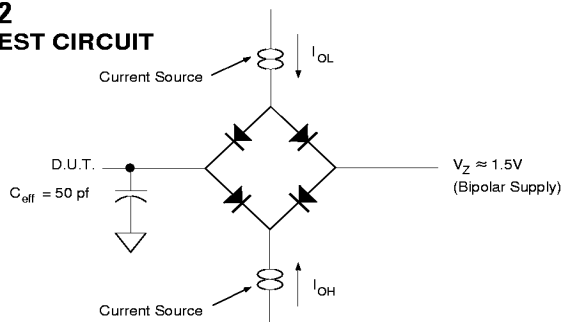
Parameter	Symbol		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{AVAV}	t _{RC}	90		120		150		nS
Address Access Time	t _{AVQV}	t _{ACC}		90		120		150	nS
Chip Select Access Time	t _{ELQV}	t _{CE}		90		120		150	nS
Output Enable to Output Valid	t _{GLQV}	t _{OE}		40		50		55	nS
Chip Select High to Output High Z (1)	t _{EHQZ}	t _{DF}		20		30		35	nS
Output Enable High to Output High Z (1)	t _{GHQZ}	t _{DF}		20		30		35	nS
Output Hold from Addresses, $\overline{CS}$ or $\overline{OE}$ Change, whichever is First	t _{AXQX}	t _{OH}	0		0		0		nS
RESET Low to Read Mode (1)		t _{Ready}		20		20		20	μS

1. Guaranteed by design, not tested.

**AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, $\overline{CS}$ CONTROLLED**(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol		<u>-90</u>		<u>-120</u>		<u>-150</u>		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{AVAV}	t _{WC}	90		120		150		nS
Write Enable Setup Time	t _{WLLEL}	t _{WS}	0		0		0		nS
Chip Select Pulse Width	t _{ELEH}	t _{CP}	45		50		50		nS
Address Setup Time	t _{AVEL}	t _{AS}	0		0		0		nS
Data Setup Time	t _{DVEH}	t _{DS}	45		50		50		nS
Data Hold Time	t _{EHDX}	t _{DH}	0		0		0		nS
Address Hold Time	t _{ELAX}	t _{AH}	45		50		50		nS
Chip Select Pulse Width High	t _{EHEL}	t _{CPH}	20		20		20		nS
Duration of Byte Programming Operation	t _{WHWH1}			1		1		1	mS
Sector Erase Time	t _{WHWH2}			15		15		15	Sec
Read Recovery Time	t _{GHLEL}		0		0		0		μS
Chip Programming Time				100		100		100	Sec
Chip Erase Time				480		480		480	Sec
Output Enable Hold Time (1)		t _{OEHL}	10		10		10		nS

1. For Toggle and Data Polling.

FIG. 2
AC TEST CIRCUIT**AC TEST CONDITIONS**

Parameter	Typ	Unit
Input Pulse Levels	V _{IL} = 0, V _{IH} = 3.0	V
Input Rise and Fall	5	nS
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z₀ = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

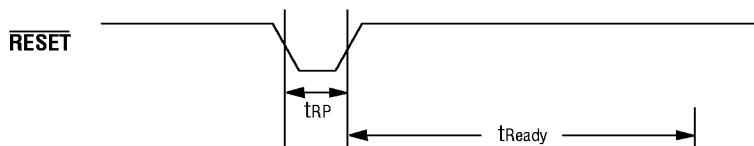
FIG. 3
RESET TIMING DIAGRAM



FIG. 4
AC WAVEFORMS FOR READ OPERATIONS

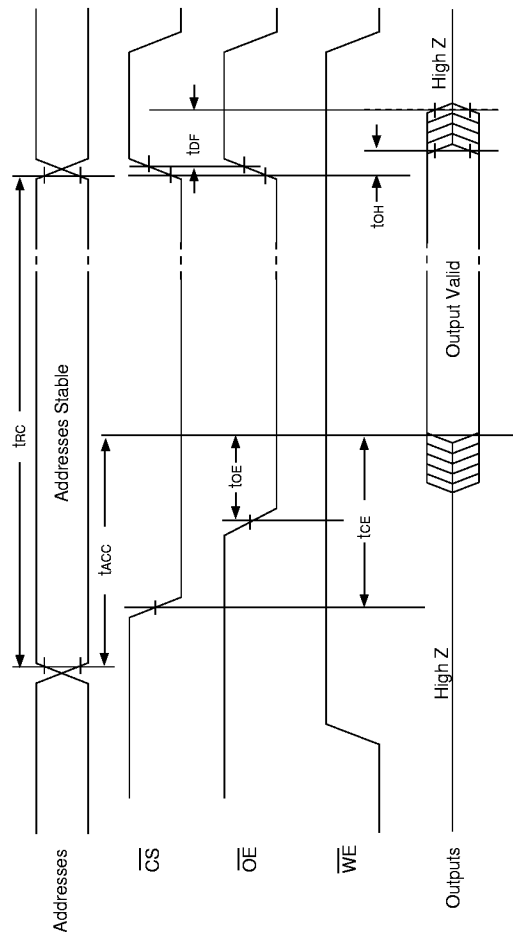
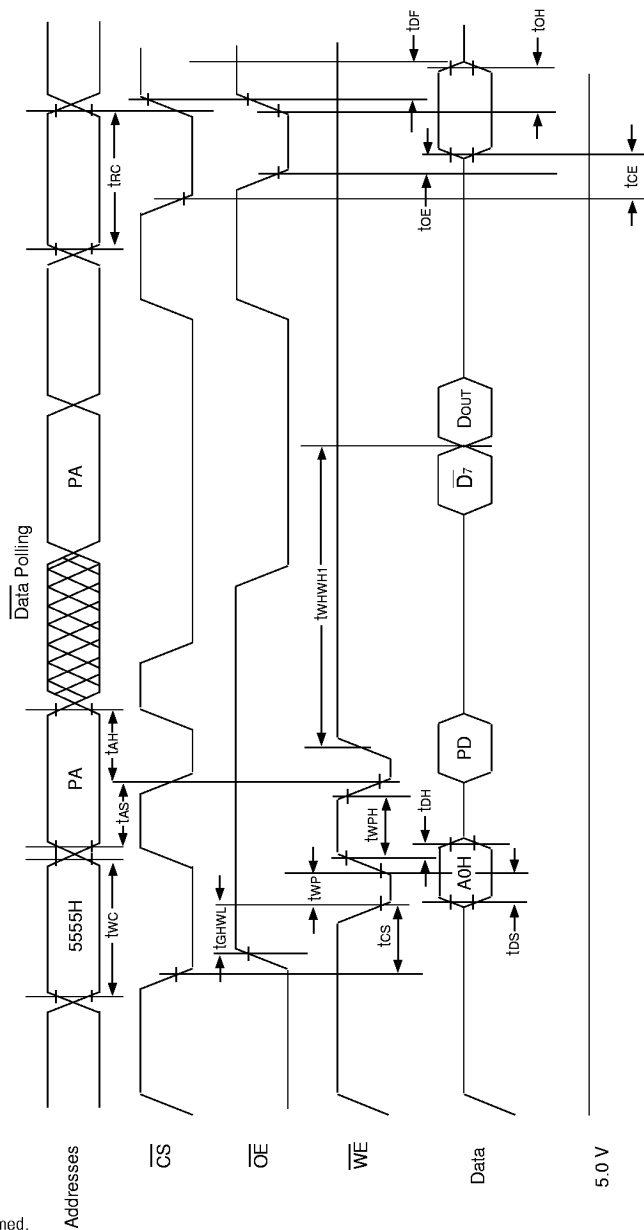




FIG. 5
WRITE/ERASE/PROGRAM
OPERATION, WE CONTROLLED

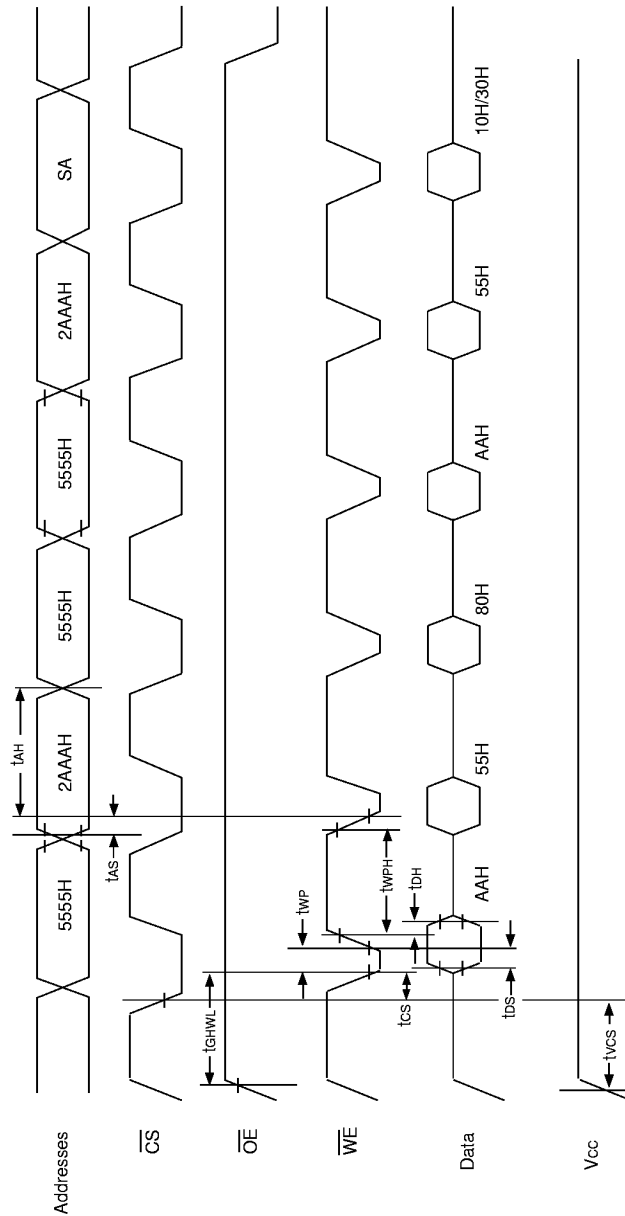


NOTES:

1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. $\overline{D_7}$ is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.



FIG. 6
AC WAVEFORMS CHIP/SECTOR
ERASE OPERATIONS

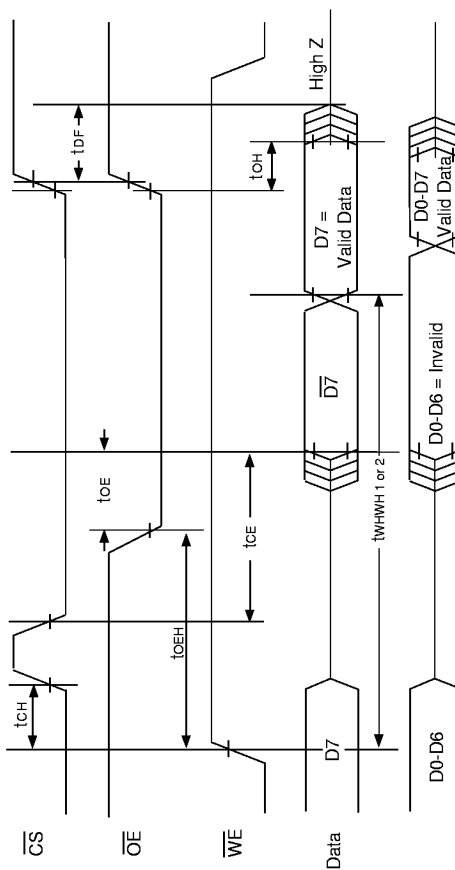


NOTE:

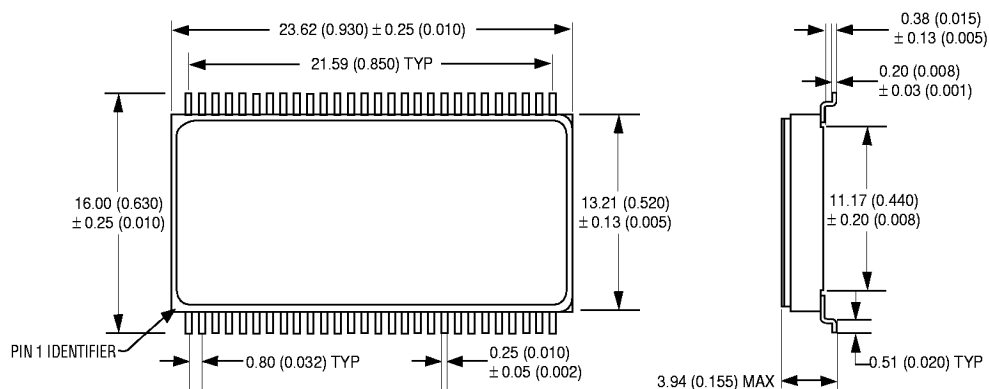
1. SA is the sector address for Sector Erase.



FIG. 7
AC WAVEFORMS FOR DATA POLLING
DURING EMBEDDED ALGORITHM OPERATIONS





**PACKAGE 207: 56 LEAD, CERAMIC SOP**

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION**W M F 2M8 - XXX X X 5****V_{PP} PROGRAMMING VOLTAGE**
5 = 5V**DEVICE GRADE:**

M = Military, 883 Screened -55°C to +125°C
I = Industrial -40°C to +85°C
C = Commercial 0°C to +70°C

PACKAGE TYPE:

OP = 56 Lead CSOP (Package 207)
fits standard 56 SSOP footprint

ACCESS TIME in nS**ORGANIZATION, 2M x 8****Flash PROM****MONOLITHIC****WHITE MICROELECTRONICS**