Introduction

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1.1 Library Description

SEC ASIC offers STDH90/MDL90 as 0.35µm CMOS standard cell libraries based on a completely new blended process. SEC's world-leading DRAM process is merged with a sophisticated 0.35µm cell-based logic process providing up to 4 layers of interconnect metal with various I/O pad–pitch options.

STDH90 and MDL90 use the same process. STDH90 can support up to three million gate count of logic providing 90% of usable gates with four layer metal. STDH90 is 40% faster than 0.5µm second generation library STD85. Logic density is 2.5 times greater than that of STD85. MDL90 consists of STDH90 and on-chip DRAMs. MDL90 adds up to 24Mbit of on-chip DRAM to the three million logic gates that STDH90 provides, truly delivering a system-on-a-chip solution.

A fully configurable memory compiler is available and datapath elements with up to 64 bit bus width are supported.

STDH90 I/O family features dual gate oxide process to support mixed-voltage designs without reducing reliability. These mixed-voltage designs interfaces between 5-volt and 3.3 volts.

To better support a system-on-a-chip design style, various core cells are available including processor cores like ARM7TDMI, 80C51 and Oak. The list of analog core cells includes ADC, DAC, CODEC and PLL.

The STDH90/MDL90 design kit supports Synopsys Design Compiler, VSS, Verilog-XL, Powerview, Mentor, Motive, Sunrise and IKOS. SEC design methodology offers a comprehensive timing solution including static timing analysis, floorplanning, RC extraction and delay calculation with very deep-submicron solutions from leading EDA vendors. For the latest status and details, please refer to the design kit release notes.

1.2 Features

- 3.3 volt standard cell library including process cores, analog cores and DRAMs.
- 0.35µm quad layer metal HCMOS technology
  – Unified process for DRAM, logic and analog
- High basic cell usages
  – Up to 3 million gates
  – Maximum usage: 90% for quad layer metal
- High speed
  – Typical 2-input NAND gate delay: 150ps (2 F/O + 2 wire load)
- Fully configurable Static RAMs and ROMs
  – Up to 512K-bit Diffusion ROM available
  – Up to 128K-bit Single-Port Static RAM available
  – Up to 64K-bit Dual-Port Static RAM
- Configurable Datapath elements available
  – 4-64 bit bus width
  – adder, ALU, barrel shifter, carry-select adder, multiplier, multi-port register file
- Operating Temperature (TA)
  – Commercial range: 0˚C to +70˚C
  – Industrial range: –40˚C to +85˚C
- Selectable output current drive capability
  – 2/4/8/12/16/24mA available for 5V
- Processor core integration capability including ARM7TDMI, 80C51, Oak and others
- Analog core integration capability including ADC, DAC, CODEC, PLL and others
- Various package options
- Fully integrated CAD software support
  – Synopsys, VSS, Verilog-XL, Powerview, Mentor, Motive and IKOS
- Cell set optimized for synthesis

1.3 CAE Support

STDH90/MDL90 supports popular design platforms and environments such as Verilog, Viewlogic, Mentor, IKOS and Synopsys for front-end logic design capture, synthesis, and simulation, and Avanti for back-end placement and routing.

For a high simulation accuracy, STDH90/MDL90 uses a proprietary delay calculator. Cell delay calculations are based on a matrix of delay parameters for each macrocell, and signal interconnection delay is based on the RC tree analysis.

1.4 Product Family

STDH90/MDL90 library include the following design elements:

- Internal Macrocells
- Compiled Macrocells
- Input/Output Cells
- JTAG Boundary Scans.

1.4.1 Internal Macrocells

Macrocells are the lowest level of logic functions such as NAND, NOR and flip-flop used for logic designs. There are about 430 different types of internal macrocells. They usually come in three levels of drive strength (1X, 2X and 4X).

These macrocells have many levels of representations—logic symbol, logic model, timing model, transistor schematic, HSPICE netlist, physical layout, and placement and routing model.

1.4.2 Compiled Macrocells

Compiled macrocells of STDH90/MDL90 consist of compiled memory and compiled datapath macrocells.

Compiled memory macrocells include three single-port RAMs (synchronous, asynchronous and alternative), three dual-port RAMs (synchronous, asynchronous and alternative) and two ROMs (synchronous diffusion programmable and via programmable). Synchronous memories have a fully synchronous operation for clock. Asynchronous memories have a synchronous operation for Write Enable in write mode and have an asynchronous operation for address in read mode. Those compiled memories have an automatic power-down mode that significantly reduces power consumption for read and write operations. This power-down mode ensures that memory consumes power for the minimum amount of time needed for a read or write operation. Some of memories support dual bank option to double the maximum capacity. Also, Flexible memory apsect ratio is provided. Now, a softmacro based memory BIST (Built-In Self Test) capability is available. Several memory macrocells of the same type or the different type in a circuit can be tested by single BIST circuit.

Compiled datapath macrocells include adder, ALU, barrel shifter, carry select adder, multiplier and multi-port register file. Adder supports both addition and subtraction and adopts a group-bypass carry propagation scheme to improve performance. ALU supports 9 arithmetic operations and 15 logical operations. Carry select adder is much faster than adder and adopts a double-carry propagation scheme to improve performance. Multiplier supports pipe-lined scheme to improve performance and also accumulation scheme. Multi-port register file allows 1-to-2 write and 1-to-4 read ports and each port is fully independent. In write mode, this register file operates synchronously for clock. In read mode, it operates asynchronously for address.

We provide two kinds of engineering design services. One is to support additional compiled datapath macrocells such as Comparators, Detectors, Incrementers and Decrementers, Multiplexers, and so on. The other is to support hardwired datapath module design.

1.4.3 Input/Output Cells

There are about four hundred different I/O buffers. Each I/O cell is implemented solely on the basic I/O cell architecture which forms the periphery of a chip.

A test logic is provided to enable the efficient parametric (threshold voltage) testing on input buffers including CMOS and TTL level converters, Schmitt trigger input buffers, clock drivers and oscillator buffers. Pull-up and pull-down resistors are optional features.

Three basic types of output buffers (non-inverting, tri-state and open drain) are available in a range of driving capabilities from 2mA to 24mA for 5 V drive . One or two levels of slew rate controls are provided for each buffer type (except 2mA buffers) to reduce output power/ground noise and signal ringing, especially in simultaneous switching outputs.

Bi-directional buffers are combinations of input buffers and output buffers (tri-state or open drain) in a single unit. The I/O structure has been fully characterized for ESD protection and latch-up resistance.

For user's convenience, STDH90/MDL90 library provides 50 KΩ pull-down and pull-up resistances respectively.

1.4.3.1 I/O Cell Drives Options

To provide designers with the greater flexibility, each I/O buffer can be selected among various current levels (e.g., 2mA, 4mA, ..., 24mA). The choice of current-level for I/O buffers affects their propagation delay and current noise.

The slew rate control helps decrease the system noise and output signal overshoot/undershoot caused by the switching of output buffers. The output edge rate can be slowed down by selecting the high slew rate control cells. STDH90/MDL90 provides three different sets of output slew rate controls. Only one I/O slot is required for any slew rate control options.

1.5 Propagation Delays

Refer to STD90/MDL90.

1.6 Delay Model

Refer to STD90/MDL90.

1.7 Testability Design Methodology

Refer to STD90/MDL90.

1.8 Maximum Fanouts

1.8.1 Internal Macrocells

Refer to STD90/MDL90.

1.8.2 Clock Drivers

STD90 max fanout for clock drivers
<condition>

- clock trunk width = 8 um
- clock trunk length = 5,000 um
- capacitance per fanout = 0.007838 pF
  (= input capacitance for CK pin of fd1)
- standard load(SL) = 0.011 pF
  (= input capacitance for iv)
- net length = 200 um per fanout
- max output transition time = 3.0 ns
- frequency $\leq$ 120 MHz

Table 1-1. Maximum Fanout of Clock Drivers

Cell Type	# of Fanout	# of SL
CK2X	522	379
CK3X	703	511
CK4X	788	572

For a design with an operating frequency higher than 120 MHz, SEC strongly recommends using clock tree synthesis.

1.8.3 I/O Cells

The maximum fanouts for I/O cells are as follows.

Table1-2. Maximum Fanouts of I/O cells(When input tr/tf = 1.6ns)

Cell Class	Output Pin	Maximum Fanouts	Cell Class	Output Pin	Maximum Fanouts
PHIC	Y	263	PHILI	Y	263
PHICD50	Y	264	PHILID50	Y	263
PHICU50	Y	264	PHILIU50	Y	263
PHIL	Y	262	PHISI	Y	263
PHILD50	Y	264	PHISID50	Y	263
PHILU50	Y	264	PHISIU50	Y	263
PHIS	Y	263	PHITATA	Y	264
PHISD50	Y	262	PHITU50ATA	Y	264
PHISU50	Y	263	PHITI	Y	263
PHIT	Y	264	PHITID50	Y	263
PHITD50	Y	264	PHITIU50	Y	264
PHITU50	Y	263	PHSOSCLF	Y	933
PHITU5	Y	263	PHSOSCMF	Y	1138
PHITU50C	Y	263	PHSOSCHF	Y	1860

1.9 Product Line-Up

Refer to STD90/MDL90.

1.10 Package Capability by Lead Count.

Refer to STD90/MDL90.

1.11 External Design Interface Considerations

Refer to STD90/MDL90.

1.12 Power Dissipation

Refer to STD90/MDL90.

1.13 VDD/VSS Rules and Guidelines

There are three types of VDD and VSS in STDH90/MDL90, providing power with internal and I/O pad area.

- Core logic
  – VDD3I, VSSI
- Pre-drive (I/O area)
  – VDD5P, VSSP
- Output-drive (I/O area)
  – VDD5O, VSSO

The number of VDD and VSS pads required for a specific design depends on the following factors:

- Number of input and output buffers
- Number of simultaneous switching outputs
- Number of used gates and simultaneous switching gates
- Operating frequency of the design.

1.13.1 Basic Placement Guidelines

The purpose of these guidelines is to minimize IR drop and noise for reliable device operation.

- Core logic and pre-driver Vdd/Vss pads should be evenly distributed on all sides of the chip.

- If you have core block demanding high power(compiled memory,analog) , extra power pads should be placed on that side.

- Power pads for SSO group should be evenly distributed in the SSO group.

- Do not place the high drive output or bi-directional buffer next to a SSO group.

- Opposite type power pads(Vdd/Vss) should be placed as close as possible. Same type power pads(Vdd/Vdd,Vss/Vss) should be separated. These two placement scheme will reduce the mutual inductance of lead of power pads.

1.13.2 Core Logic VDD/VSS Bus and VDDI/VSSI Pad Allocation Guidelines

The purpose of these guidelines is to ensure that minimum number of core logic power pad pairs requirement based on electro-migration current limit. The number of VDD/VSS pads required for a specific design is the function of the operating frequency of a chip, i.e., designs operating at high frequency should use more VDD/VSS pads.

- VDD bus width and pad requirements are equal to those of VSS.

- VDD/VSS buses and pads should be distributed evenly in the core and on all sides of the chip.

- The total number of core logic VDDI pads required is equal to that of VSSI pads

The number of VSSI/VDDI pad pairs required for a design can be calculated from the following expression:

The number of VDDI/VSSI pad pairs =

$$|| (G \times S \times F \times GC_{eq\_current}) + \{\Sigma(P\_i \times F\_i)\} / I_{em} || \text{ round-up}$$

In the above formula,

G = The core (excluding hard macro blocks) size in gate counts
S = % of simultaneous switching gates (default = 0.2)
F = Switching frequency (MHz)
$GC_{eq\_current}$ = Equivalent power(current) per gate(0.101uW/MHz/V)
P_i = Characterized power (current) for the i-th hard macro block(mA/MHz)
F_i = Switching frequency for the i-th hard macro block(MHz)
I_{em} = Current limit per Vdd/Vss pad pairs based on electromigration rule. (100mA)

For reliable device operation and minimum IR voltage drop, minimum number of VSSI/VDDI pad pairs is 4.
Extra power may be needed for the demanding high power macro blocks (SRAM,analog block,and so on)

1.13.3 Input Buffer VDD/VSS Pad VDDP/VSSP Allocation Guidelines

These guidelines ensure that an adequate input threshold voltage margin is maintained during a switching.

The number of VSSP/VDDP pad pairs required for a design can be calculated from the following expression:

The number of VDDP/VSSP pad pairs =

$$|| Ieq\_p / I_{em} || \text{round-up}$$

in the above formula,

Ieq_p = ∑(Average current of input buffers and output pre-drivers at maximum operating frequency)
I_{em} = Current limit per Vdd/Vss pad pairs based on electro-migration rule. (100 mA)

Table 1-3. Ieq_p(at F=100MHz) value of each input buffer and output pre-driver.

Table 1-3(a). Ieq_p(at F=100MHz) value of each type of input buffer

Input Buffer Type	CMOS	CMOS Schmitt	TTL	TTL Schmitt
Ieq_p(mA)	0.37	0.45	0.30	0.53

Table 1-3(b). Ieq_p(at F=100MHz) value of each type of output pre-driver

Output Slew-Rate Type	Normal	Medium	High
Ieq_p(mA)	1.0	1.2	1.8

If buffer type is bi-directional, then you should combine the proper input buffer and output pre-driver Ieq_p value.
For reliable device operation and minimum IR voltage drop, minimum number of VSSP/VDDP pad pairs is 4.
In order to minimize number of power pads, you may use combined power pad. You can get the combined power pad pairs VDDIP/VSSIP from the following formula.

The number of VDDIP/VSSIP pad pairs =

$$|| (G \times S \times F \times GC_{eq\_current}) + \{\Sigma(P\_i \times F\_i)\} / I_{em} + Ieq\_p / I_{em} || \text{ round-up}$$

For reliable device operation and minimum IR voltage drop, minimum number of VSSIP/VDDIP pad pairs is 4.

1.13.4 Output Buffer VDD/VSS Pad VDDO/VSSO Allocation Guidelines

SSO(Simultaneous Switching Output) current induced in power and ground inductance can cause system failure because of voltage fluctuations. In case of output driver power pad calculation, we consider the SSO noise as well as current limit based on electro-migration. We may define SSO as outputs are considered to be simultaneous in 1ns window such as bus type buffers.

The number of VDDO/VSSO pads required for a device can be calculated from the following expressions.

- The number of power pads for each SSO group from the following formula.

  $NVDDO_{each\_sso} = (number\_of\_SSO \times L_{lead}) / (D_{sso\_mode} \times NB_{vdd})$
  $NVSSO_{each\_sso} = (number\_of\_SSO \times L_{lead}) / (D_{sso\_mode} \times NB_{vss})$

  in the above formula,

$NVDDO_{each\_sso}$ = the number of VDDO pads required for each SSO group
$NVSSO_{each\_sso}$ = the number of VSSO pads required for each SSO group
NB_{vdd} = the number of buffers per VDD power pad with 1nH lead inductance
NB_{vss} = the number of buffers per VSS ground pad with 1nH lead inductance
L_{lead} = lead frame inductance of package
(Refer to 1.10 Package Capability by Lead Count)

$D_{sso\_mode} = D_{L\_mode} \times D_{P\_mode} \times D_{V\_mode} \times D_{T\_mode} \times D_{C\_mode}$

D_{L_mode} : Lead inductance derating factor
D_{P_mode} : Process derating factor
D_{V_mode} : Voltage derating factor
D_{T_mode} : Temperature derating factor
D_{C_mode} : C_{load} derating factor
(mode is either vdd or vss. Refer to Table 1.4)

Table 1-4. Derating Equation

Item	Mode	Equation	Range
Package Lead	D_{L_vdd}	0.0052 * Lpg + 0.9794	3nH ≤ Lpg ≤ 10nH
		-0.0052 * Lpg + 1.0825	10nH < Lpg ≤ 15nH
	D_{L_vss}	-0.0094 * Lpg + 1.0377	3nH ≤ Lpg ≤ 10nH
		0.0377 * Lpg + 0.5660	10nH < Lpg ≤ 15nH
Process	D_{P_vdd}	1	best
		1.1134	typical
		1.2887	worst
	D_{P_vss}	1	best
		1.3208	typical
		1.5094	worst
Voltage	D_{V_vdd}	-0.2222 * voltage + 2.1556	4.5 ≤ voltage ≤ 5.0
		-0.1778 * voltage + 2.9333	5.0 < voltage ≤ 5.5
	D_{V_vdd}	-0.2500 * voltage + 2.2812	4.5 ≤ voltage ≤ 5.0
		-0.1250 * voltage + 1.6562	5.0 < voltage ≤ 5.5
Temp.	D_{T_vdd}	0.0008 * temp + 1.0000	-40 ≤ temp ≤ 25
		0.0006 * temp + 1.0066	25 < temp ≤ 125
	D_{T_vdd}	0.0045 * temp + 1.0000	-40 ≤ temp ≤ 25
		0.0034 * temp + 1.0274	25 < temp ≤ 125
Cload	D_{C_vdd}	0.0155 * Cload + 0.5361	10pF ≤ Cload ≤ 30pF
		0.0180 * Cload + 0.4588	30pF < Cload ≤ 100pF
	D_{C_vdd}	0.0255 * Cload + 0.2358	10pF ≤ Cload ≤ 30pF
		0.0142 * Cload + 0.5755	30pF < Cload ≤ 100pF

- The number of power pads for total SSO groups from the following formula.

  $NVDDO_{sso} = \sum NVDDO_{each\_sso}$
  $NVSSO_{sso} = \sum NVSSO_{each\_sso}$

  in the above formula,

  $NVDDO_{sso}$ = the number of VDDO pads required for total SSO groups
  $NVSSO_{sso}$ = the number of VSSO pads required for total SSO groups

- The number of power pads for non-SSO group from the following formula.

  $N_{NSvddo} = I_{eq\_o} / I_{em}$
  $N_{NSvsso} = I_{eq\_o} / I_{em}$

  in the above formula,

  $I_{eq\_o} = \sum_{non\text{-}SSO} (C_{load} \times V \times F \times P)$

  C_{load} : output load capacitance
  V : operating voltage
  F : operating frequency
  P : I/O switching percent(marginal=0.5)
  I_{em} : Current density based on electro-migration rule(100mA)

- The total number of power pads for VDDO from the following formula.

  $|| \sum(number\_of\_SSO \times L_{lead}) / (D_{sso\_mode} \times NB_{vdd}) + I_{eq\_o} / I_{em} ||$ round-up

- The total number of power pads for VSSO from the following formula.

  $|| \sum (number\_of\_SSO \times L_{lead}) / (D_{sso\_mode} \times NB_{vss}) + I_{eq\_o} / I_{em} ||$ round-up

If you use open-drain type buffers, you can consider only VSSO power pads because they have only current sink.

Table 1-5. NBvdd/NBvss Parameter
(Condition : Process=best , Voltage=5.25V , Temp=0°C , Cload=30pF)

Buffer Type	Normal		Medium		High	
	NBvdd	NBvss	NBvdd	NBvss	NBvdd	NBvss
B2	170	116				
B4	84	55	89	58		
B8	39	28	40	29		
B12	28	20	30	21	31	22
B16	23	16	24	17	26	18
B24	19	13	20	14	22	15

1.14 Crystal Oscillator Consideration

Refer to STD90/MDL90.