FUJITSU MICROELECTRONICS
DATA SHEET

DS05-11454-1E

MEMORY Mobile FCRAM™

CMOS

128 M Bit (8 M word×16 bit)

Mobile Phone Application Specific Memory

MB82DBS08164D-70L

■ DESCRIPTION

The FUJITSU MICROELECTRONICS MB82DBS08164D is a CMOS Fast Cycle Random Access Memory (FCRAM*) with asynchronous Static Random Access Memory (SRAM) interface containing 134,217,728 storages accessible in a 16-bit format.
The MB82DBS08164D adopts asynchronous mode and synchronous burst mode for fast memory access as user configurable options.
The MB82DBS08164D is suited for mobile applications such as Cellular Handset and PDA.

* : FCRAM is a trademark of Fujitsu Microelectronics Limited, Japan

■ FEATURES

- Asynchronous SRAM Interface
- COSMORAM Revision 3 Compliance
  (COSMORAM : Common Specifications of Mobile RAM)
- Fast Access Time : t_{CE} = 70 ns Max
- Burst Read/Write Access Capability :
  t_{CK} = 13 ns Min /77 MHz Max
  t_{AC} = 6 ns Max
- Low Voltage Operating Condition : V_{DD} = 1.7 V to 1.95 V
- Wide Operating Temperature : T_A = 0 °C to + 70 °C
- Byte Control by $\overline{LB}$ and $\overline{UB}$
- Low-Power Consumption : I_{DDA1} = 35 mA Max
  I_{DDS1} = 200 µA Max ($T_A \leq$ + 40 °C)
- Various Power Down mode : Sleep
  16 M-bit Partial
  32 M-bit Partial
  64 M-bit Partial

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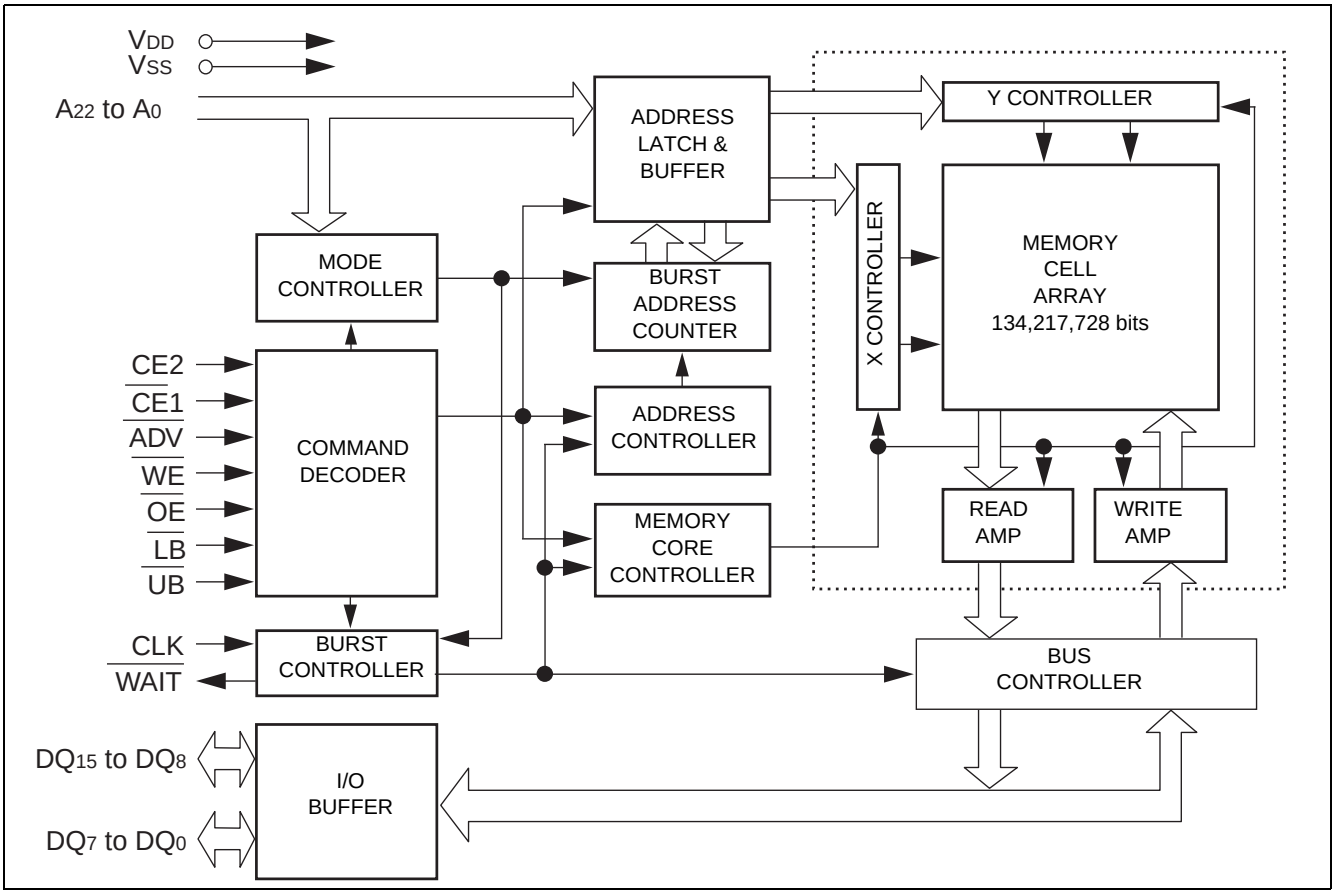
2009.10

■ BLOCK DIAGRAM



2. Synchronous Operation (Burst Mode)

Mode	CE2	$\overline{CE1}$	CLK	$\overline{ADV}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	A_{22} to A_0	DQ_{15} to DQ_0	$\overline{WAIT}$
Standby(Deselect)	H	H	X	X	X	X	X	X	X	High-Z	High-Z
Start Address Latch*1		L	*3 ↑	L	X*4	X*6	X*7	X*7	Valid*8	High-Z*9	Output Invalid
Advance Burst Read to Next Address*1			*3 ↑	H	H	L			X	Output Valid*10	Output Valid
Burst Read Suspend*1			*3 ↑			H				High-Z	High*12
Advance Burst Write to Next Address*1			*3 ↑	H	L*5	H				Input Valid*11	High*13
Burst Write Suspend*1			*3 ↑		H*5					Input Invalid	High*12
Terminate Burst Read		↑	X		H	X				High-Z	High-Z
Terminate Burst Write		↑	X		X	H				High-Z	High-Z
Power Down*2	L	X	X	X	X	X	X	X	X	High-Z	High-Z

Note : L = V_{IL}, H = V_{IH}, X can be either V_{IL} or V_{IH}, ↑ = valid edge, High-Z = High impedance

*1 : Should not be kept this logic condition longer than 8 µs.

*2 : Power Down mode can be entered from Standby state and all output are in High-Z state.
Data retention depends on the selection of Partial Size for Power Down Program.
Refer to "Power Down" in "■FUNCTIONAL DESCRIPTION" for the details.

*3 : CLK must be started and stable prior to memory access.

*4 : Can be V_{IH} for the burst write operation in "$\overline{WE}$ Level Control" mode but must be V_{IL} for the burst write operation in "$\overline{WE}$ Single Clock Pulse Control" mode. $\overline{WE}$ must be V_{IH} for the burst read operation.

*5 : When device is operating in "$\overline{WE}$ Single Clock Pulse Control" mode, $\overline{WE}$ is a "don't care" once write operation is determined by $\overline{WE}$ Low Pulse at the beginning of write access together with address latching. Burst write suspend feature is not supported in "$\overline{WE}$ Single Clock Pulse Control" mode.

*6 : Can be V_{IL} for the burst read operation but must be V_{IH} for the burst write operation.

*7 : Can be either V_{IL} or V_{IH}. During burst write operation, byte write control by $\overline{LB}$ and $\overline{UB}$ can be performed at each clock cycle. During read operation, $\overline{LB}$ and $\overline{UB}$ must be valid before read operation is initiated. And once $\overline{LB}$ and $\overline{UB}$ input levels are determined, they must not be changed until the end of burst read.

*8 : Once a valid address is determined, the input address must not be changed during $\overline{ADV}$ = L.

*9 : If $\overline{OE}$ = L, data output is either Invalid or High-Z depending on the level of $\overline{LB}$ and $\overline{UB}$ input. If $\overline{WE}$ = L, data input is Invalid. If $\overline{OE}$ = $\overline{WE}$ = H, data output is High-Z.

*10 : Data output is either Valid or High-Z depending on the level of $\overline{LB}$ and $\overline{UB}$ input.

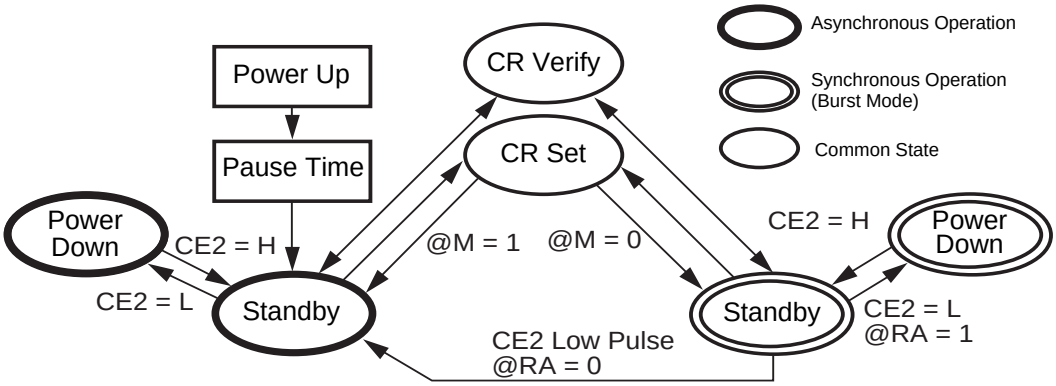
*11 : Data input is either Valid or Invalid depending on the level of $\overline{LB}$ and $\overline{UB}$ input.

*12 : Keep the level from previous cycle except for suspending on last data. Refer to "$\overline{WAIT}$ Output Function" in "■FUNCTIONAL DESCRIPTION" for the details.

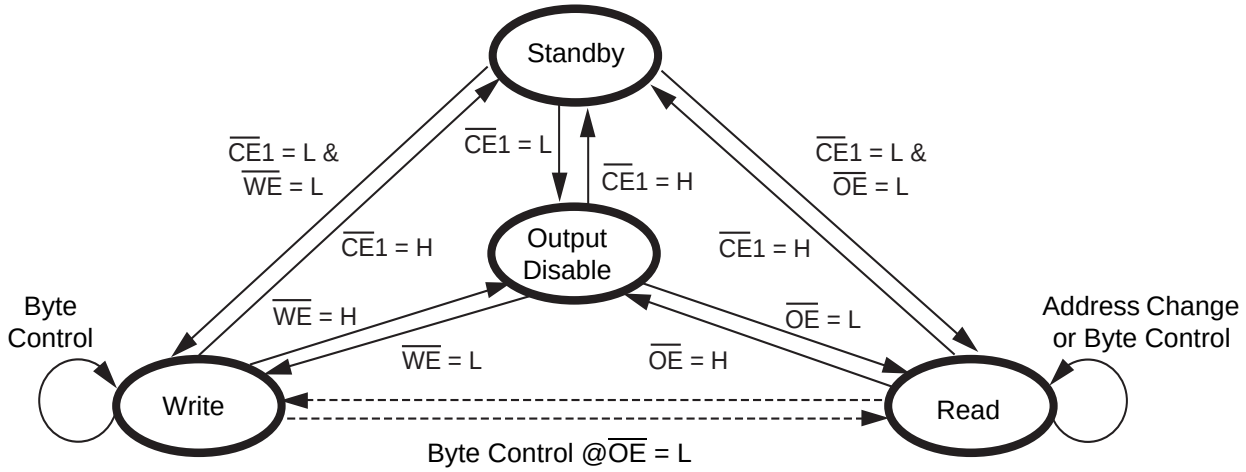
*13 : $\overline{WAIT}$ output is driven in High level during burst write operation.

■ STATE DIAGRAM

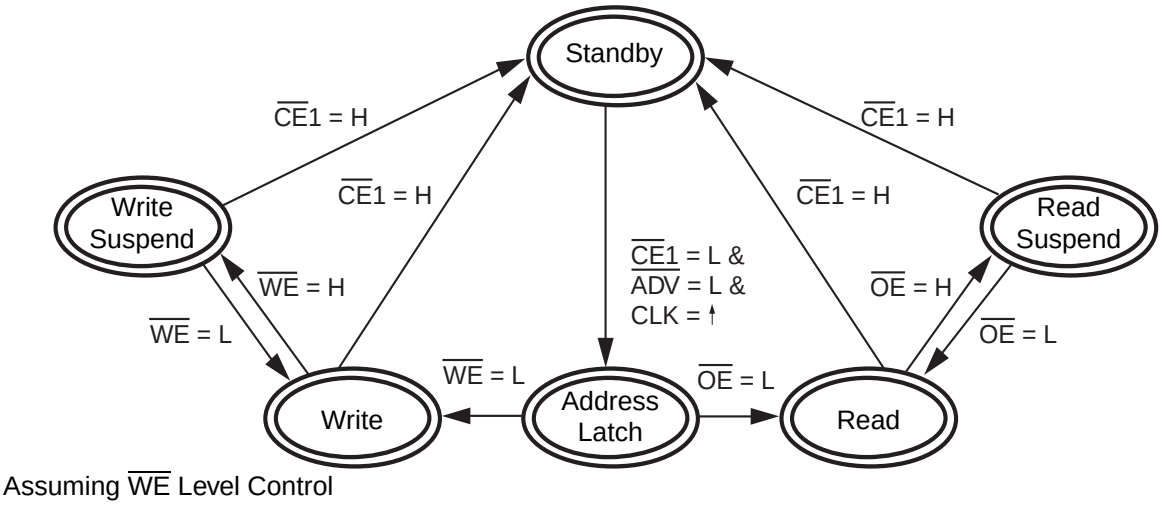
• Initial/Standby State



• Asynchronous Operation



• Synchronous Operation



* : Assuming $\overline{WE}$ Level Control

Note : Assuming all the parameters specified in AC CHARACTERISTICS are satisfied. Refer to the "■ FUNCTION TRUTH TABLE", "■ FUNCTIONAL DESCRIPTION", "2. AC Characteristics" in "■ ELECTRICAL CHARACTERISTICS", and "■TIMING DIAGRAMS" for details.

■ FUNCTIONAL DESCRIPTION

This device supports asynchronous read & write operation and synchronous burst read and burst write operations for faster memory access and features four kinds of power down modes for power saving as user configurable option.

• Power-up

It is required to follow the power-up timing to start executing proper device operation. Refer to "Power-up Timing". After Power-up, the device defaults to asynchronous read & write operation mode with sleep power down feature.

• Configuration Register

The Configuration Register(CR) is used to configure the type of device function among optional features. Each selection of features is set through CR Set sequence after power-up. If CR Set sequence is not performed after power-up, the device is configured for asynchronous operations with sleep power down feature as default configuration. The content of CR can be confirmed using CR Verify sequence.

• CR Set & Verify Sequence

The CR Set and CR Verify requires total 6 read/write operations with unique address and data. The device should be in standby mode in the interval between each read/write operation. The following table shows the detail sequence of CR Set and CR Verify.

Cycle #	Address	CR Set		CR Verify	
		Operation	Data	Operation	Data
1st	7FFFFFh (MSB)	Read	Read Data (RDa)	Read	Read Data (RDa)
2nd	7FFFFFh	Write	RDa	Write	RDa
3rd	7FFFFFh	Write	RDa	Write	RDa
4th	7FFFFFh	Write	CR Key 0	Write	CR Key 0
5th	7FFFFFh	Write	CR Key 1	Read	CR Key 1
6th	7FFFFFh	Write	CR Key 2	Read	CR Key 2

The 1st cycle is to read from most significant address(MSB).
The 2nd and 3rd cycles are to write to MSB. If the 2nd or 3rd cycle is written into the different address, the CR Set is cancelled and the data written by the 2nd or 3rd cycle is valid as a normal write operation. It is recommended to write back the data(RDa) read by 1st cycle to MSB in order to secure the data.

The 4th cycle is to write the appropriate “CR Key 0” to select the CR Set or CR Verify.
The 5th and 6th cycles are to access into MSB to set the “CR Keys” or to verify the “CR Keys”. Refer to the "CR Key Table". If the 4th to 6th cycles are not access into MSB , the CR Set or CR Verify are cancelled and CR input or output data will be invalid.

Once this CR Set sequence is performed from an initial CR Set to the other new CR Set, the written data stored in the memory cell array may be lost. Therefore CR Set sequence should be performed prior to regular read/ write operation if necessary to change from the default configuration.

2. Synchronous Operation (Burst Mode)

Mode	CE2	$\overline{CE1}$	CLK	$\overline{ADV}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	A_{22} to A_0	DQ_{15} to DQ_0	$\overline{WAIT}$
Standby(Deselect)	H	H	X	X	X	X	X	X	X	High-Z	High-Z
Start Address Latch*1		L	*3 ↑	L	X*4	X*6	X*7	X*7	Valid*8	High-Z*9	Output Invalid
Advance Burst Read to Next Address*1			*3 ↑	H	H	L			X	Output Valid*10	Output Valid
Burst Read Suspend*1			*3 ↑			H				High-Z	High*12
Advance Burst Write to Next Address*1			*3 ↑	H	L*5	H				Input Valid*11	High*13
Burst Write Suspend*1			*3 ↑		H*5					Input Invalid	High*12
Terminate Burst Read		↑	X		H	X				High-Z	High-Z
Terminate Burst Write		↑	X		X	H				High-Z	High-Z
Power Down*2	L	X	X	X	X	X	X	X	X	High-Z	High-Z

Note : L = V_{IL}, H = V_{IH}, X can be either V_{IL} or V_{IH}, ↑ = valid edge, High-Z = High impedance

*1 : Should not be kept this logic condition longer than 8 µs.

*2 : Power Down mode can be entered from Standby state and all output are in High-Z state.
Data retention depends on the selection of Partial Size for Power Down Program.
Refer to "Power Down" in "■FUNCTIONAL DESCRIPTION" for the details.

*3 : CLK must be started and stable prior to memory access.

*4 : Can be V_{IH} for the burst write operation in "$\overline{WE}$ Level Control" mode but must be V_{IL} for the burst write operation in "$\overline{WE}$ Single Clock Pulse Control" mode. $\overline{WE}$ must be V_{IH} for the burst read operation.

*5 : When device is operating in "$\overline{WE}$ Single Clock Pulse Control" mode, $\overline{WE}$ is a "don't care" once write operation is determined by $\overline{WE}$ Low Pulse at the beginning of write access together with address latching. Burst write suspend feature is not supported in "$\overline{WE}$ Single Clock Pulse Control" mode.

*6 : Can be V_{IL} for the burst read operation but must be V_{IH} for the burst write operation.

*7 : Can be either V_{IL} or V_{IH}. During burst write operation, byte write control by $\overline{LB}$ and $\overline{UB}$ can be performed at each clock cycle. During read operation, $\overline{LB}$ and $\overline{UB}$ must be valid before read operation is initiated. And once $\overline{LB}$ and $\overline{UB}$ input levels are determined, they must not be changed until the end of burst read.

*8 : Once a valid address is determined, the input address must not be changed during $\overline{ADV}$ = L.

*9 : If $\overline{OE}$ = L, data output is either Invalid or High-Z depending on the level of $\overline{LB}$ and $\overline{UB}$ input. If $\overline{WE}$ = L, data input is Invalid. If $\overline{OE}$ = $\overline{WE}$ = H, data output is High-Z.

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*12 : Keep the level from previous cycle except for suspending on last data. Refer to "$\overline{WAIT}$ Output Function" in "■FUNCTIONAL DESCRIPTION" for the details.

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2. Synchronous Operation (Burst Mode)

Mode	CE2	$\overline{CE1}$	CLK	$\overline{ADV}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	A_{22} to A_0	DQ_{15} to DQ_0	$\overline{WAIT}$
Standby(Deselect)	H	H	X	X	X	X	X	X	X	High-Z	High-Z
Start Address Latch*1		L	*3 ↑	L	X*4	X*6	X*7	X*7	Valid*8	High-Z*9	Output Invalid
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Advance Burst Write to Next Address*1			*3 ↑	H	L*5	H				Input Valid*11	High*13
Burst Write Suspend*1			*3 ↑		H*5					Input Invalid	High*12
Terminate Burst Read		↑	X		H	X				High-Z	High-Z
Terminate Burst Write		↑	X		X	H				High-Z	High-Z
Power Down*2	L	X	X	X	X	X	X	X	X	High-Z	High-Z

Note : L = V_{IL}, H = V_{IH}, X can be either V_{IL} or V_{IH}, ↑ = valid edge, High-Z = High impedance

*1 : Should not be kept this logic condition longer than 8 µs.

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Data retention depends on the selection of Partial Size for Power Down Program.
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*11 : Data input is either Valid or Invalid depending on the level of $\overline{LB}$ and $\overline{UB}$ input.

*12 : Keep the level from previous cycle except for suspending on last data. Refer to "$\overline{WAIT}$ Output Function" in "■FUNCTIONAL DESCRIPTION" for the details.

*13 : $\overline{WAIT}$ output is driven in High level during burst write operation.

- **Power Down**

  The Power Down is low power idle state controlled by CE2. CE2 Low drives the device in power down mode and maintains low power idle state as long as CE2 is kept Low. CE2 High resumes the device from power down mode.

  This device has four power down modes, Sleep, 16 M-bit Partial, 32 M-bit Partial, and 64 M-bit Partial. Those power down modes are effective when RA = 1. The selection of power down mode is set through CR Set sequence. Each mode has following data retention features.

Mode	Data Retention Size	Retention Address
Sleep [default]	No	N/A
16 M-bit Partial	16 M bits	000000h to 0FFFFFh
32 M-bit Partial	32 M bits	000000h to 1FFFFFh
64 M-bit Partial	64 M bits	000000h to 3FFFFFh

  The default state is Sleep and it is the lowest power consumption. However all data will be lost once CE2 is brought to Low for Power Down. It is not required to perform CR Set sequence to set to Sleep mode after power-up in case of asynchronous operation.

  When RA = 0, CE2 brought to Low reset the device to asynchronous standby state regardless PS set value.

- **Burst Read/Write Operation**

  Synchronous burst read/write operation provides faster memory access that synchronized to the microcontroller or system bus frequency. Configuration Register(CR) Set is required to perform a burst read & write operation after power-up. Once CR Set sequence is performed to select the synchronous burst mode, the device is configured to synchronous burst read/write operation mode with corresponding RL and BL that is set through CR Set sequence together with the operation mode.

- **Address Latch by $\overline{ADV}$**

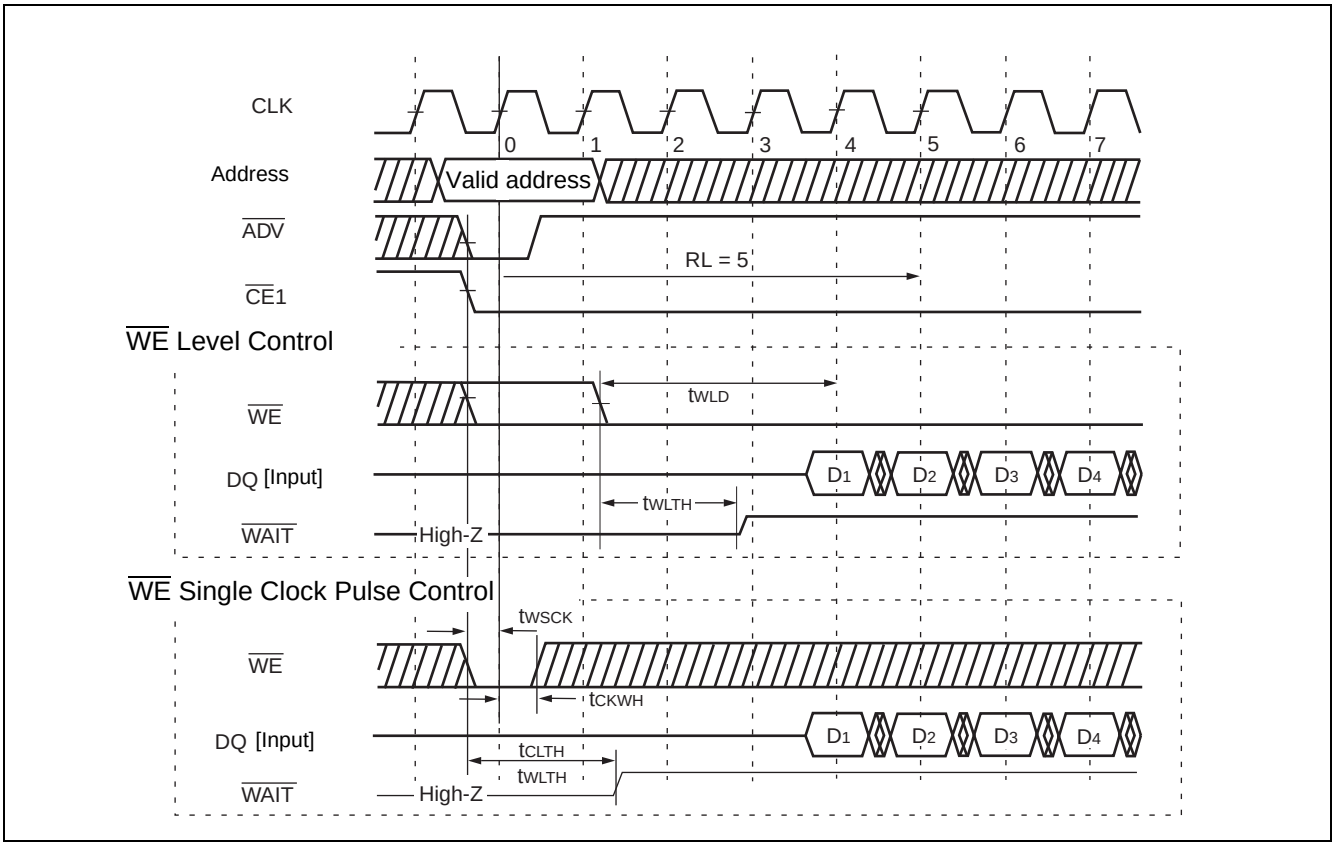
  The $\overline{ADV}$ latches the valid address presence on address inputs. During synchronous burst read/write operation mode, all the addresses are determined on first rising edge when $\overline{ADV}$ = $\overline{CE}$1 = L. The specified minimum value of $\overline{ADV}$ = L setup time and hold time against valid edge of clock where RL count is begun must be satisfied for appropriate RL counts. Valid address must be determined with specified setup time against valid clock edge. And the determined valid address must not be changed during $\overline{ADV}$ = L period.

- **Burst Length**

  Burst Length is the number of word to be read or written during synchronous burst read/write operation as the result of a single address latch cycle. It can be set on 8, 16, 32, 64, 128 words boundary for entire address through CR Set sequence. The burst type is sequential that is incremental decoding scheme within a boundary address. Starting from an initial address being latched, the device internal address counter assigns +1 to the previous address until reaching the end of boundary address and then wrap round to least significant address (= 0). After completing read data output or write data latch for the set burst length, operation automatically ended.

- **Write Control**

  The device has two types of $\overline{WE}$ signal control method, "$\overline{WE}$ Level Control" and "$\overline{WE}$ Single Clock Pulse Control", for synchronous burst write operation. It is configured through CR Set sequence. When device is operating in "$\overline{WE}$ Single Clock Pulse Control" mode, burst write operation is determined by $\overline{WE}$ = L at the rising edge of CLK. In case of "$\overline{WE}$ Level Control", $\overline{WE}$ can be High at address latching and $\overline{WE}$ = L enables burst write operation.

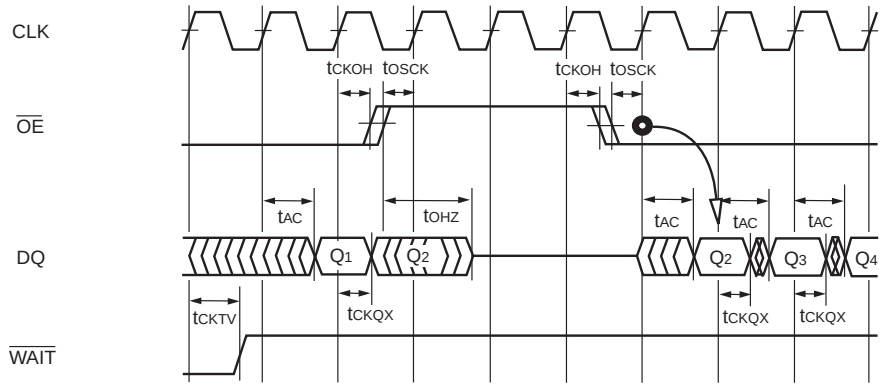


- **Burst Read Suspend**

Burst read operation can be suspended by $\overline{OE}$ High pulse. During burst read operation, $\overline{OE}$ brought to High suspends the burst read operation. Once $\overline{OE}$ is brought to High with the specified setup time against clock where the data being suspended, the device internal counter is suspended, and the data output becomes high impedance after specified time duration. It is inhibited to suspend the first data output at the beginning of burst read.

$\overline{OE}$ brought to Low resumes the burst read operation. Once $\overline{OE}$ is brought to Low, data output becomes valid after specified time duration, and the internal address counter is reactivated. The last data output being suspended as the result of $\overline{OE}$ = H and first data output as the result of $\overline{OE}$ = L are from the same address.

In order to guarantee to output last data before suspension and first data after resumption, the specified minimum value of $\overline{OE}$ = L hold time and setup time against clock edge must be satisfied respectively.



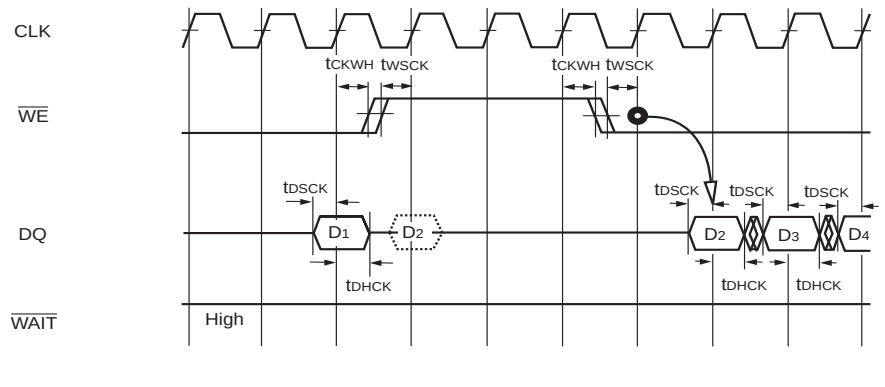
- **Burst Write Suspend**

Burst write operation can be suspended by $\overline{WE}$ High pulse. During burst write operation, $\overline{WE}$ brought to High suspends the burst write operation. Once $\overline{WE}$ is brought to High with the specified setup time against clock where the data being suspended, the device internal counter is suspended, data input is ignored. It is inhibited to suspend the first data input at the beginning of burst write.

$\overline{WE}$ brought to Low resumes the burst write operations. Once $\overline{WE}$ is brought to Low, data input becomes valid after specified time duration, and the internal address counter is reactivated. The write address of the cycle where data being suspended and the first write address as the result of $\overline{WE}$ = L are the same address.

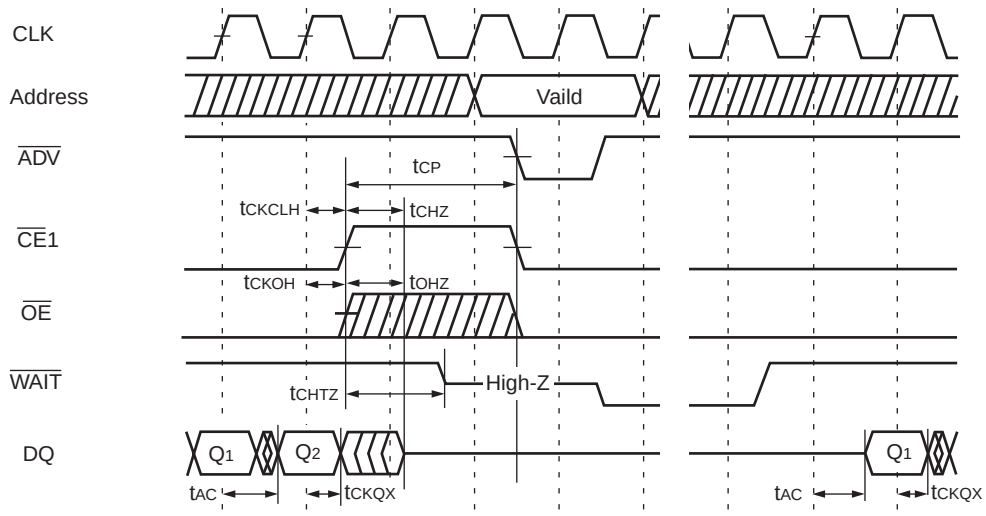
In order to guarantee to latch the last data input before suspension and first data input after resumption, the specified minimum value of $\overline{WE}$ = L hold time and setup time against clock edge must be satisfied respectively.

Burst write suspend function is available only when the device is operating in $\overline{WE}$ level controlled burst write.



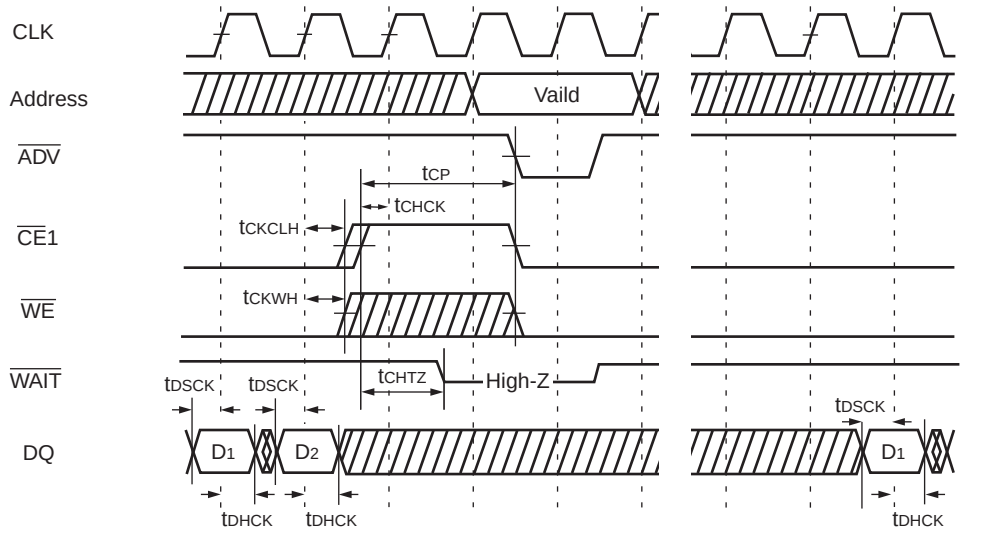
• **Burst Read Termination**

Burst read operation can be terminated by $\overline{CE}1$ brought to High. It is inhibited to terminate the burst read before first data output is completed. In order to guarantee last data output, the specified minimum value of $\overline{CE}1$ = L hold time from the clock edge must be satisfied. After termination, the specified minimum recovery time is required to start a new access.



• **Burst Write Termination**

Burst write operation can be terminated by $\overline{CE}1$ brought to High. It is inhibited to terminate the burst write before first data input is completed. In order to guarantee last write data being latched, the specified minimum values of $\overline{CE}1$ = L hold time from the clock edge must be satisfied. After termination, the specified minimum recovery time is required to start a new access.



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Voltage of V_{DD} Supply Relative to V_{SS} *	V_{DD}	− 0.5	+ 2.3	V
Voltage at Any Pin Relative to V_{SS} *	V_{IN}, V_{OUT}	− 0.5	+ 2.3	V
Short Circuit Output Current	I_{OUT}	− 50	+ 50	mA
Storage Temperature	T_{STG}	− 55	+ 125	°C

* : All voltages are referenced to V_{SS} = 0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value		Unit
		Min	Max	
Power Supply Voltage*1	V_{DD}	1.7	1.95	V
Ground	V_{SS}	0	0	V
High Level Input Voltage*1, *2	V_{IH}	$V_{DD} \times 0.8$	$V_{DD} + 0.2$	V
Low Level Input Voltage*1, *3	V_{IL}	− 0.3	$V_{DD} \times 0.2$	V
Ambient Temperature	T_A	0	+ 70	°C

*1 : All voltages are referenced to V_{SS} = 0 V.

*2 : Maximum DC voltage on input and I/O pins is V_{DD} + 0.2 V. During voltage transitions, inputs may overshoot to V_{DD} + 1.0 V for the periods of up to 5 ns.

*3 : Minimum DC voltage on input and I/O pins is -0.3 V. During voltage transitions, inputs may undershoot V_{SS} to -1.0 V for the periods of up to 5 ns.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ PIN CAPACITANCE

(f = 1 MHz, T_A = +25 °C)

Parameter	Symbol	Test conditions	Value			Unit
			Min	Typ	Max	
Address Input Capacitance	C_{IN1}	V_{IN} = 0 V	—	—	5	pF
Control Input Capacitance	C_{IN2}	V_{IN} = 0 V	—	—	5	pF
Data Input/Output Capacitance	C_{IO}	V_{IO} = 0 V	—	—	8	pF

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(At recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions		Value		Unit
				Min	Max	
Input Leakage Current	I_{LI}	$V_{SS} \le V_{IN} \le V_{DD}$		− 1.0	+ 1.0	µA
Output Leakage Current	I_{LO}	0 V ≤ V_{OUT} ≤ V_{DD}, Output Disable		− 1.0	+ 1.0	µA
Output High Voltage Level	V_{OH}	$V_{DD} = V_{DD}$ (Min), I_{OH} = − 0.5 mA		1.4	—	V
Output Low Voltage Level	V_{OL}	I_{OL} = 1 mA		—	0.4	V
V_{DD} Power Down Current	I_{DDPS}	$V_{DD} = V_{DD}$ (Max), $V_{IN} = V_{DD}$ or V_{SS}, CE2 = V_{SS}	Sleep	—	10	µA
	I_{DDP16}		16 M-bit Partial	—	230	µA
	I_{DDP32}		32 M-bit Partial	—	260	µA
	I_{DDP64}		64 M-bit Partial	—	310	µA
V_{DD} Standby Current	I_{DDS}	$V_{DD} = V_{DD}$ (Max), V_{IN} (including CLK) = V_{IH} or V_{IL}, $\overline{CE}1$ = CE2 = V_{IH}		—	1.5	mA
	I_{DDS1}	$V_{DD} = V_{DD}$ (Max), V_{IN} (including CLK) = V_{DD} or V_{SS}, $\overline{CE}1$ = CE2 = V_{DD}	$T_A \le +70$ °C	—	400	µA
			$T_A \le +40$ °C	—	200	µA
	I_{DDS2}	$V_{DD} = V_{DD}$ (Max), $t_{CK} = t_{CK}$ (Min), $V_{IN} = V_{DD}$ or V_{SS}, $\overline{CE}1$ = CE2 = V_{DD}		—	500	µA
V_{DD} Active Current	I_{DDA1}	$V_{DD} = V_{DD}$ (Max), $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE}1 = V_{IL}$ and CE2 = V_{IH}, I_{OUT} = 0 mA	t_{RC}/t_{WC} = Min	—	35	mA
	I_{DDA2}		t_{RC}/t_{WC} = 1 µs	—	5	mA
V_{DD} Burst Access Current	I_{DDA4}	$V_{DD} = V_{DD}$ (Max), $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE}1 = V_{IL}$ and CE2 = V_{IH}, $t_{CK} = t_{CK}$ (Min), BL = 128, I_{OUT} = 0 mA		—	24	mA

Notes :
- All voltages are referenced to V_{SS} = 0 V.
- I_{DD} depends on the output termination, load conditions, and AC characteristics.
- After power on, initialization following power-up timing is required. DC characteristics are guaranteed after the initialization.
- I_{DDP16}, I_{DDP32}, I_{DDP64}, I_{DDS} and I_{DDS1} might be higher for up to 400 ms after power-up or power down/standby mode entry.

(3) Synchronous Operation - Clock Input (Burst Mode)

(At recommended operating conditions unless otherwise noted)

Parameter		Symbol	Value		Unit	Notes
			Min	Max		
Clock Period	RL = 6	t_{CK}	13	—	ns	*1
	RL = 5		15	—	ns	*1
	RL = 4		18	—	ns	*1
Clock High Time		t_{CKH}	3	—	ns	
Clock Low Time		t_{CKL}	3	—	ns	
Clock Transition Time		t_{CKT}	—	1.5	ns	*2

*1 : Clock period is defined between valid clock edges.

*2 : Clock transition time is defined between V_{IH} (Min) and V_{IL} (Max)

(4) Synchronous Operation - Address Latch (Burst Mode)

(At recommended operating conditions unless otherwise noted)

Parameter		Symbol	Value		Unit	Notes
			Min	Max		
Address Setup Time to CLK		t_{ASCK}	3	—	ns	*1
Address Hold Time from CLK		t_{CKAH}	1	—	ns	*1
$\overline{ADV}$ Low Pulse Width		t_{VPL}	7	—	ns	*2
$\overline{ADV}$ Low Setup Time to CLK	RL = 6	t_{VSCK}	3	—	ns	*1
	RL = 4, 5		5	—		
$\overline{CE}$1 Low Setup Time to CLK	RL = 6	t_{CLCK}	3	—	ns	*1
	RL = 4, 5		5	—		
$\overline{ADV}$ Low Hold Time from CLK		t_{CKVH}	1	—	ns	*1
$\overline{CE}$1 High Hold Time from CLK		t_{CKCH}	1	—	ns	*3

*1 : Applicable to the 1st rising clock edge.

*2 : t_{VPL} is specified from the falling edge of either $\overline{CE}$1 or $\overline{ADV}$ whichever comes late.

*3 : Applicable to the positive clock edge before address latching.

(6) Synchronous Write Operation (Burst Mode)

(At recommended operating conditions unless otherwise noted)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
Burst Write Cycle Time	t_{WCB}	—	8000	ns	
Data Setup Time to CLK	t_{DSCK}	3	—	ns	
Data Hold Time from CLK	t_{DHCK}	1	—	ns	
$\overline{WE}$ Low Setup Time to 1st Data Input	t_{WLD}	45	—	ns	
$\overline{WE}$ Setup Time to CLK	t_{WSCK}	3	—	ns	
$\overline{WE}$ Hold Time from CLK	t_{CKWH}	1	—	ns	
$\overline{LB}$, $\overline{UB}$ Setup Time to CLK	t_{BSCK}	3	—	ns	*1
$\overline{LB}$, $\overline{UB}$ Hold Time from CLK	t_{CKBH}	1	—	ns	*1
$\overline{CE}$1 Low to $\overline{WAIT}$ High	t_{CLTH}	5	15	ns	*2, *3
$\overline{WE}$ Low to $\overline{WAIT}$ High	t_{WLTH}	—	15	ns	*2, *3
$\overline{CE}$1 High to $\overline{WAIT}$ High-Z	t_{CHTZ}	—	9.5	ns	*2
Burst End $\overline{CE}$1 Low Hold Time from CLK	t_{CKCLH}	1	—	ns	
Burst End $\overline{CE}$1 High Setup Time to next CLK	t_{CHCK}	3	—	ns	
$\overline{CE}$1 High Pulse Width	t_{CP}	9.5	—	ns	

*1 : t_{BSCK} and t_{CKBH} should be satisfied for byte mask control.

*2 : The output load 50 pF with 50 Ω termination to $V_{DD} \times 0.5$ V.

*3 : $\overline{WAIT}$ outputs Low-Z after t_{CLTH} (Min) from $\overline{CE}$1 = L. $\overline{WAIT}$ outputs to High level after t_{WLTH} or t_{CLTH} from $\overline{WE}$ = L or $\overline{CE}$1 = L whichever occurs last.

(7) Power Down Parameters

(At recommended operating conditions unless otherwise noted)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
CE2 Low Setup Time for Power Down Entry	t_{CSP}	10	—	ns	
CE2 Low Hold Time after Power Down Entry	t_{C2LP}	70	—	ns	
CE2 Low Hold Time for Reset to Asynchronous Mode	t_{C2LPR}	70	—	ns	*1
$\overline{CE}$1 High Hold Time following CE2 High after Power Down Exit [Sleep mode only]	t_{CHH}	300	—	µs	*2
$\overline{CE}$1 High Hold Time following CE2 High after Power Down Exit [not in Sleep mode]	t_{CHHP}	70	—	ns	*3
$\overline{CE}$1 High Setup Time following CE2 High after Power Down Exit	t_{CHS}	0	—	ns	*2

*1 : Applicable when RA = 0 (Reset to Asynchronous mode) .

*2 : Applicable also to power-up.

*3 : Applicable when Partial Power Down mode and Reset to Asynchronous mode are set.

(8) Other Timing Parameters

(At recommended operating conditions unless otherwise noted)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
$\overline{CE}$1 High to $\overline{OE}$ Invalid Time for Standby Entry	t_{CHOX}	0	—	ns	
$\overline{CE}$1 High to $\overline{WE}$ Invalid Time for Standby Entry	t_{CHWX}	0	—	ns	*1
CE2 Low Hold Time after Power-up	t_{C2LH}	50	—	µs	
$\overline{CE}$1 High Hold Time following CE2 High after Power-up	t_{CHH}	300	—	µs	
Input Transition Time (except for CLK)	t_T	1	25	ns	*2, *3

*1 : Some data might be written into any address location if t_{CHWX} (Min) is not satisfied.

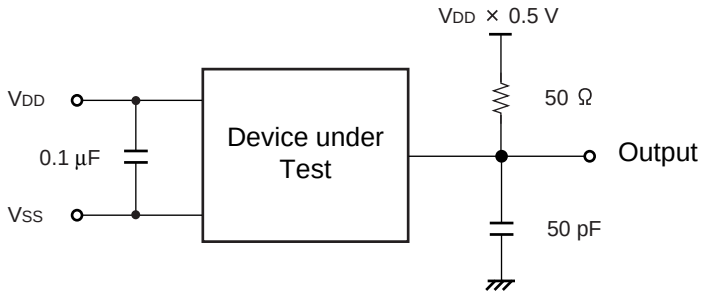
*2 : Except for the CLK input transition time.

*3 : The Input Transition Time (t_T) at AC testing is 3 ns for Asynchronous operation and 1.5 ns for Synchronous operation respectively. If actual t_T is longer than 3 ns or 1.5 ns specified as AC test condition, it may violate AC specification of some timing parameters. Refer to " (9) AC Test Conditions".

(9) AC Test Conditions

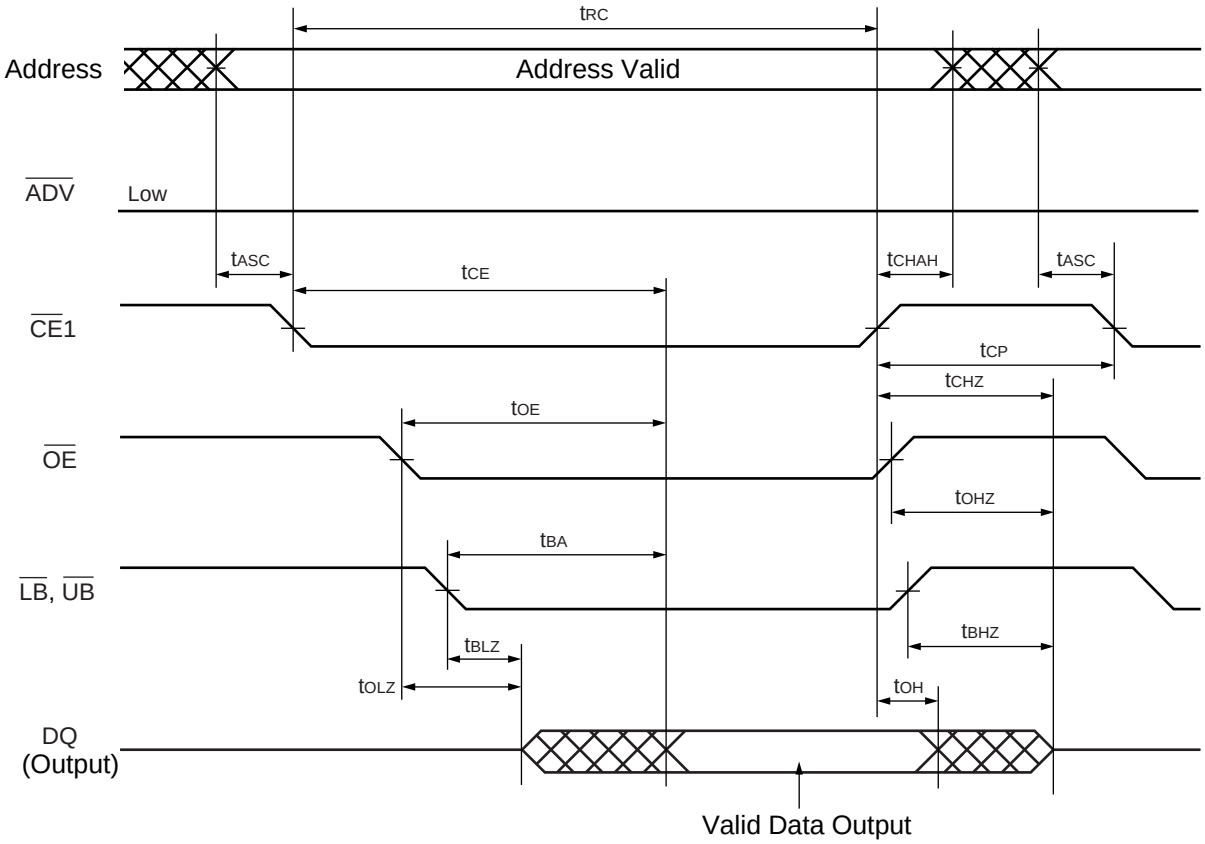
Description		Symbol	Test Setup	Value	Unit	Notes
Input High Level		V_{IH}	—	$V_{DD} \times 0.8$	V	
Input Low Level		V_{IL}	—	$V_{DD} \times 0.2$	V	
Input Timing Measurement Level		V_{REF}	—	$V_{DD} \times 0.5$	V	
Input Transition Time	Async.	t_T	Between V_{IL} and V_{IH}	3	ns	
	Sync.			1.5	ns	

• AC MEASUREMENT OUTPUT LOAD CIRCUIT



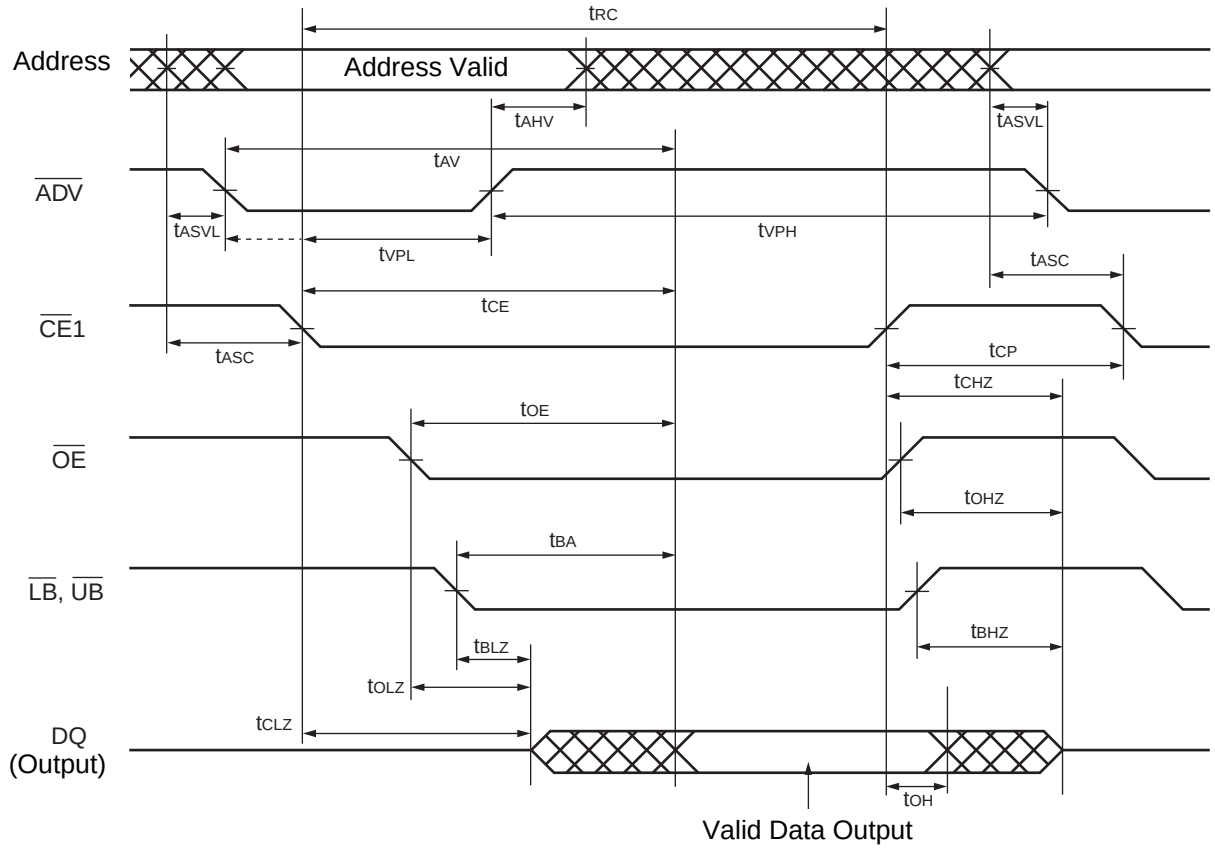
■ TIMING DIAGRAMS

(1) Asynchronous Read Timing 1-1 (Basic Timing)



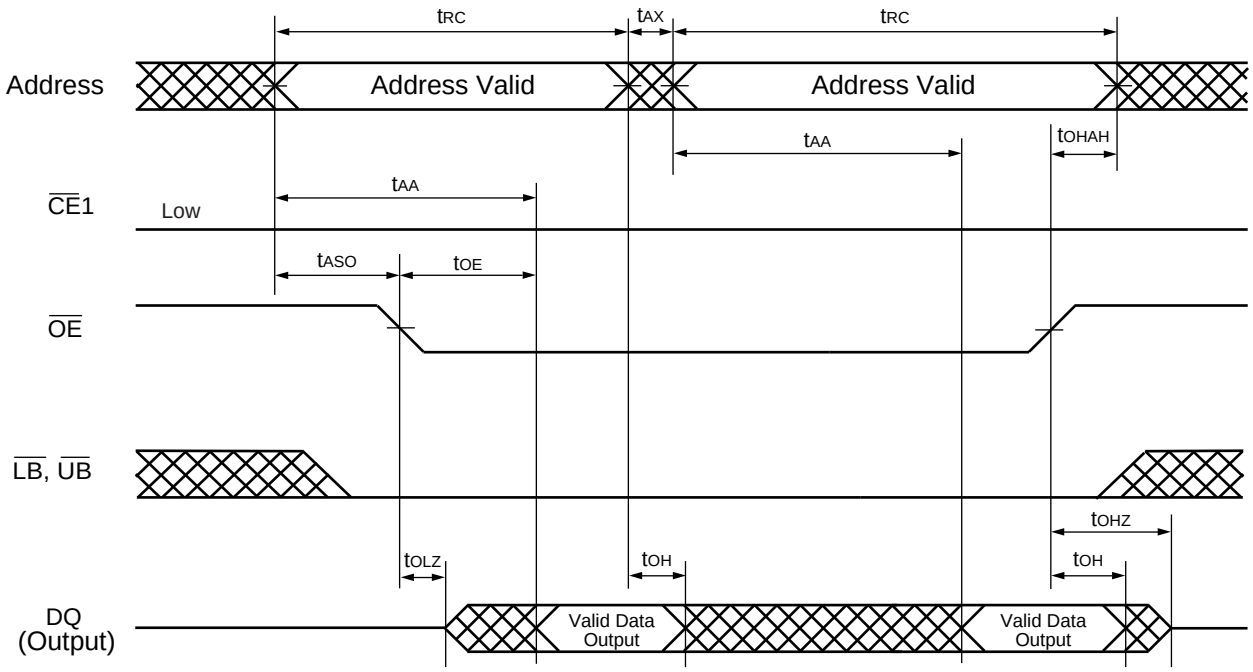
Note : This timing diagram assumes CE2 = H and $\overline{WE}$ = H.

(2) Asynchronous Read Timing 1-2 (Basic Timing)



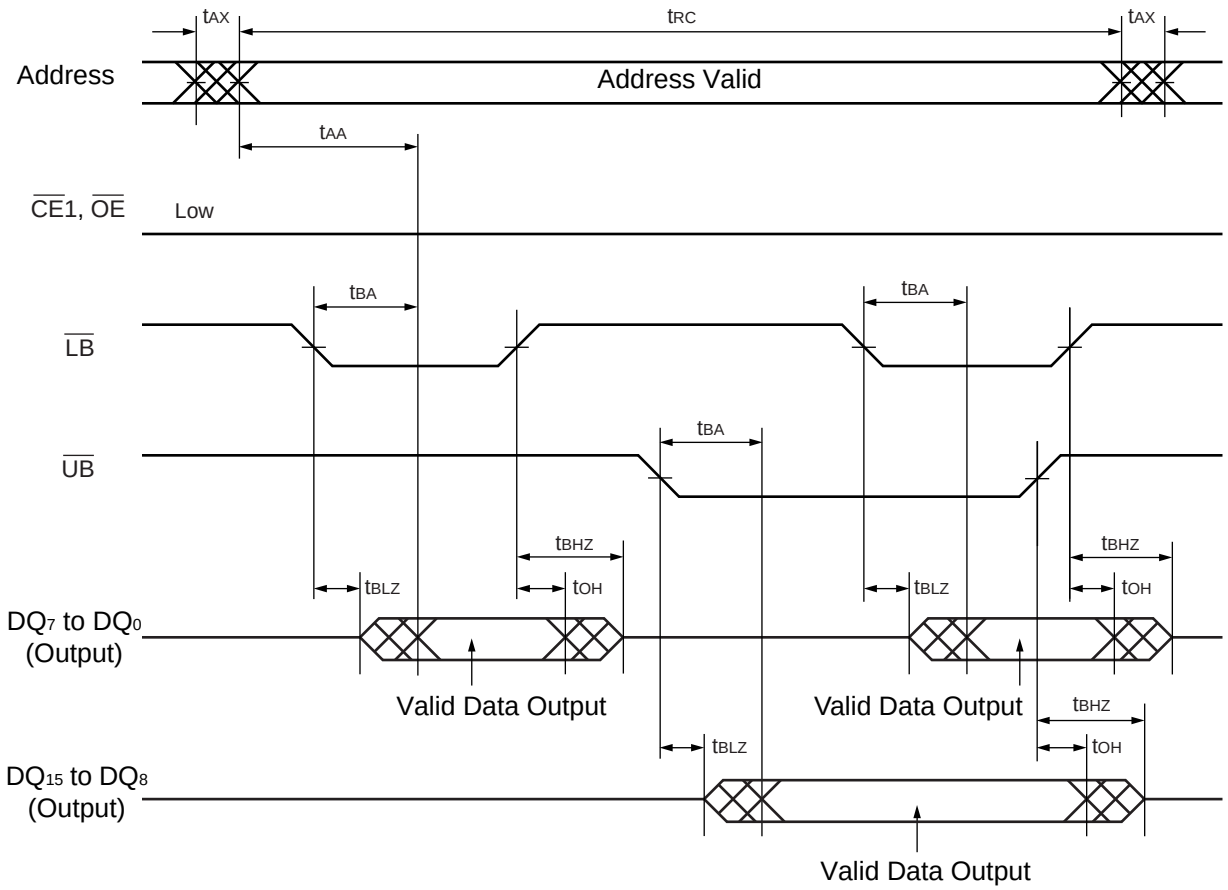
Note : This timing diagram assumes CE2 = H and $\overline{WE}$ = H.

(3) Asynchronous Read Timing 2 ($\overline{OE}$ Control & Address Access)



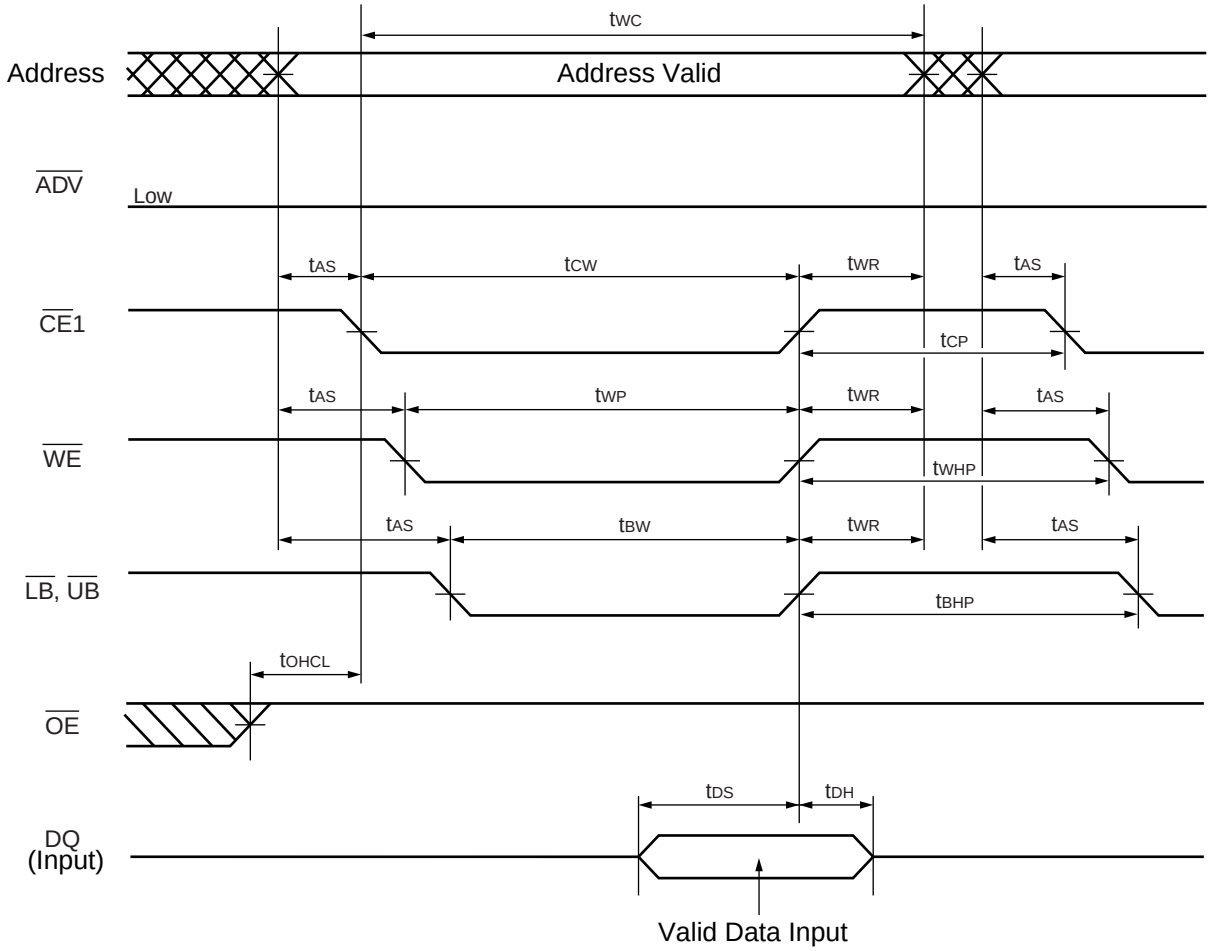
Note : This timing diagram assumes CE2 = H, $\overline{ADV}$ = L and $\overline{WE}$ = H.

(4) Asynchronous Read Timing 3 ($\overline{LB}$, $\overline{UB}$ Byte Control Access)



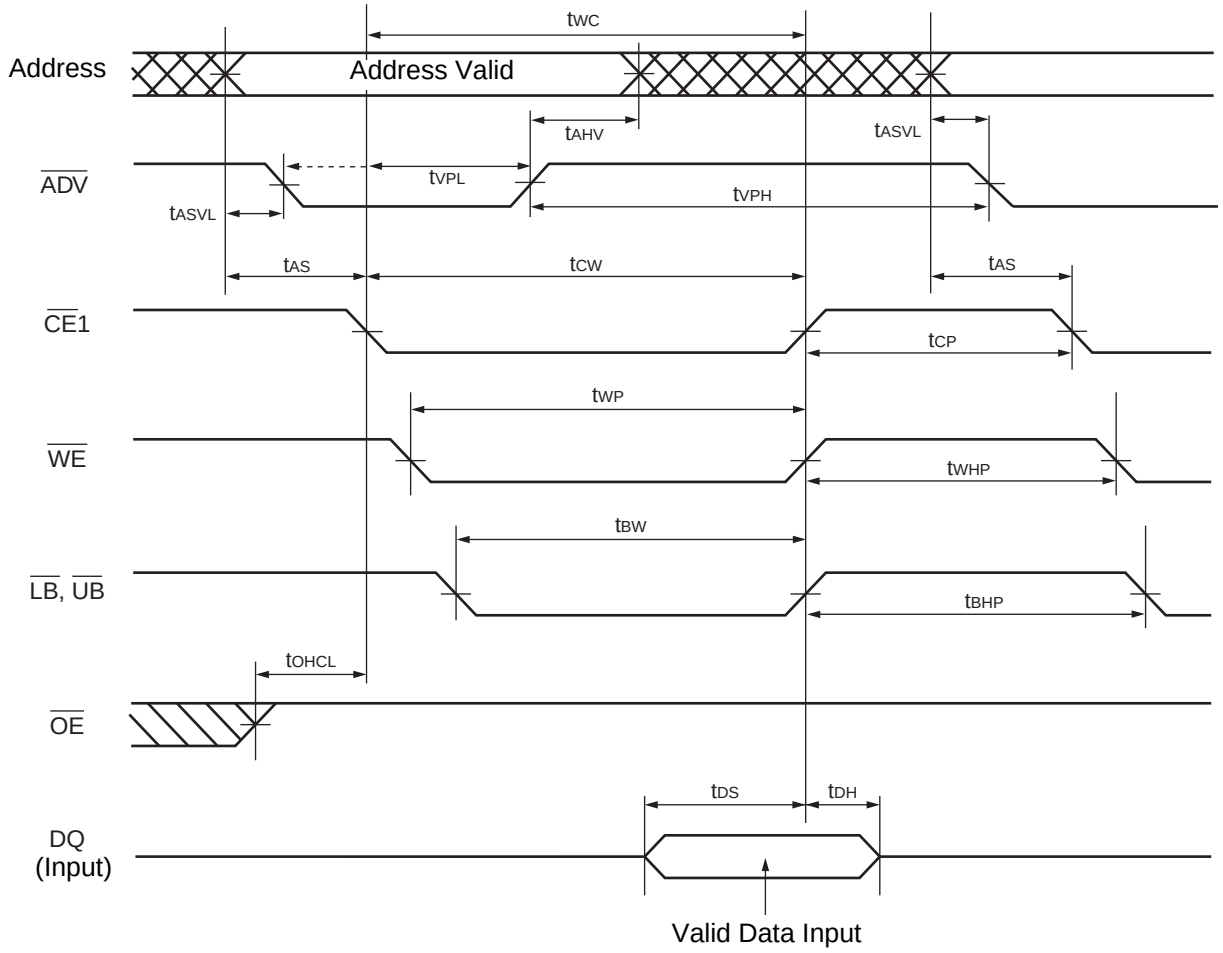
Note : This timing diagram assumes CE2 = H, $\overline{ADV}$ = L and $\overline{WE}$ = H.

(5) Asynchronous Write Timing 1-1 (Basic Timing)



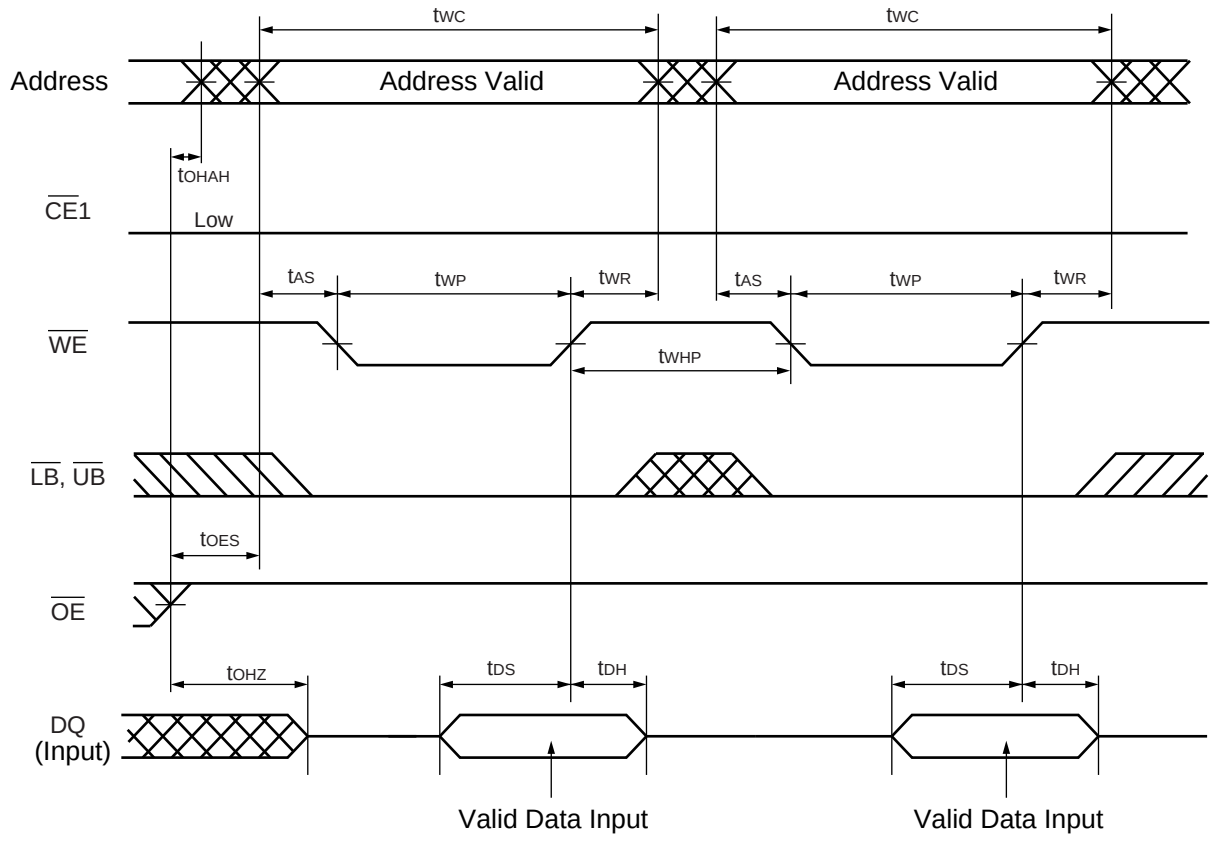
Note : This timing diagram assumes CE2 = H.

(6) Asynchronous Write Timing 1-2 (Basic Timing)



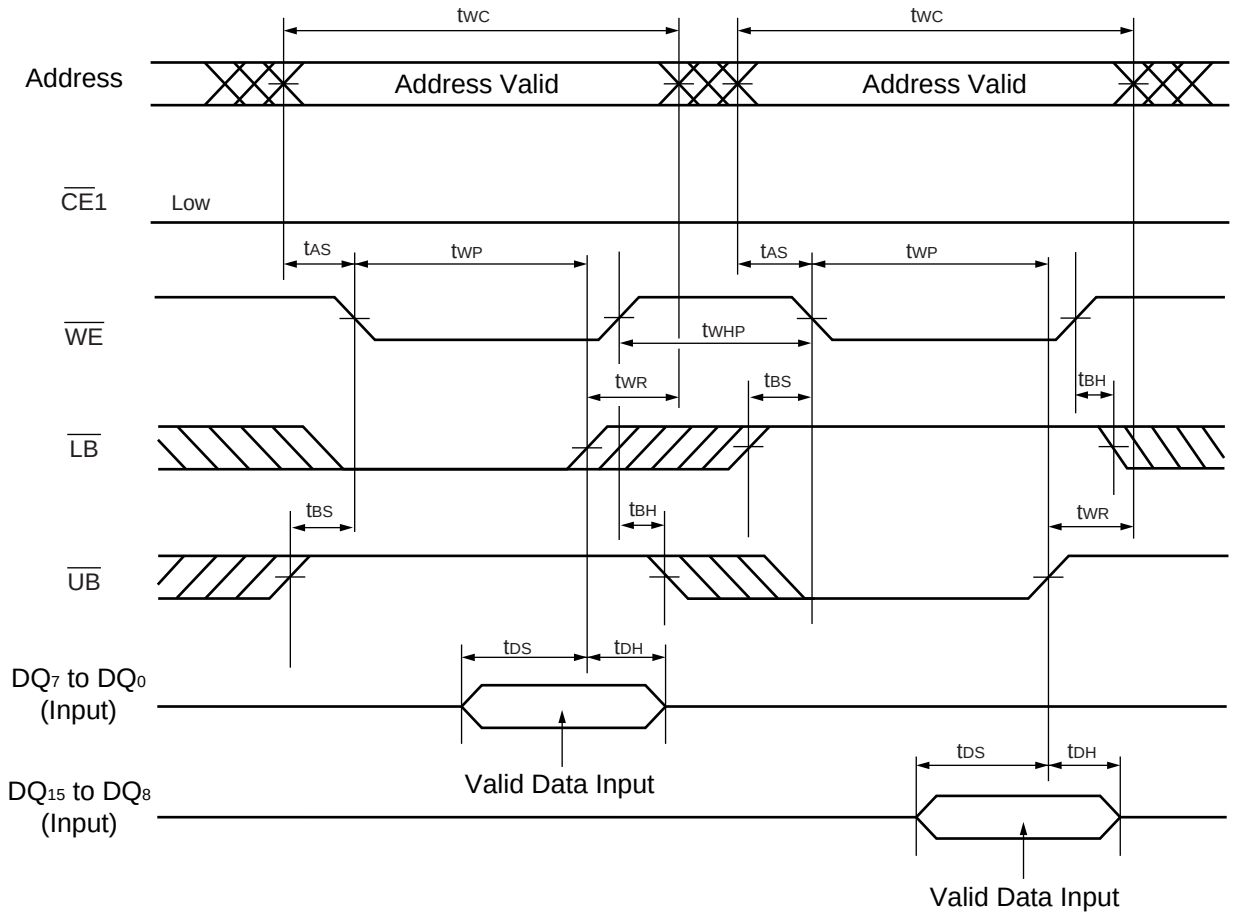
Note : This timing diagram assumes CE2 = H.

(7) Asynchronous Write Timing 2 ($\overline{WE}$ Control)



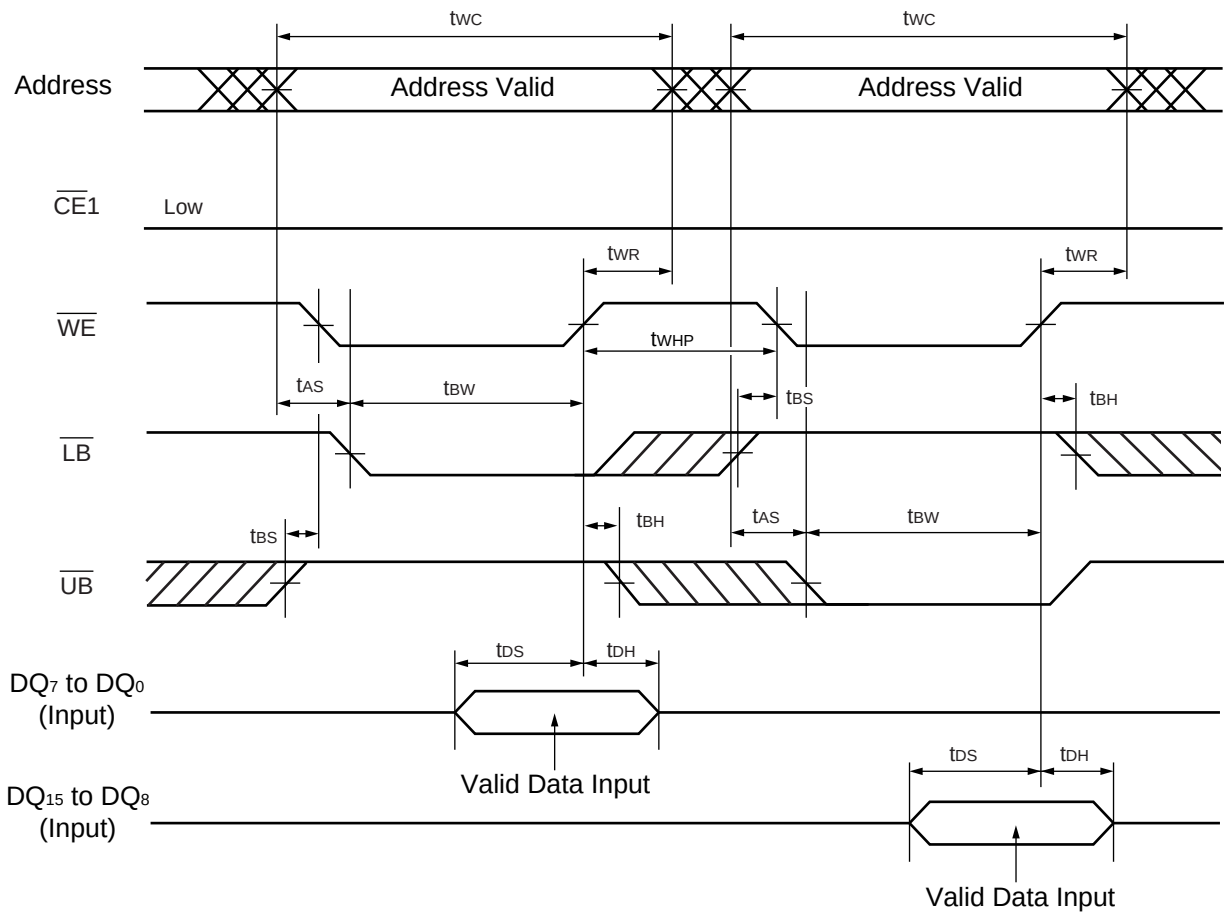
Note : This timing diagram assumes CE2 = H and $\overline{ADV}$ = L.

(8) Asynchronous Write Timing 3-1 ($\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Byte Write Control)



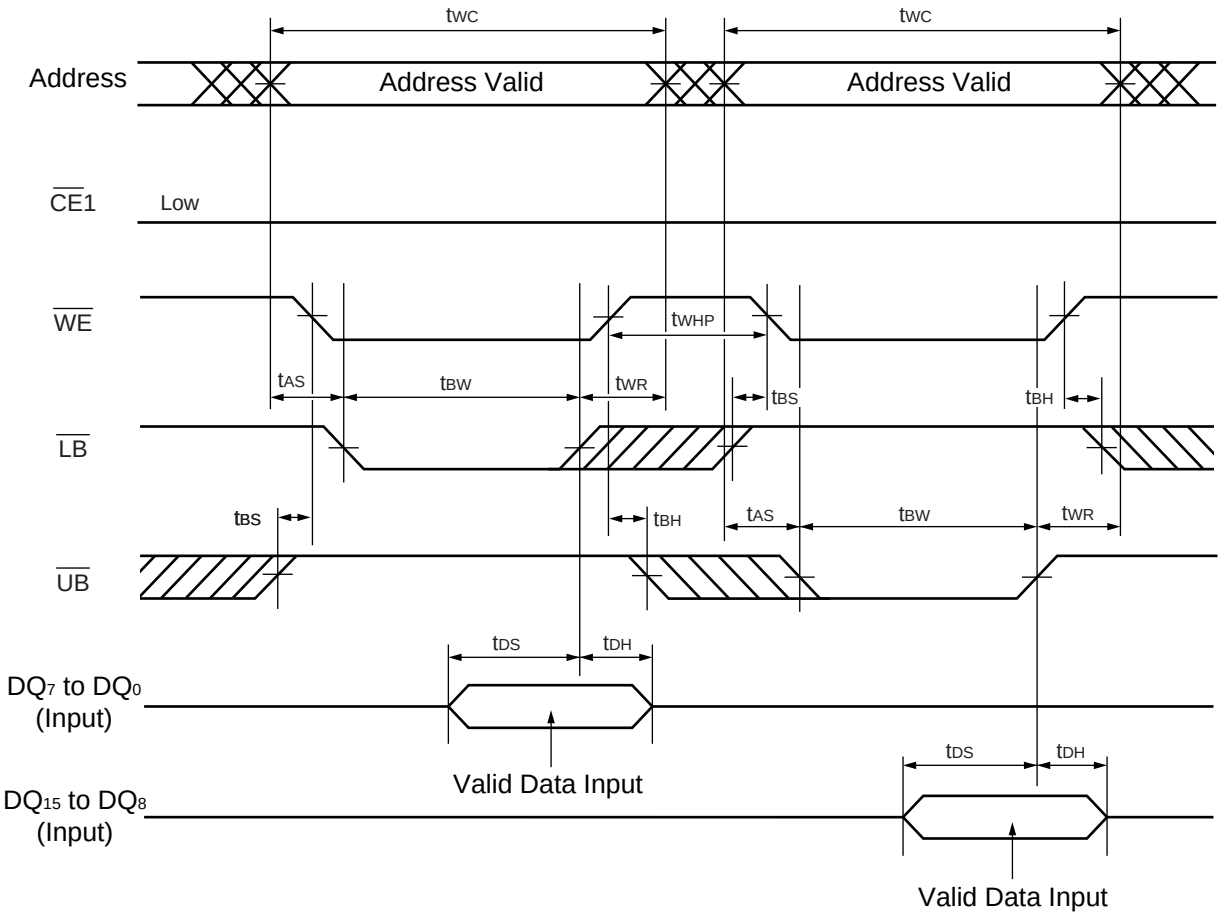
Note : This timing diagram assumes CE2 = H, $\overline{ADV}$ = L and $\overline{OE}$ = H.

(9) Asynchronous Write Timing 3-2 ($\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Byte Write Control)



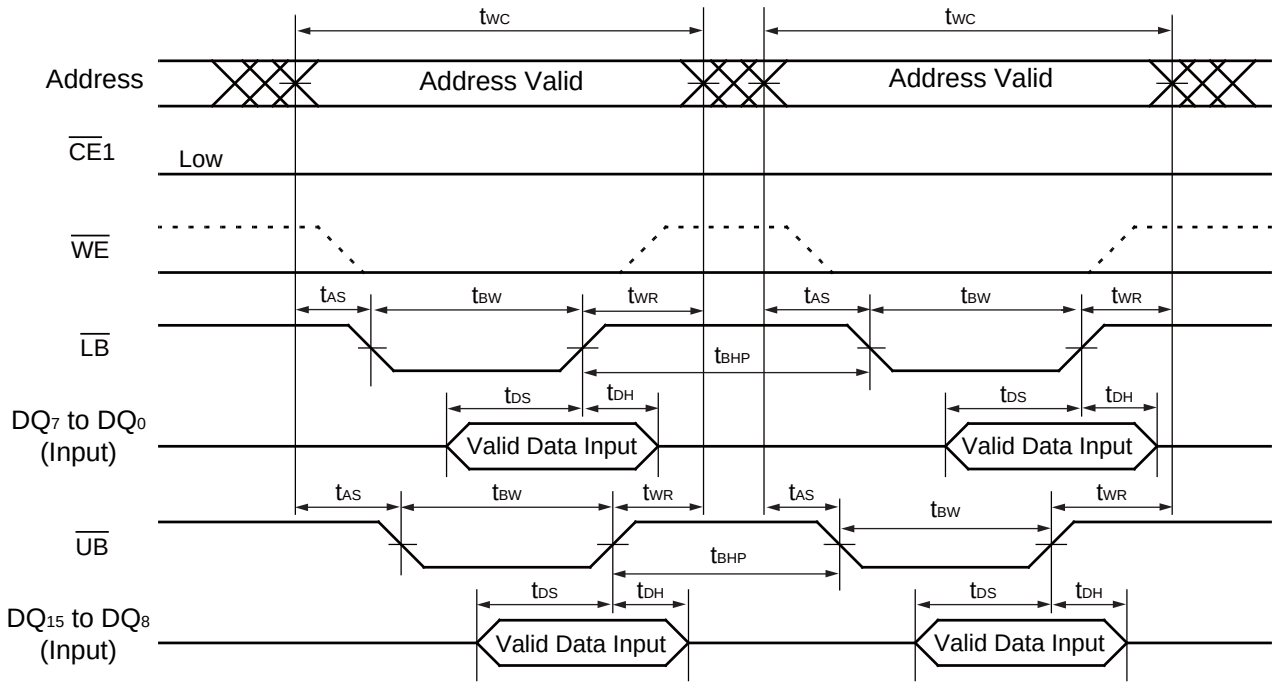
Note : This timing diagram assumes CE2 = H, $\overline{ADV}$ = L and $\overline{OE}$ = H.

(10) Asynchronous Write Timing 3-3 ($\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Byte Write Control)



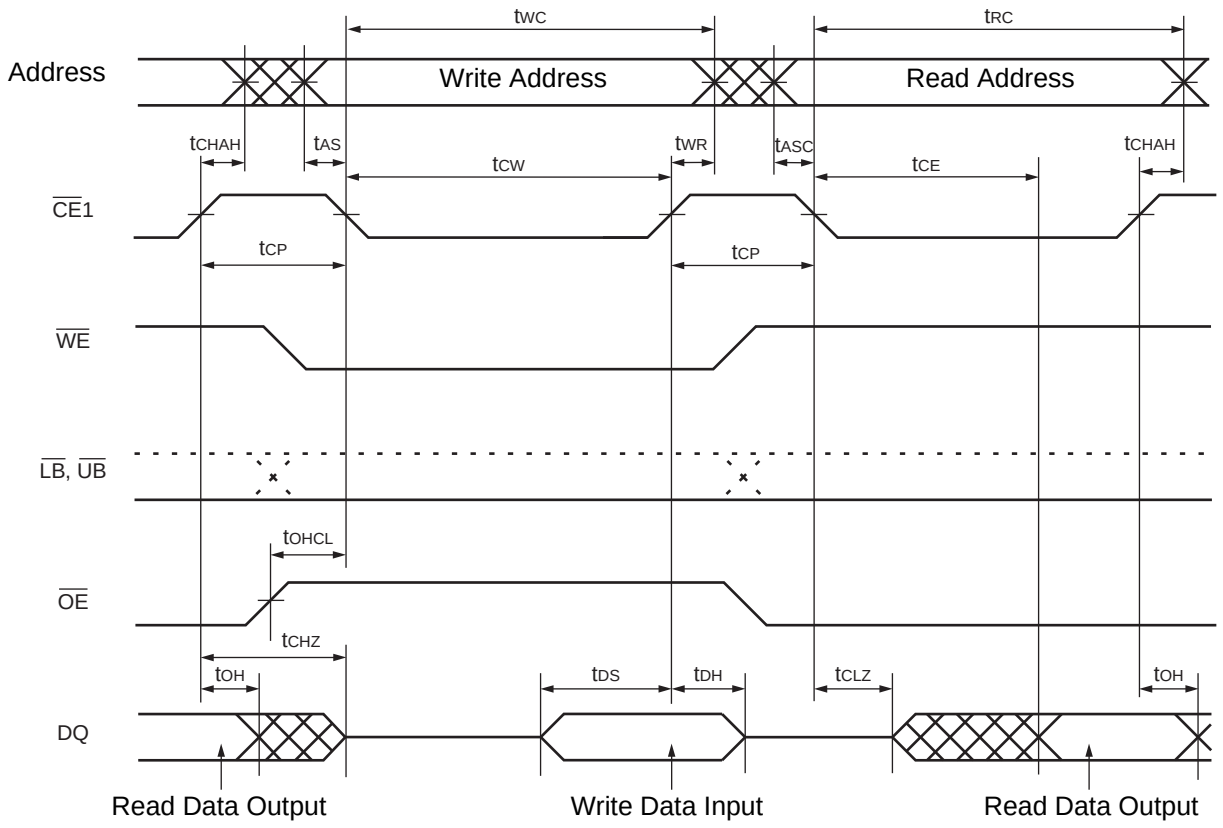
Note : This timing diagram assumes CE2 = H, $\overline{ADV}$ = L and $\overline{OE}$ = H.

(11) Asynchronous Write Timing 3-4 ($\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Byte Write Control)



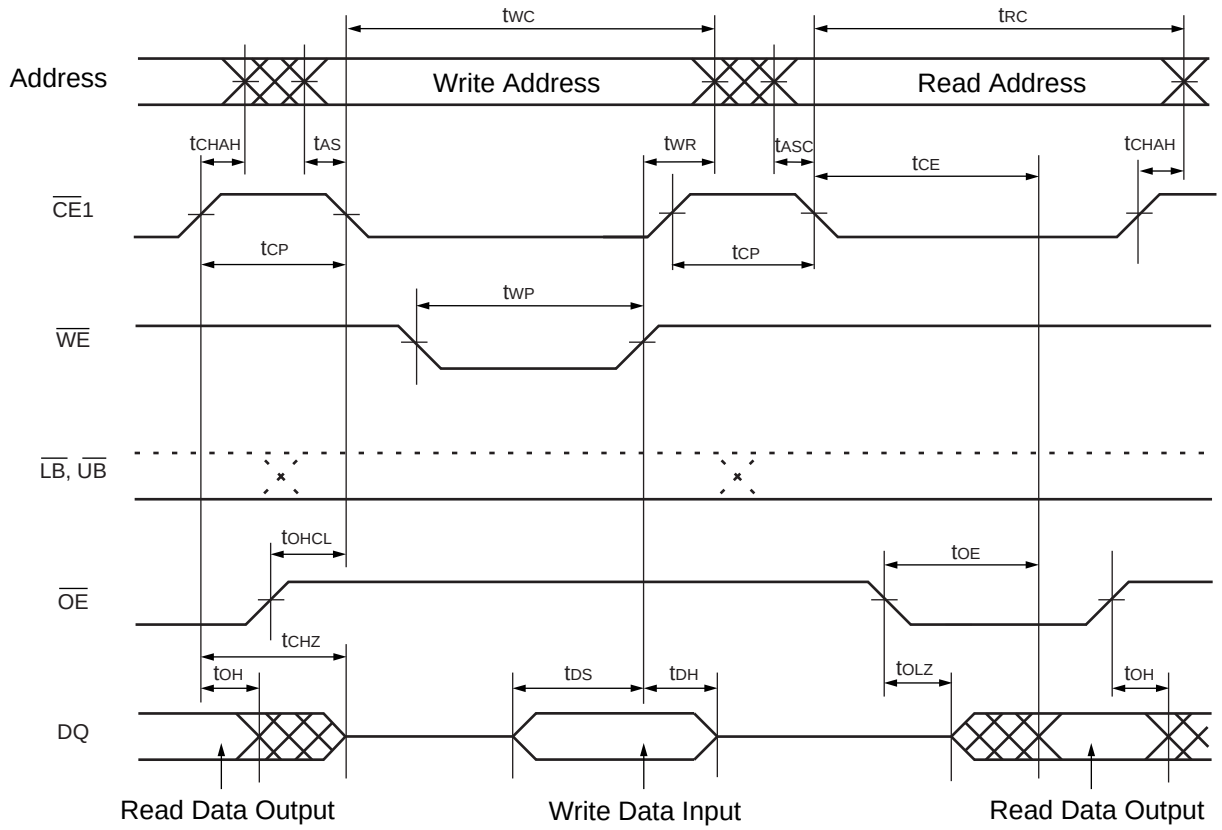
Note : This timing diagram assumes CE2 = H, $\overline{ADV}$ = L and $\overline{OE}$ = H.

(12) Asynchronous Read/Write Timing 1-1 ($\overline{CE}$1 Control)



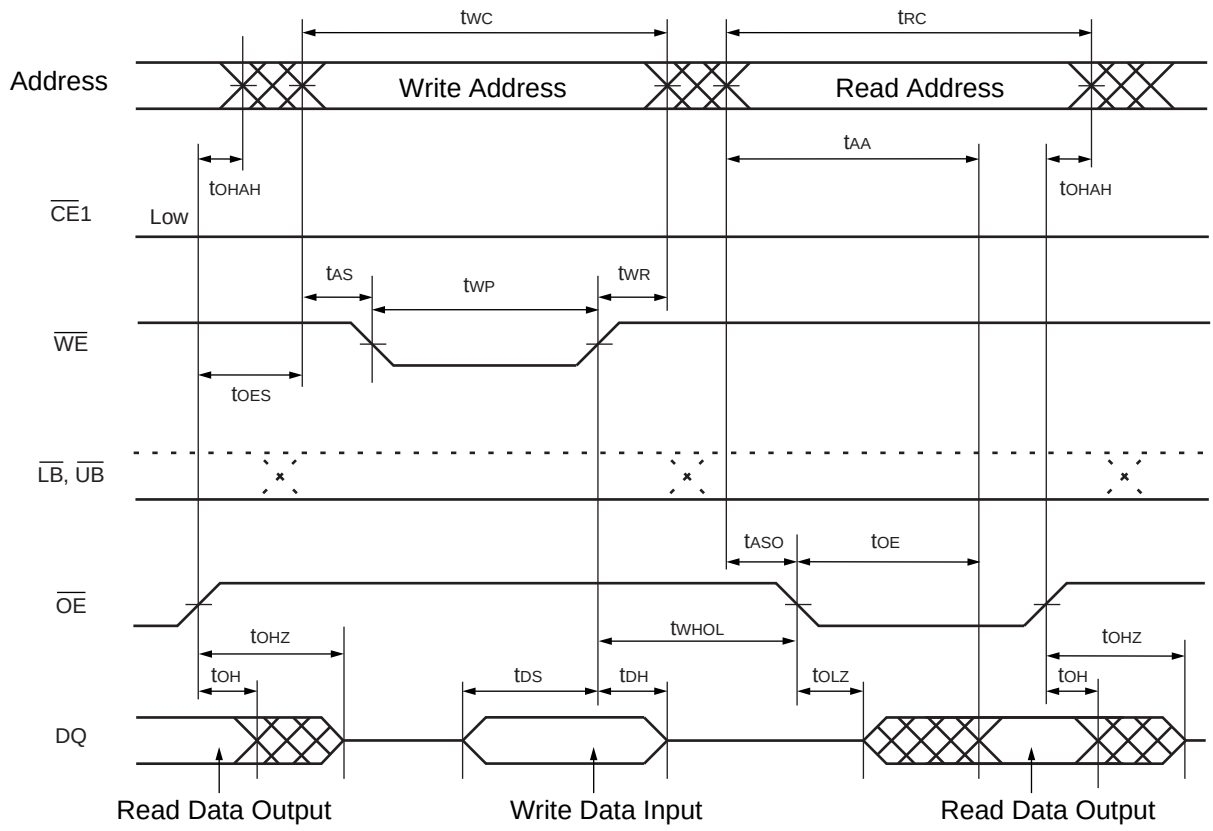
Notes : • This timing diagram assumes CE2 = H and $\overline{ADV}$ = L.
• Write address is valid from either $\overline{CE}$1 or $\overline{WE}$ of last falling edge.

(13) Asynchronous Read/Write Timing 1-2 ($\overline{CE}$1, $\overline{WE}$, $\overline{OE}$ Control)



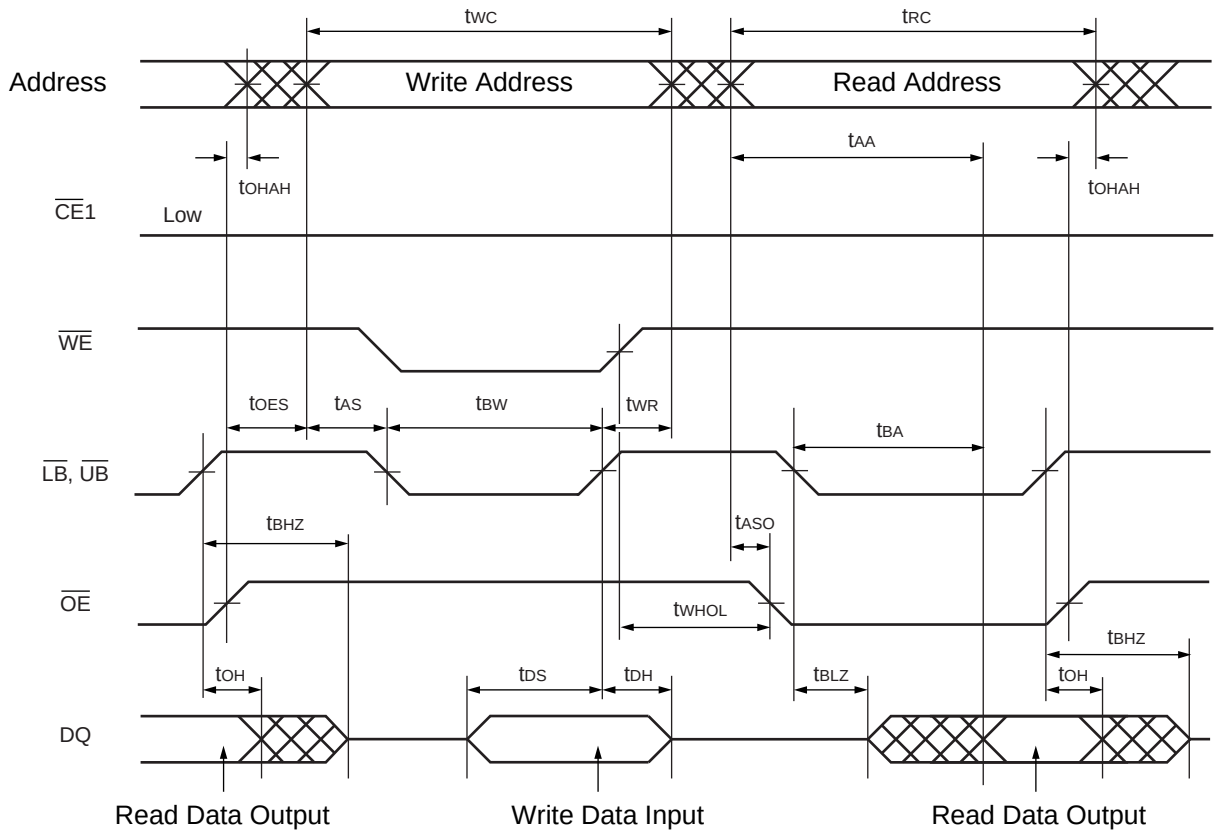
Notes : • This timing diagram assumes CE2 = H and $\overline{ADV}$ = L.
• $\overline{OE}$ can be fixed Low during write operation if it is $\overline{CE}$1 controlled write at Read-Write-Read sequence.

(14) Asynchronous Read/Write Timing 2 ($\overline{OE}$, $\overline{WE}$ Control)



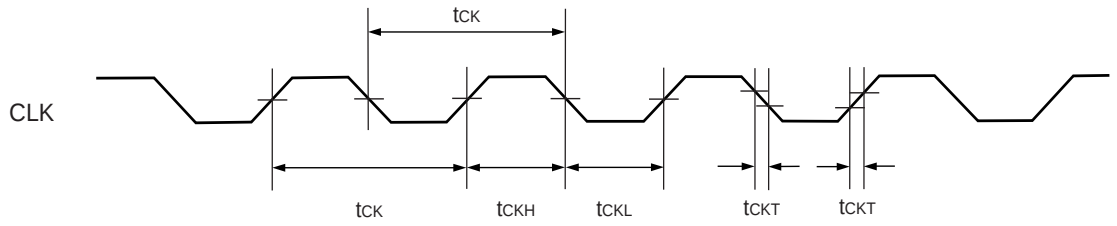
Notes : • This timing diagram assumes CE2 = H and $\overline{ADV}$ = L.
- $\overline{CE}$1 can be tied to Low for $\overline{WE}$ and $\overline{OE}$ controlled operation.
- Read data will be available after t_{AA} from $\overline{WE}$ = H if read addresses are not changed from write address.

(15) Asynchronous Read/Write Timing 3 ($\overline{OE}$, $\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Control)



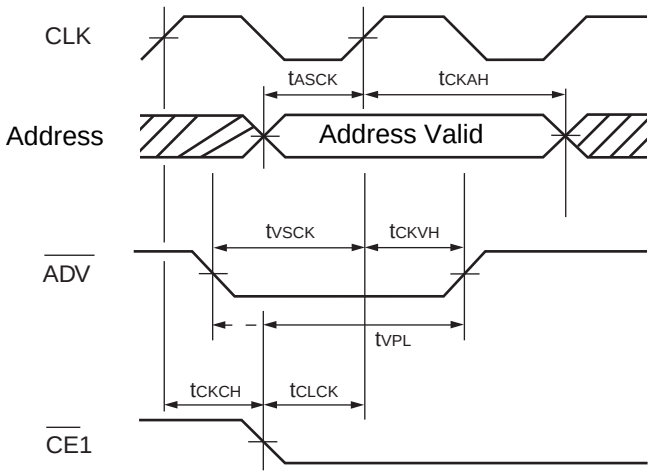
Notes : • This timing diagram assumes CE2 = H and $\overline{ADV}$ = L.
• $\overline{CE}$1 can be tied to Low for $\overline{WE}$ and $\overline{OE}$ controlled operation.
• Read data will be available after t_{AA} from $\overline{WE}$ = H if read addresses are not changed from write address.

(16) Clock Input Timing



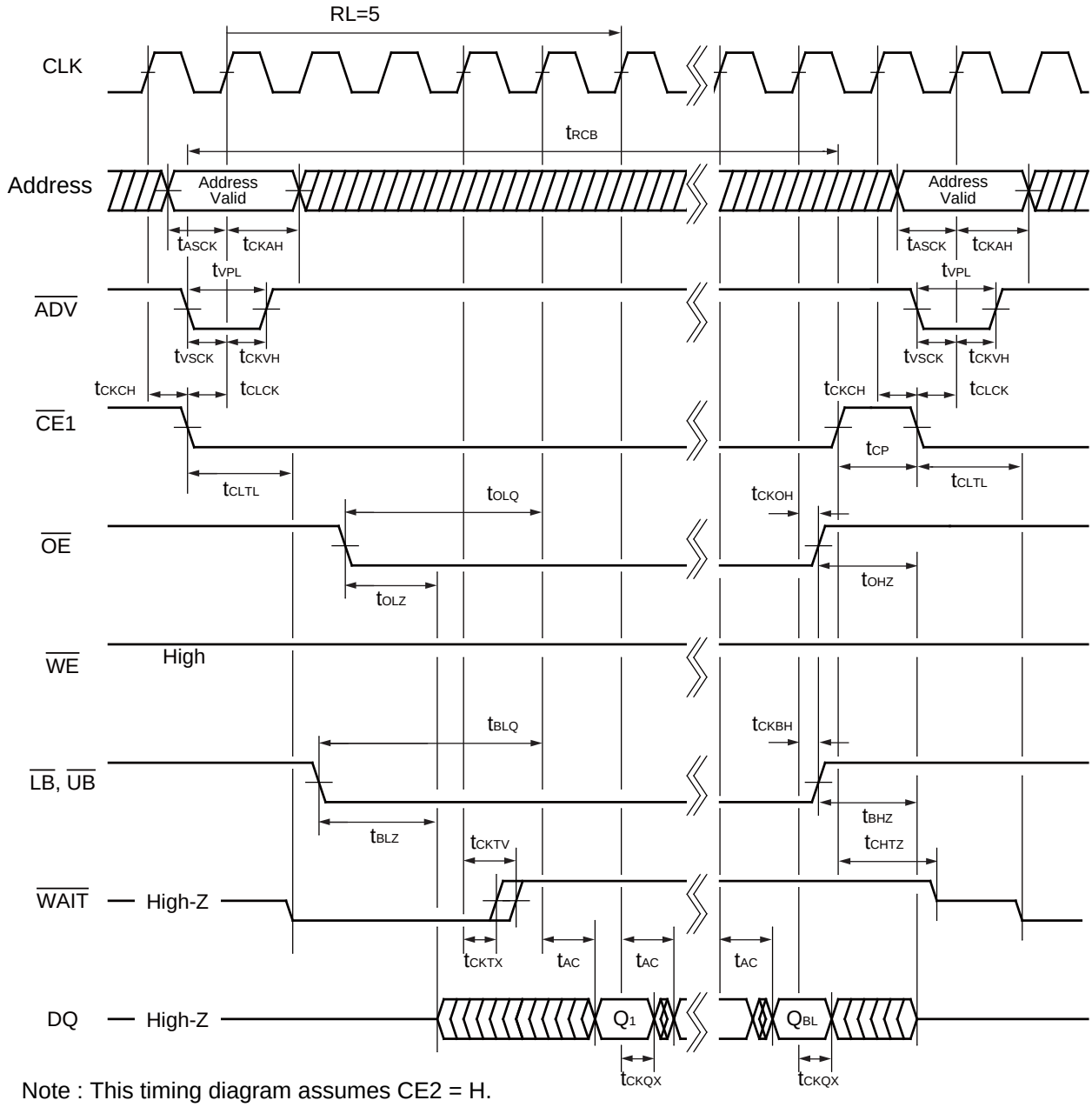
Notes : • Stable clock input must be required during $\overline{CE}1$ = L.
• t_{CK} is defined between rising clock edges.
• t_{CKT} is defined between V_{IH} (Min) and V_{IL} (Max).

(17) Address Latch Timing (Synchronous Mode)



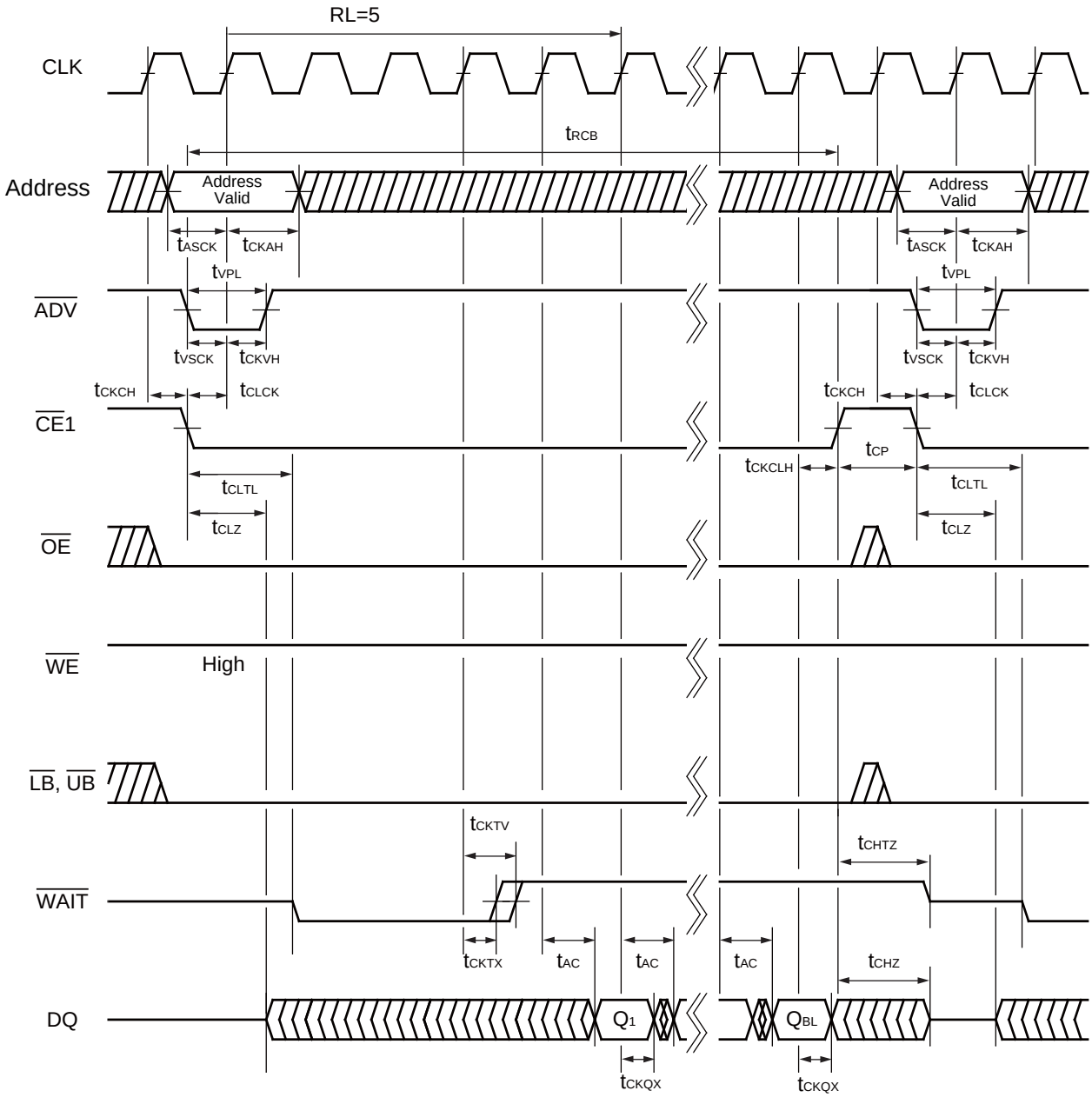
Notes : • t_{VPL} is specified from the falling edge of either $\overline{CE}1$ or $\overline{ADV}$ whichever comes late.
At least one rising clock edge must be input during $\overline{ADV}$ = L.
• t_{ASCK}, t_{VSCK} and t_{CLCK} are applied to the 1st valid clock edge during $\overline{ADV}$ = L.
• t_{CKCH} is applied to the rising clock edge before address latching.

(18) Synchronous Read Timing 1 ($\overline{OE}$ Control)



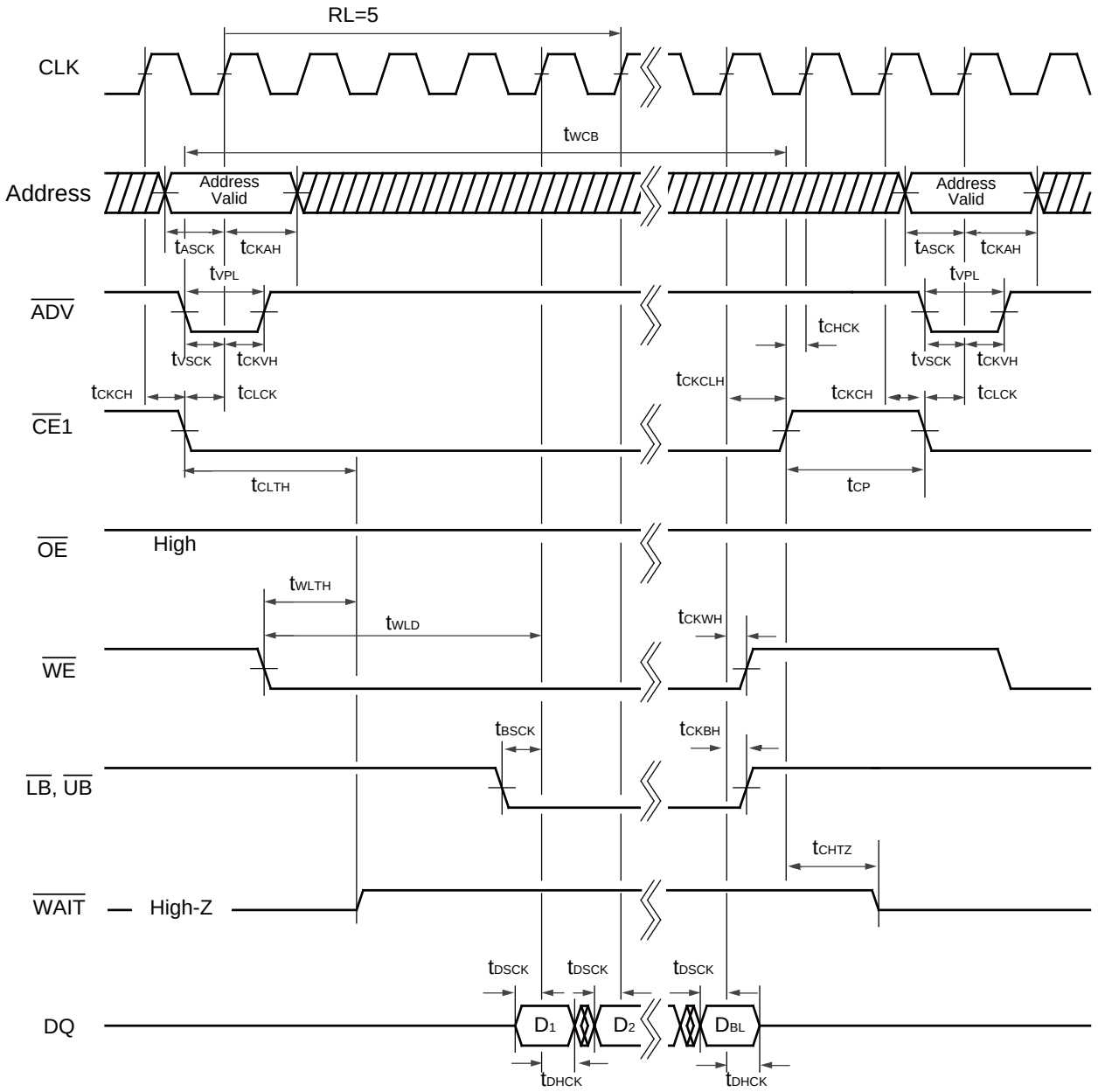
Note : This timing diagram assumes CE2 = H.

(19) Synchronous Read Timing 2 ($\overline{CE}$1 Control)



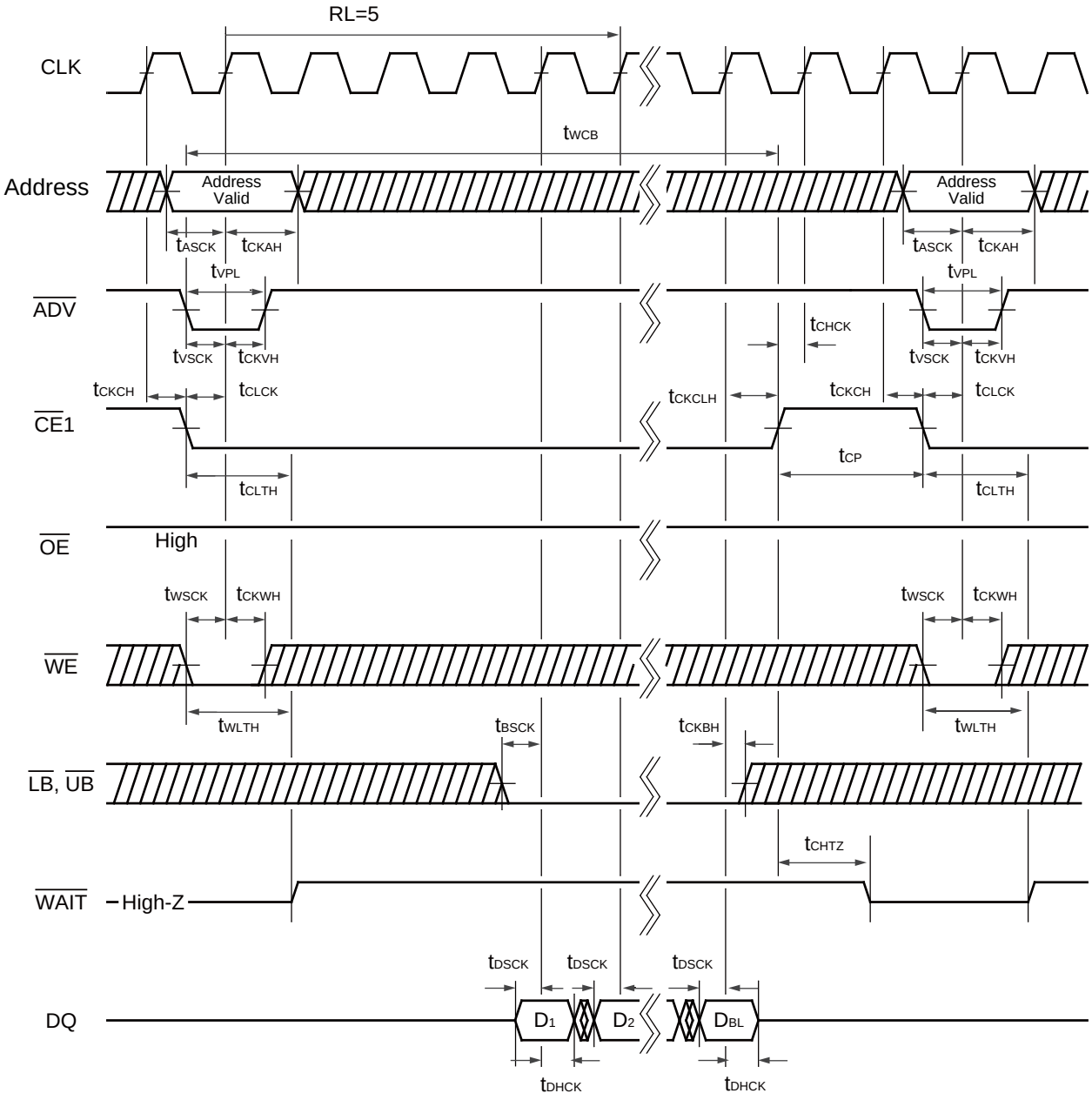
Note : This timing diagram assumes CE2 = H.

(20) Synchronous Write Timing 1 ($\overline{WE}$ Level Control)



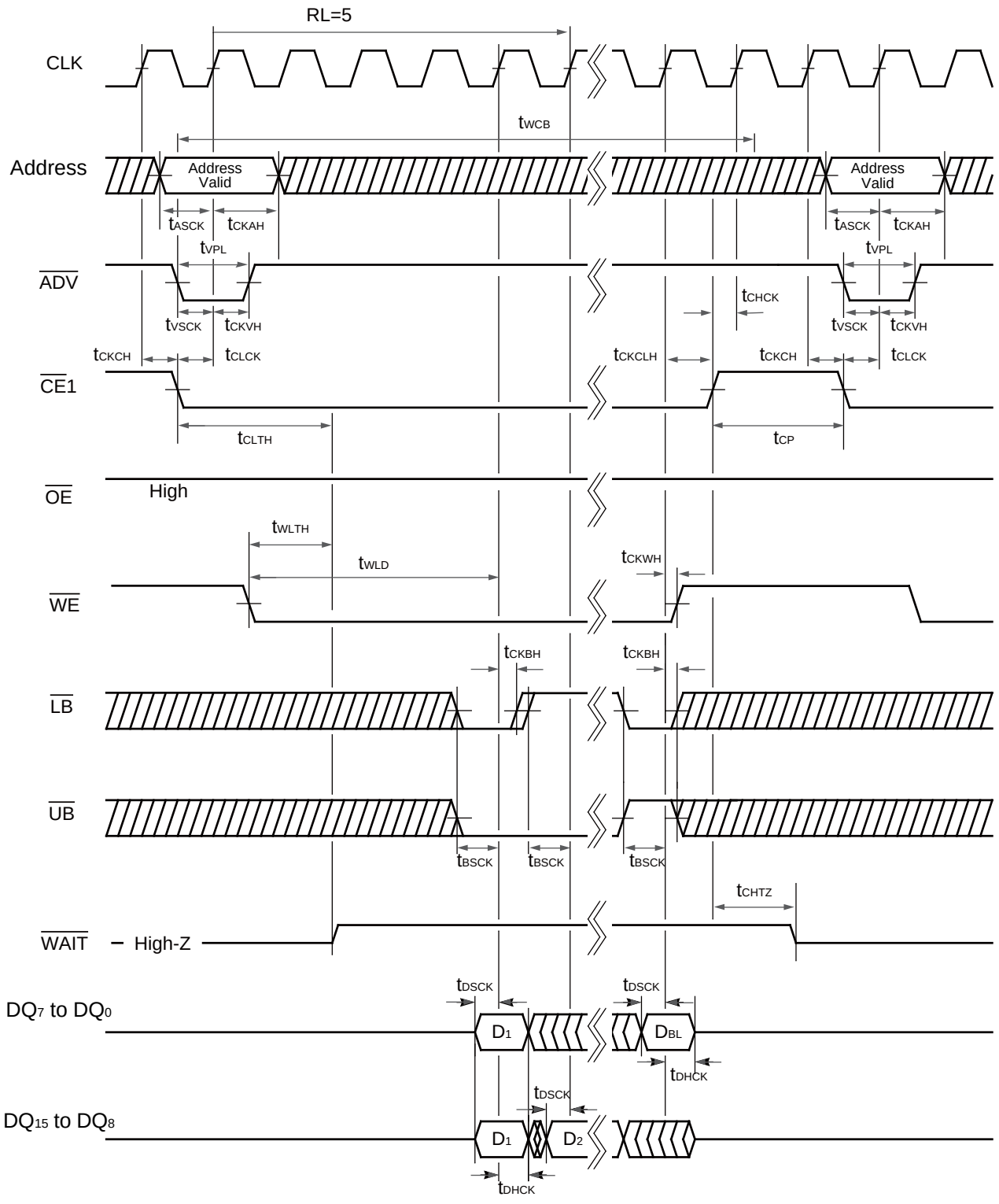
Note : This timing diagram assumes CE2 = H.

(21) Synchronous Write Timing 2 ($\overline{WE}$ Single Clock Pulse Control)



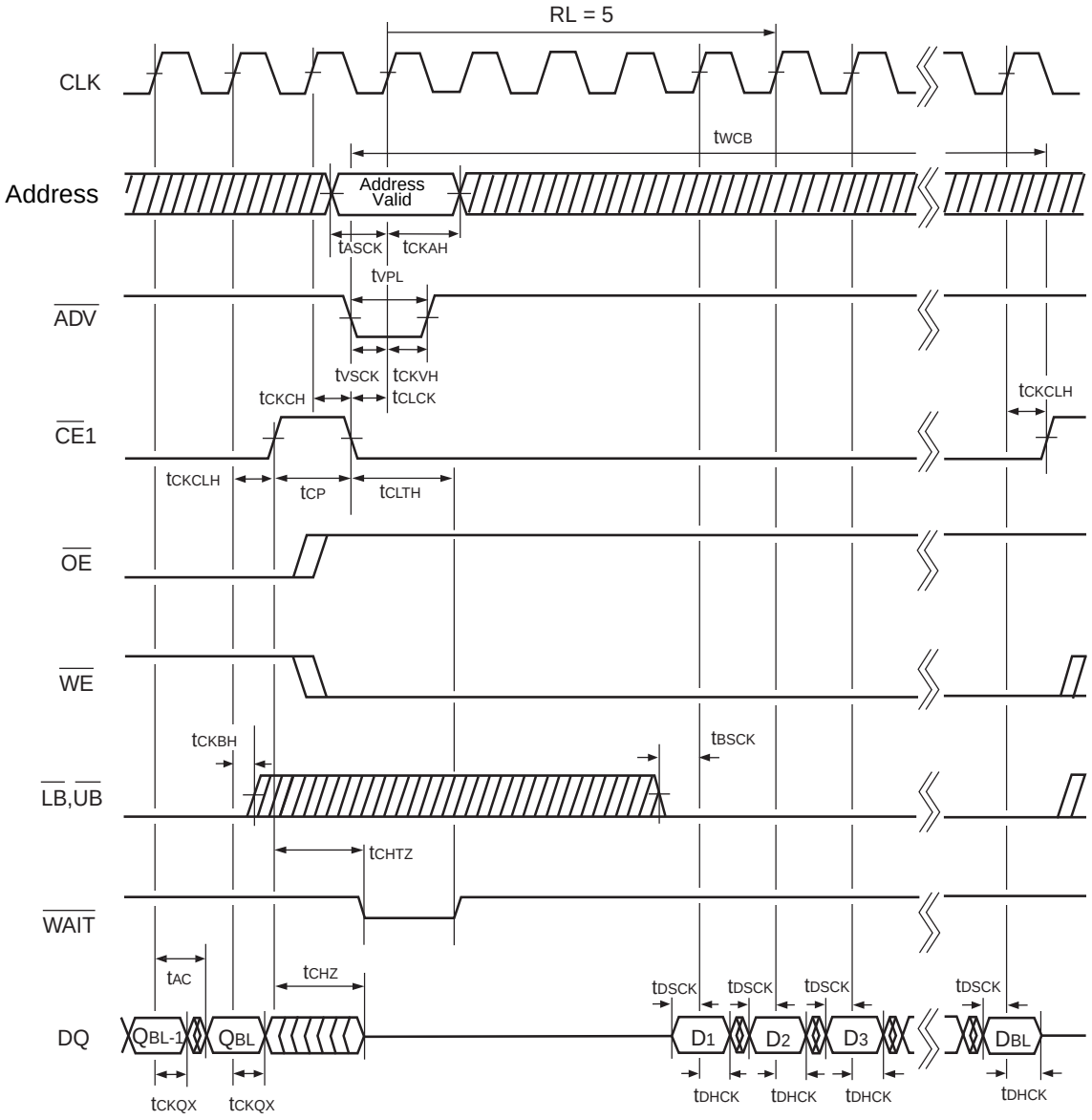
Note : This timing diagram assumes CE2 = H.

(22) Synchronous Write Timing 3 ($\overline{LB}$, $\overline{UB}$ Byte Mask Control)



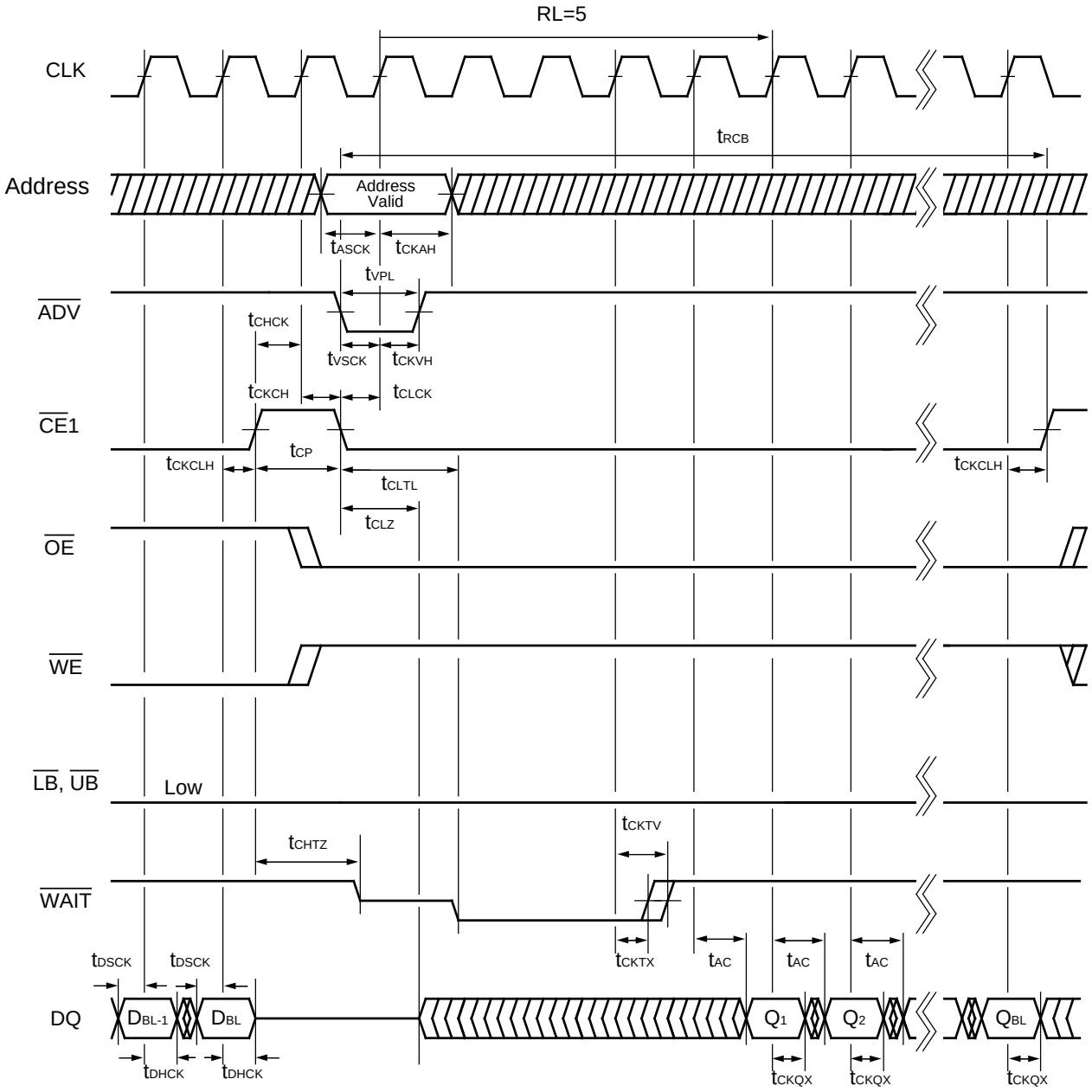
Note : This timing diagram assumes CE2 = H and $\overline{WE}$ Level Control.

(23) Synchronous Read to Write Timing 1 ($\overline{CE}$1 Control)



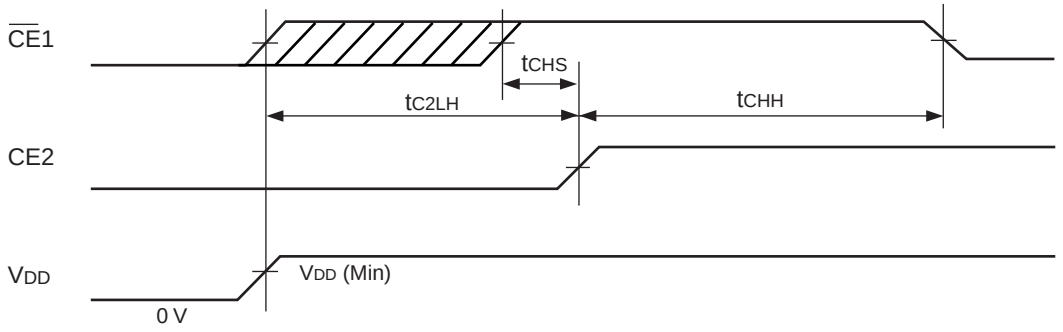
Note : This timing diagram assumes CE2 = H.

(24) Synchronous Write to Read Timing 1 ($\overline{CE}$1 Control)



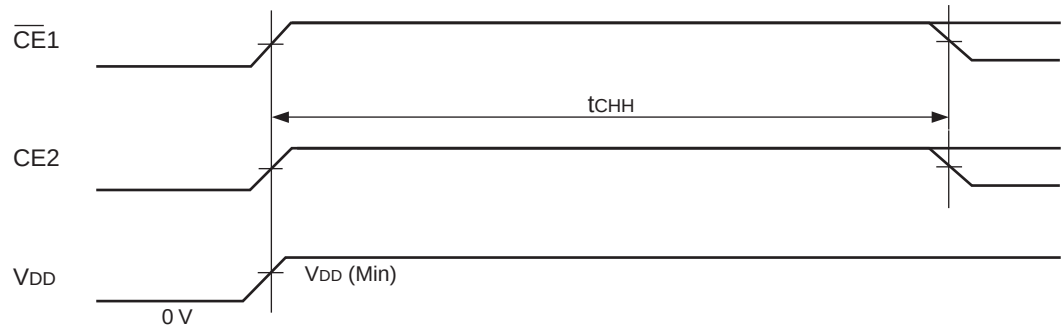
Note : This timing diagram assumes CE2 = H.

(25) Power-up Timing 1



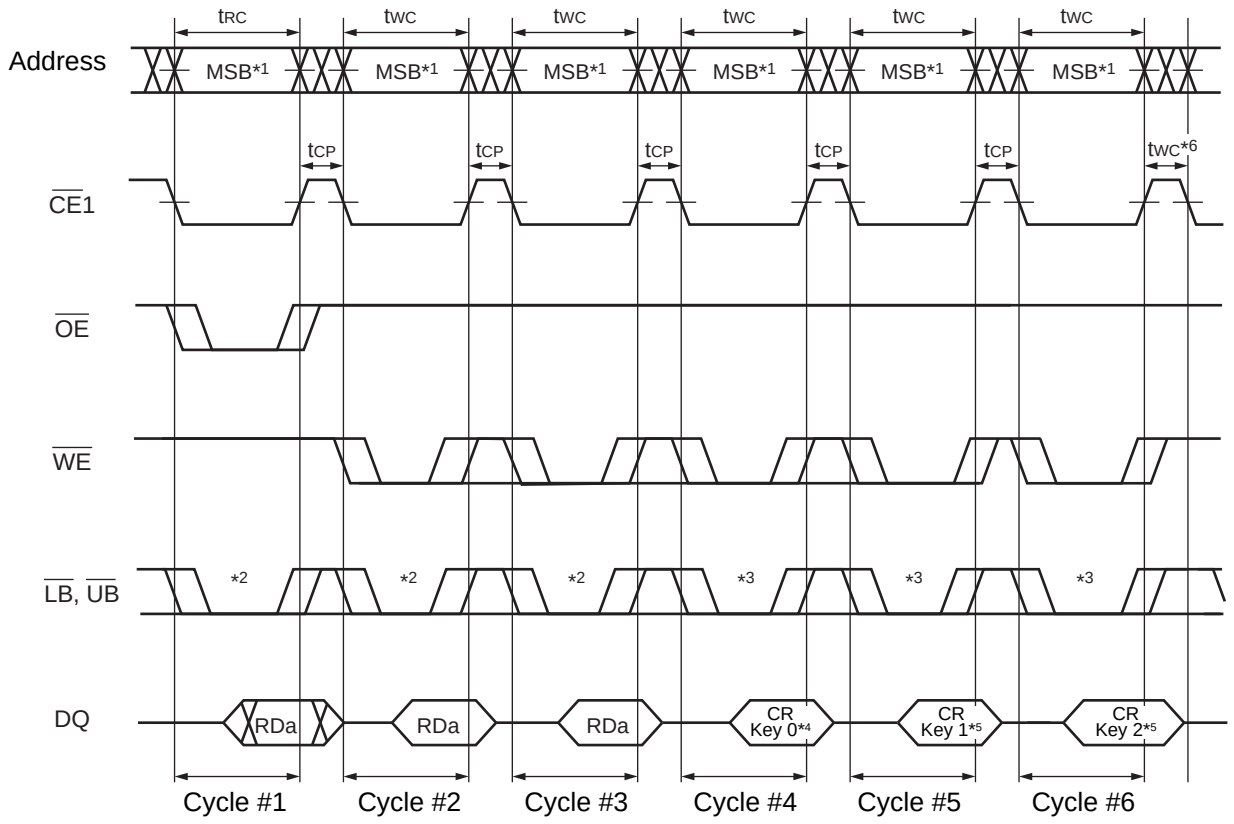
Note : The t_{C2LH} specifies after V_{DD} reaches specified minimum level.

(26) Power-up Timing 2



Note : The t_{CHH} specifies after V_{DD} reaches specified minimum level and applicable to both $\overline{CE}$1 and CE2. If transition time of V_{DD} (from 0 V to V_{DD} (Min)) is longer than 50 ms, (25) Power-up Timing 1 must be applied.

(29) Configuration Register Set Timing 1 (Asynchronous Operation)



*1 : The all address inputs must be High from Cycle #1 to #6.

*2 : At least either $\overline{LB}$ or $\overline{UB}$ must be brought to Low during Cycle #1 to #3.

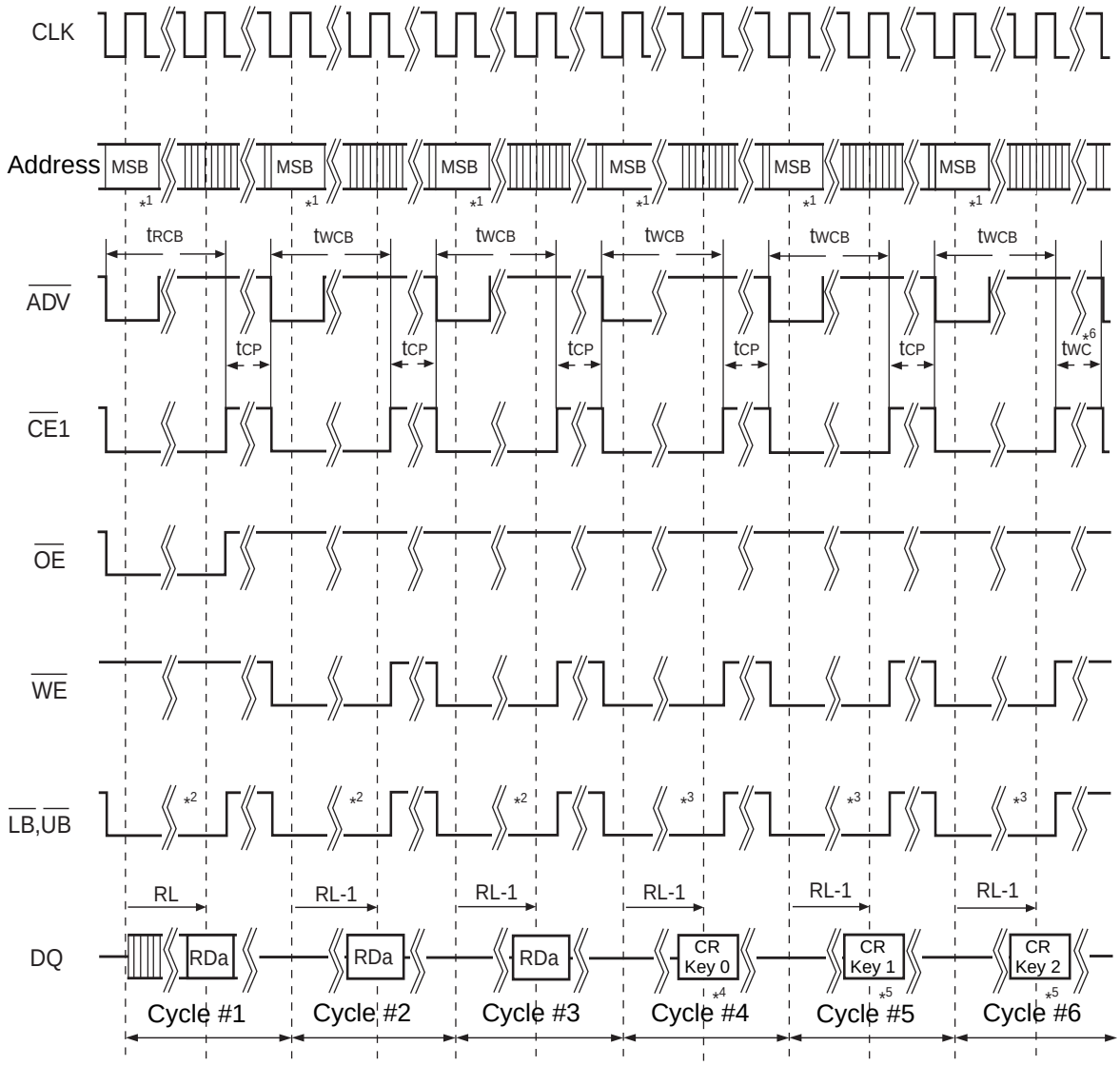
*3 : $\overline{LB}$ must be brought to Low in order to input the CR Keys during Cycle #4 to #6.

*4 : The CR Key 0 must be set “1” for the CR Set as specified in “■FUNCTIONAL DESCRIPTION”.

*5 : The CR Keys must conform to the format specified in “■FUNCTIONAL DESCRIPTION”. If not, any operations and data are not guaranteed.

*6 : After t_{WC} following Cycle #6, the Configuration Register Set is completed and returned to the normal operation.

(31) Configuration Register Set Timing 2 (Synchronous Operation)



*1 : The all address inputs must be High from Cycle #1 to #6.

*2 : At least either $\overline{LB}$ or $\overline{UB}$ must be brought to Low during Cycle #1 to #3.

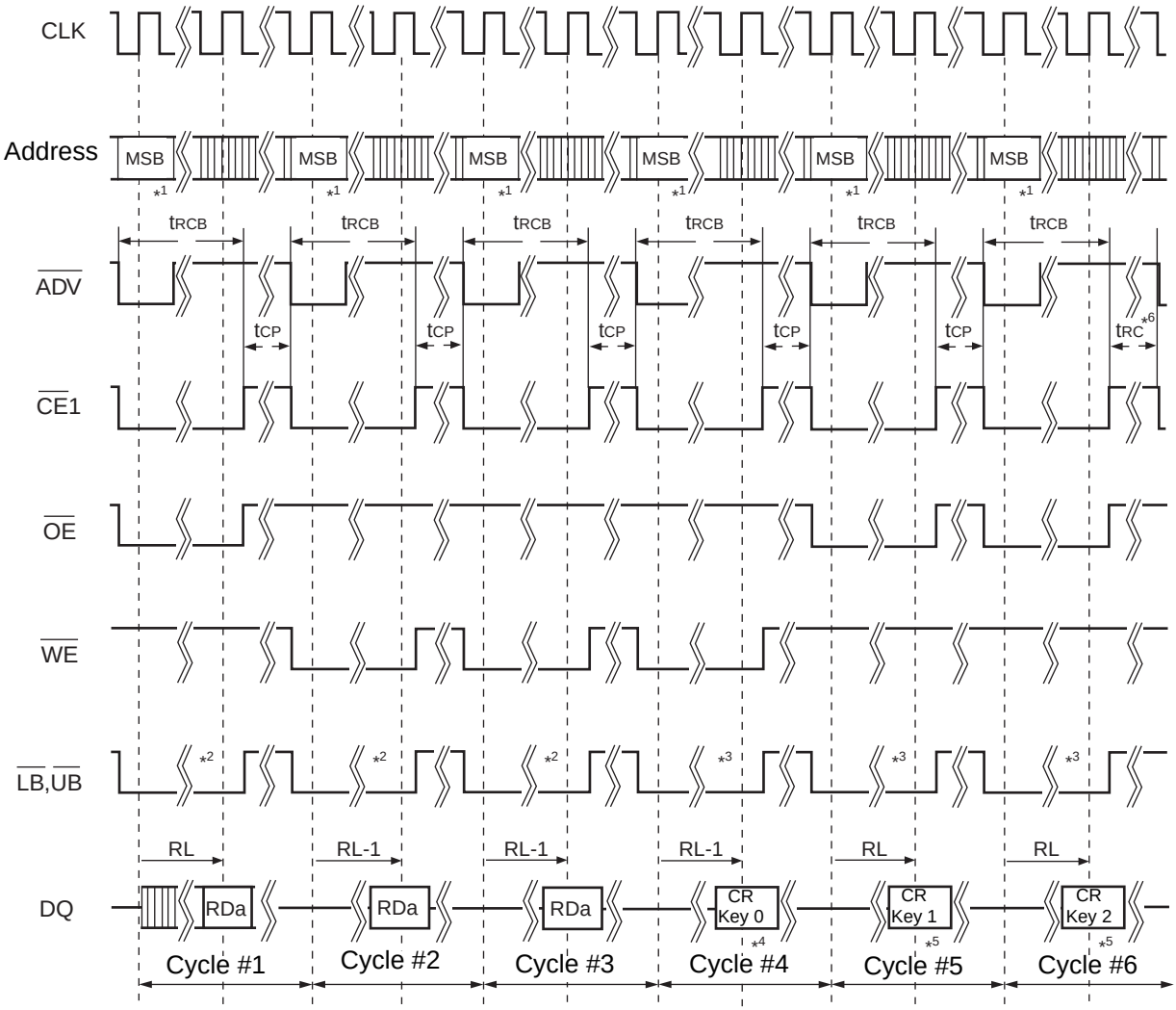
*3 : $\overline{LB}$ must be brought to Low in order to input the CR Keys during Cycle #4 to #6.

*4 : The CR Key 0 must be set “1” for the CR Set as specified in “■ FUNCTIONAL DESCRIPTION”.

*5 : The CR Keys must conform to the format specified in “■ FUNCTIONAL DESCRIPTION”. If not, any operations and data are not guaranteed.

*6 : After t_{WC} following Cycle #6, the Configuration Register Set is completed and returned to the normal operation.

(32) Configuration Register Verify Timing 2 (Synchronous Operation)



*1 : The all address inputs must be High from Cycle #1 to #6.

*2 : At least either $\overline{LB}$ or $\overline{UB}$ must be brought to Low during Cycle #1 to #3.

*3 : $\overline{LB}$ must be brought to Low in order to input or output the CR Keys during Cycle #4 to #6.

*4 : The CR Key 0 must be set “0” for the CR Verify as specified in “■FUNCTIONAL DESCRIPTION”.

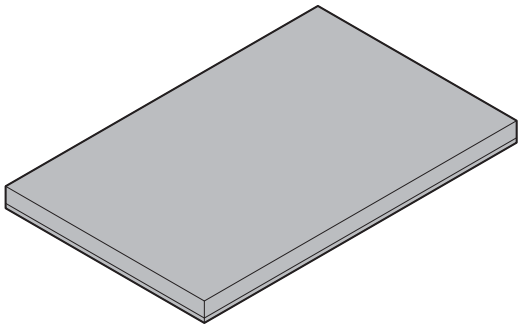
*5 : The CR Keys must conform to the format specified in “■FUNCTIONAL DESCRIPTION”. If not, any operations and data are not guaranteed.

*6 : After t_{RC} following Cycle #6, the Configuration Register Verify is completed and returned to the normal operation.

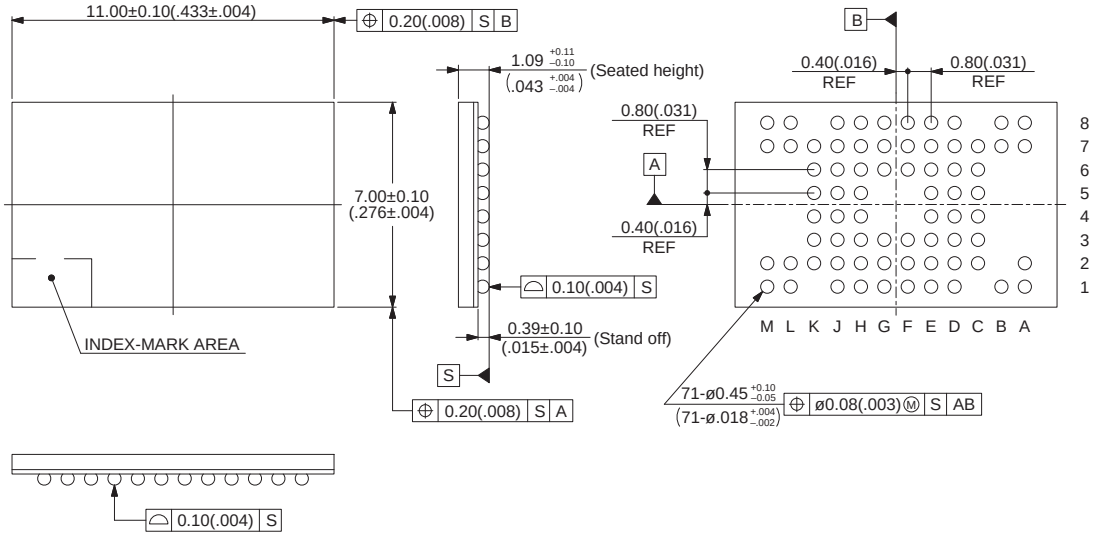
■ ORDERING INFORMATION

Part Number	Package
MB82DBS08164D-70LTBG	71-ball plastic FBGA (BGA-71P-M03)

■ PACKAGE DIMENSIONS

71-ball plastic FBGA		
	Ball pitch	0.80 mm
	Package width × package length	7.00 × 11.00 mm
	Lead shape	Soldering ball
	Sealing method	Plastic mold
	Ball size	∅0.45 mm
	Mounting height	1.20 mm Max.
(BGA-71P-M03)	Weight	0.14 g

71-ball plastic FBGA
(BGA-71P-M03)



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Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest Package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

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