LH5P8129

CMOS 1M (128K × 8)
CS-Control Pseudo-Static RAM

FEATURES

- 131,072 × 8 bit organization
- Access times (MAX.): 60/80/100 ns
- Cycle times (MIN.): 100/130/160 ns
- Power consumption:
  Operating: 572/440/358 mW (MAX.)
  Standby: 275 µW (MAX.) in self-refresh mode
- CS Control Type
  CS Standby Mode Available
- TTL compatible I/O
- Available for auto-refresh and self-refresh modes
- 512 refresh cycles/8 ms
- Packages:
  32-pin, 600-mil DIP
  32-pin, 525-mil SOP
  32-pin, 8 × 20 mm^2 TSOP (Type I)
  (normal and reverse bend pins)

DESCRIPTION

The LH5P8129 is a 1M bit Pseudo-Static RAM organized as 131,072 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

A PSRAM uses on-chip refresh circuitry with a DRAM memory cell for pseudo static operation which eliminates external clock inputs, while considering the pinout compatibility with industry standard SRAMs. The advantage is the cost savings realized with the lower cost PSRAM.

The LH5P8129 PSRAM has the ability to fill the gap between DRAM and SRAM by offering low cost, low power standby and a simple interface.

PIN CONNECTIONS

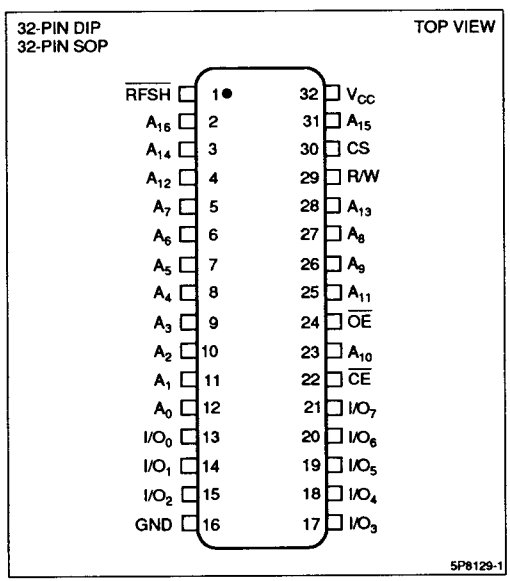


Figure 1. Pin Connections for DIP and SOP Packages

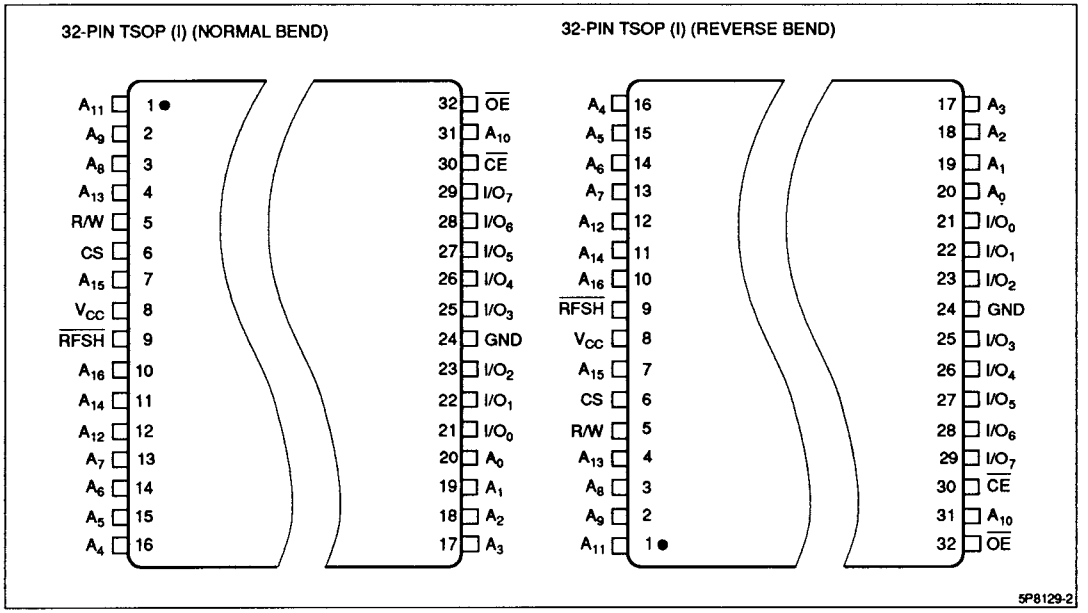


Figure 2. Pin Connections for TSOP Packages

TRUTH TABLE

$\overline{CE}$	CS	$\overline{OE}$	R/W	$\overline{RFSH}$	A_0 - A_{16}	I/O_1 - I/O_8	MODE
L	H	L	H	H	VX	D_{OUT}	Read
L	H	X	L	H	VX	D_{IN}	Write
L	H	H	H	H	VX	High-Z	$\overline{CE}$ only refresh
L	L	X	X	X	X	High-Z	CS standby
H	X	X	X	L	X	High-Z	Auto/Self refresh
H	X	X	X	H	X	High-Z	Standby

NOTES:

H = High at V_{IN} = VCC + 0.3 V to V_{IH} (MIN.)

L = Low at V_{IN} = V_{IL} (MAX.) to -1.0 V

X = Don't care at V_{CC} + 0.3 V to -1.0 V

VX = Input when $\overline{CE}$ = L, then Don't Care

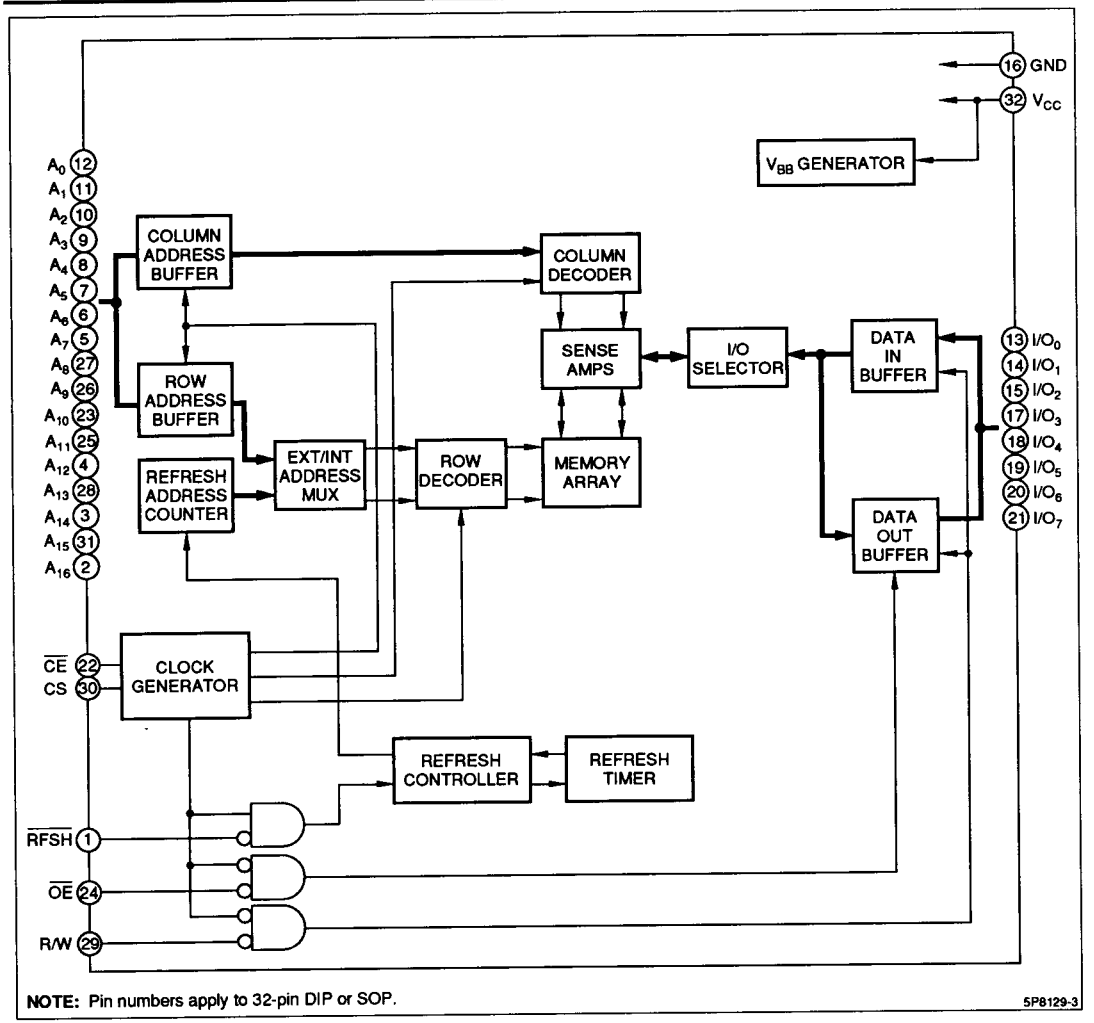


Figure 3. LH5P8129 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{16}	Address input
R/W	Read/Write input
$\overline{OE}$	Output Enable input
$\overline{CE}$	Chip Enable input

SIGNAL	PIN NAME
CS	Chip Select input
$\overline{RFSH}$	Refresh input
I/O_0 - I/O_7	Data input/output

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Applied voltage on any pins	V_T	-1.0 to +7.0	V	1
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	
Output short circuit current	I_O	50	mA	
Power consumption	P_D	600	mW	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input voltage	V_{IH}	2.4		V_{CC} + 0.3	V
	V_{IL}	-1.0		0.8	V

CAPACITANCE (T_A = 0 to +70°C, f = 1MHz, V_{CC} = 5.0 V ± 10%)

PARAMETER		SYMBOL	MIN.	MAX.	UNIT
Input capacitance	A_0 - A_{16}	C_{IN1}		8	pF
	R/W, $\overline{OE}$	C_{IN2}		5	pF
	$\overline{CE}$, CS	C_{IN3}		5	pF
	$\overline{RFSH}$	C_{IN4}		5	pF
Input/output capacitance	I/O_0 - I/O_7	C_{OUT1}		10	pF

DC CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 5.0 V ± 10%)

PARAMETER		SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Operating current	LH5P8129-60	I_{CC1}	tRC = t_{RC} (MIN)		104	mA	1, 2
	LH5P8129-80				80		
	LH5P8129-10				65		
Standby current	TTL Input	I_{CC2}			1	mA	1, 3
	CMOS Input				0.05		1, 4
Self-refresh average current	TTL Input	I_{CC3}			1	mA	1, 5
	CMOS Input				0.05		1, 6
CPU internal cycle average current	LH5P8129-60	I_{CC4}	(R/W = $\overline{OE}$ = V_{IH})		104	mA	1, 2
	LH5P8129-80				80		
	LH5P8129-10				65		
Input leakage current		I_{LI}	0 V ≤ V_{IN} ≤ 6.5 V 0 V on all other test pins	-10	10	µA	
I/O leakage current		I_{LO}	0 V ≤ V_{OUT} ≤ V_{CC} + 0.3 V Output in high-impedance state	-10	10	µA	
Output HIGH voltage		V_{OH}	I_{OUT} = 1 mA	2.4		V	
Output LOW voltage		V_{OL}	I_{OUT} = 4 mA		0.4	V	

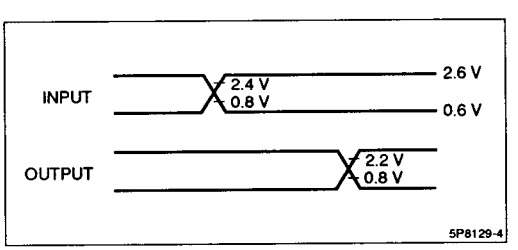
NOTES:
1. The output pins are in high-impedance state
2. I_{CC1} and I_{CC4} depend on the cycle time
3. $\overline{CE}$ = V_{IH}, $\overline{RFSH}$ = V_{IH}
4. $\overline{CE}$ = V_{CC} - 0.2 V, $\overline{RFSH}$ = V_{CC} - 0.2 V
5. $\overline{CE}$ = V_{IH}, $\overline{RFSH}$ = V_{IL}
6. $\overline{CE}$ = V_{CC} - 0.2 V, $\overline{RFSH}$ = 0.2 V

AC ELECTRICAL CHARACTERISTICS [1,2,3] (T_A = 0 to +70°C, V_{CC} = 5.0 V ± 10%)

PARAMETER	SYMBOL	LH5P8129-60		LH5P8129-80		LH5P8129-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random read, write cycle time	t_{RC}	100		130		160		ns	
Read modify write cycle time	t_{RMW}	155		195		235		ns	
$\overline{CE}$ pulse width	t_{CE}	60	10,000	80	10,000	100	10,000	ns	
$\overline{CE}$ precharge time	t_P	30		40		50		ns	
Address setup time	t_{AS}	0		0		0		ns	4
Address hold time	t_{AH}	15		20		25		ns	4
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time	t_{RCH}	0		0		0		ns	
$\overline{CE}$ access time	t_{CEA}		60		80		100	ns	5
$\overline{OE}$ access time	t_{OEA}		25		30		35	ns	5
$\overline{CE}$ to output in Low-Z	t_{CLZ}	20		20		20		ns	
$\overline{OE}$ to output in Low-Z	t_{OLZ}	0		0		0		ns	
Output enable from end of write	t_{WLZ}	0		0		0		ns	
Chip disable to output in High-Z	t_{CHZ}		20		25		30	ns	
Output disable to output in High-Z	t_{OHZ}		20		25		30	ns	
Write enable to output in High-Z	t_{WHZ}		20		25		30	ns	
$\overline{OE}$ setup time	t_{OES}	0		0		0		ns	
$\overline{OE}$ hold time	t_{OEH}	10		10		10		ns	
CS setup time	t_{CSS}	0		0		0		ns	
CS hold time	t_{CSH}	15		20		25		ns	
Write command pulse width	t_{WP}	30		30		30		ns	
Write command setup time	t_{WCS}	30		30		30		ns	
Write command hold time	t_{WCH}	40		50		60		ns	
Data setup time from write	t_{DSW}	25		30		35		ns	6
Data setup time from $\overline{CE}$	t_{DSC}	25		30		35		ns	6
Data hold time from write	t_{DHW}	0		0		0		ns	6
Data hold time from $\overline{CE}$	t_{DHC}	0		0		0		ns	6
Transition time (rise and fall)	t_T	3	35	3	35	3	35	ns	
Refresh time interval	t_{REF}		8		8		8	ms	
Refresh command hold time	t_{RHC}	15		15		15		ns	
Auto refresh cycle time	t_{FC}	100		130		160		ns	
Refresh delay time from $\overline{CE}$	t_{RFD}	30		40		50		ns	
Refresh pulse width (Auto refresh)	t_{FAP}	30	8,000	30	8,000	30	8,000	ns	
Refresh precharge time (Auto refresh)	t_{FP}	30		30		30		ns	
Refresh pulse width (Self refresh)	t_{FAS}	8,000		8,000		8,000		ns	
$\overline{CE}$ delay time from refresh precharge (Self refresh)	t_{FRS}	140		160		190		ns	

NOTES:

1. In order to initialize the circuit, $\overline{CE}$ should be kept in V_{IH} for 100 µs after power-up.
2. AC characteristics are measured at t_T = 5 ns.
3. AC characteristics are measured at the following condition (see figure at right).
4. Address is latched at the negative edge of $\overline{CE}$.
5. Measured with a load equivalent to 2TTL + 100 pF.
6. Data is latched at the positive edge of W/R or at the positive edge of $\overline{CE}$.



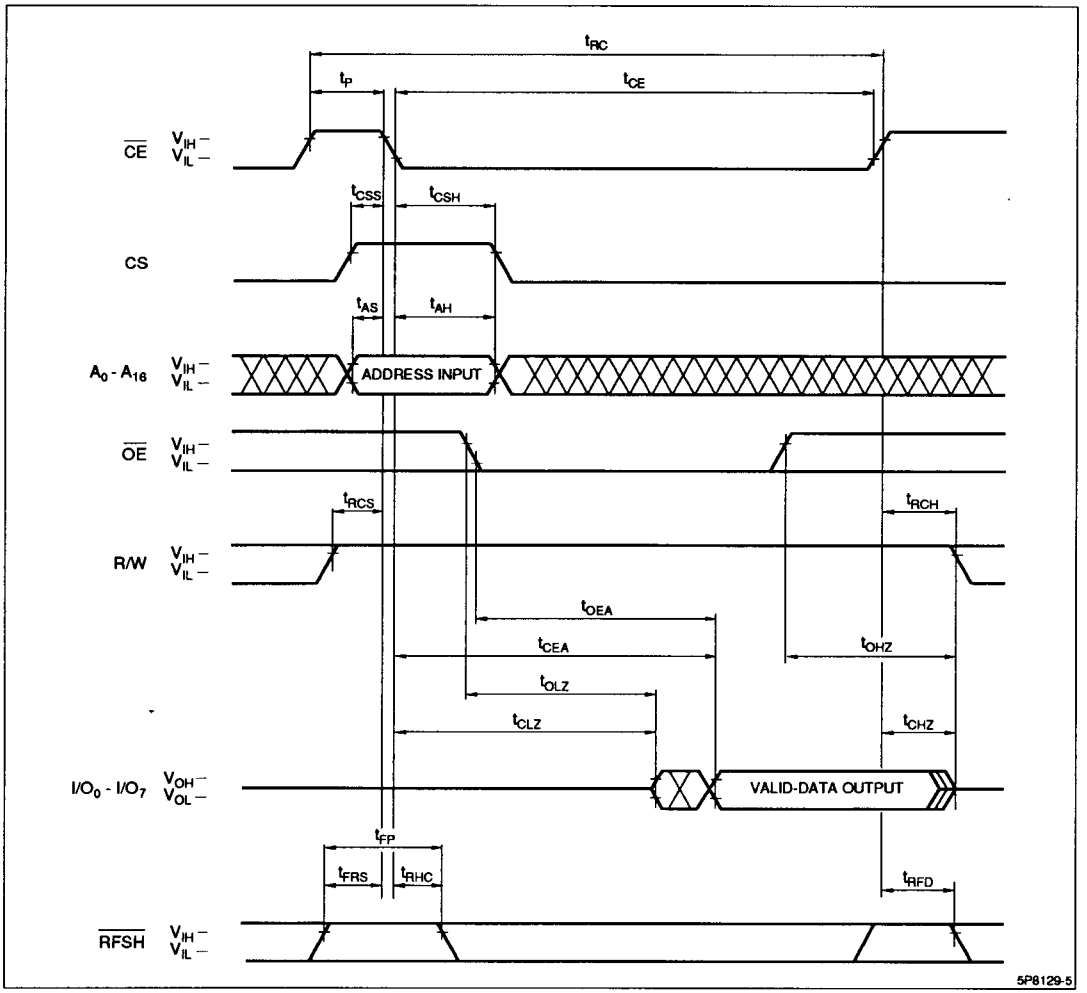


Figure 4. Read Cycle

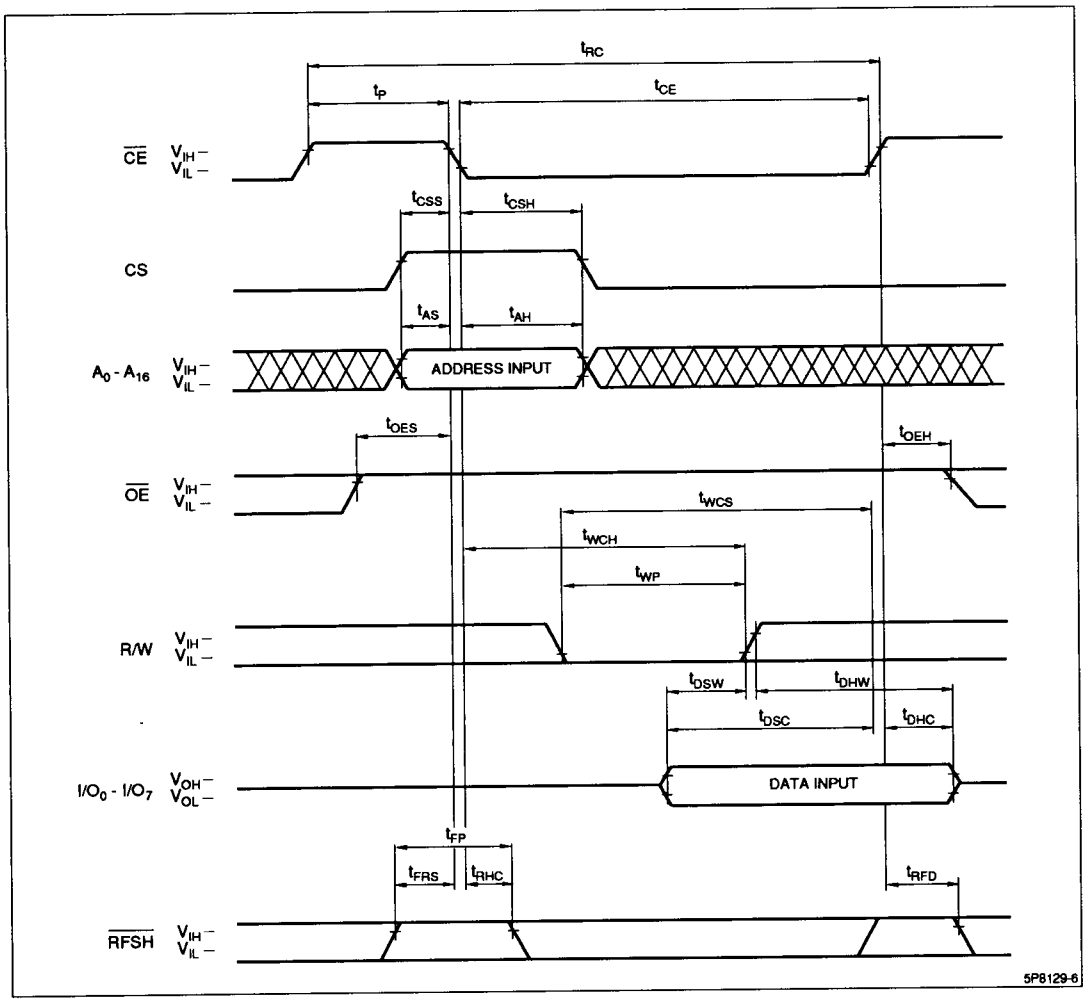


Figure 5. Write Cycle 1 ($\overline{OE}$ = HIGH)

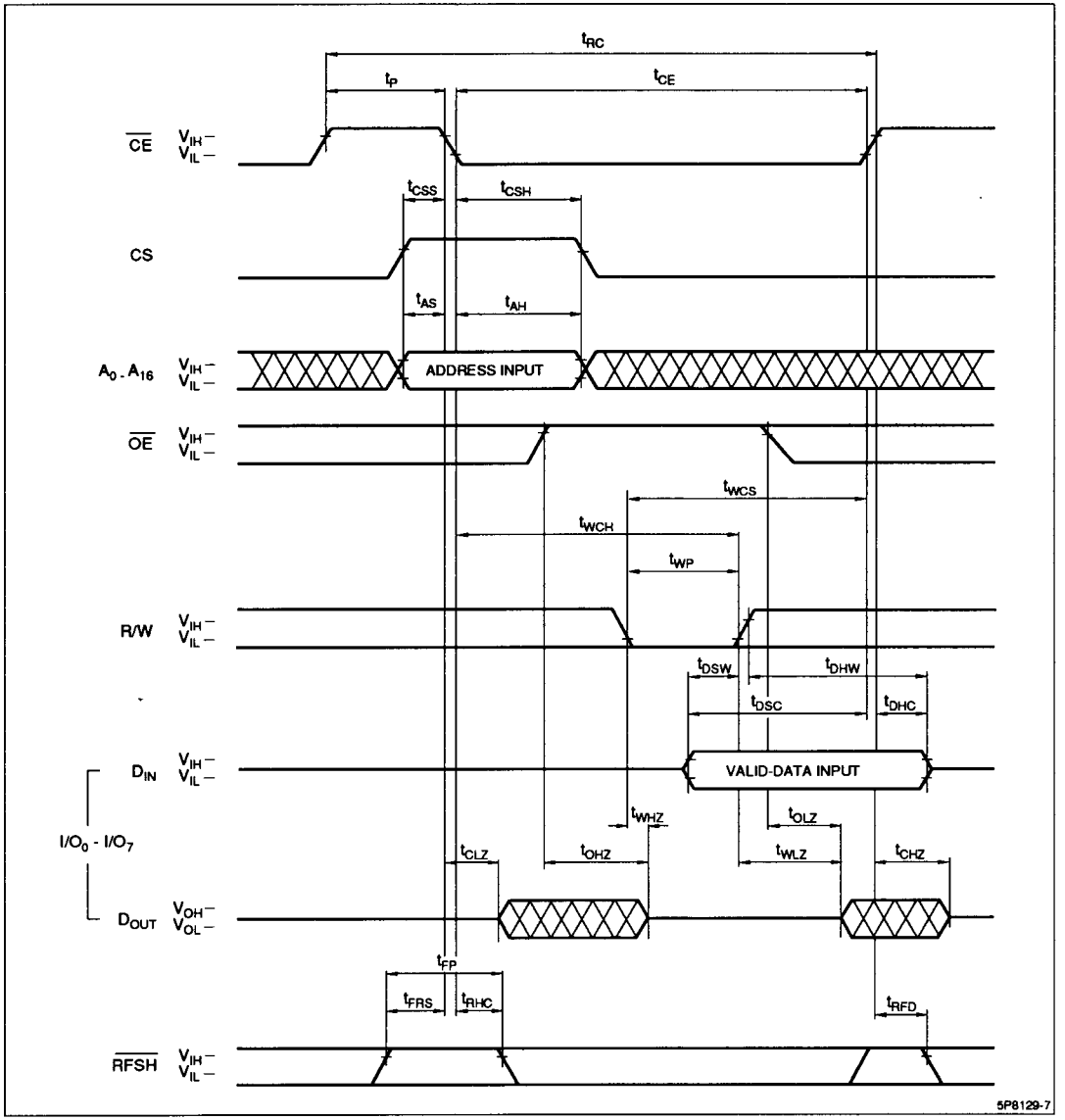


Figure 6. Write Cycle 2 ($\overline{OE}$ Clock)

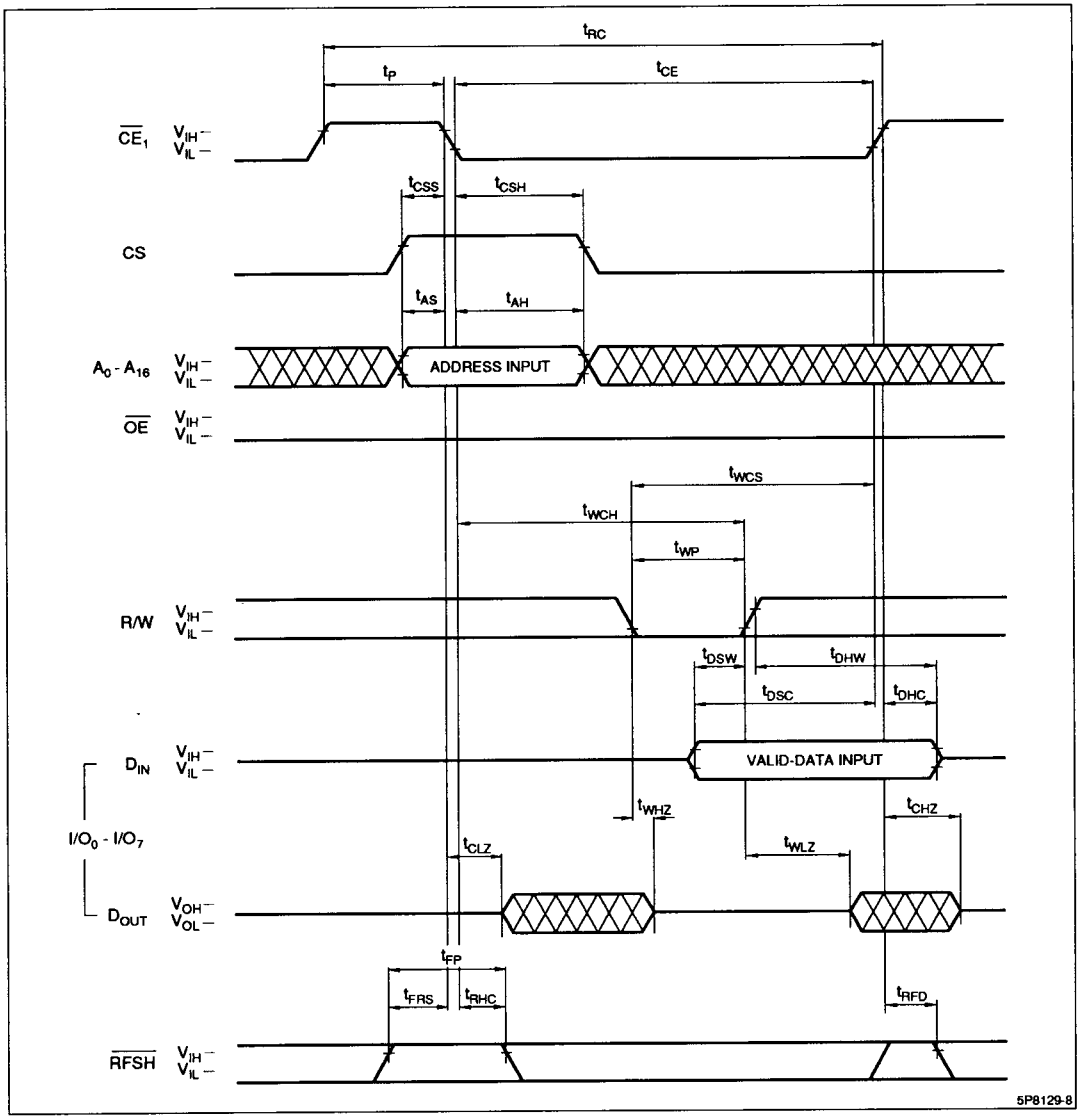


Figure 7. Write Cycle 3 ($\overline{OE}$ = LOW)

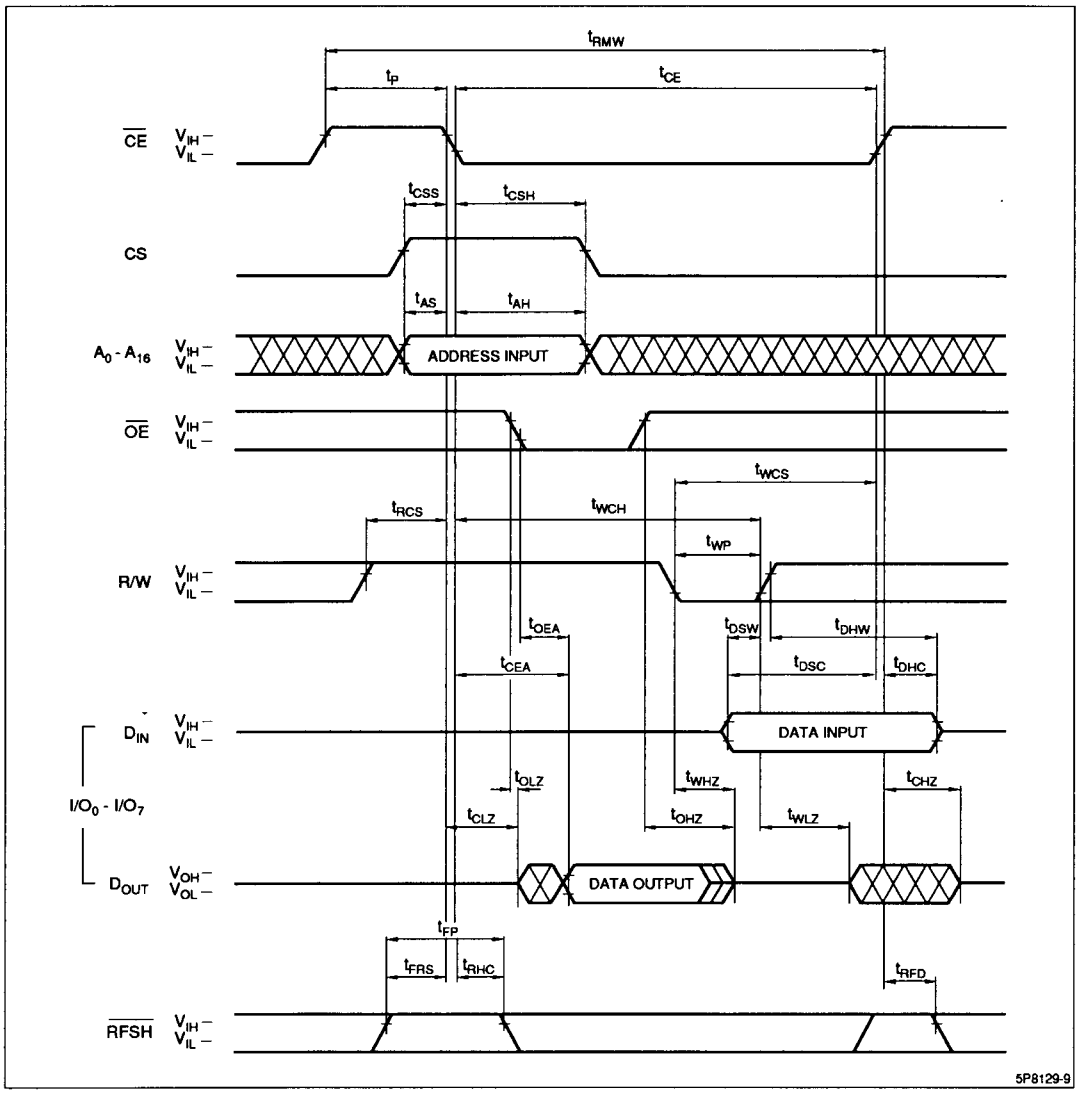


Figure 8. Read-Modify-Write Cycle

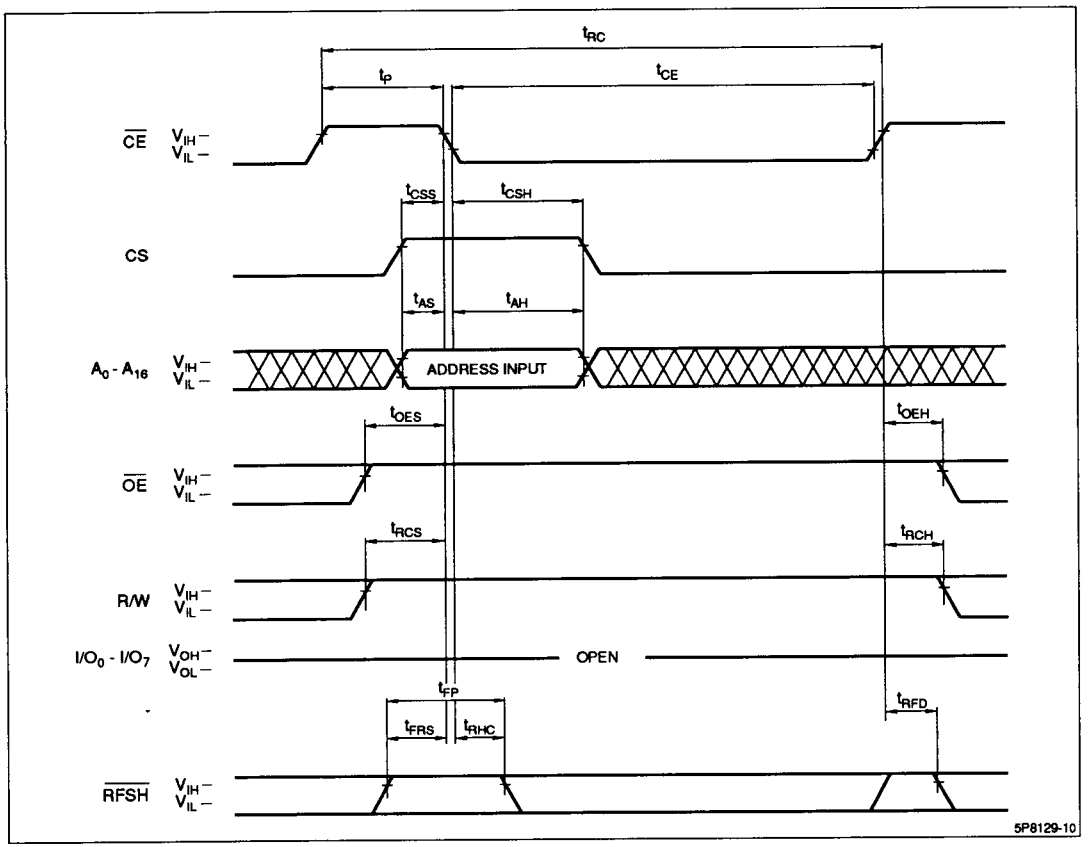


Figure 9. $\overline{CE}$ Only Refresh

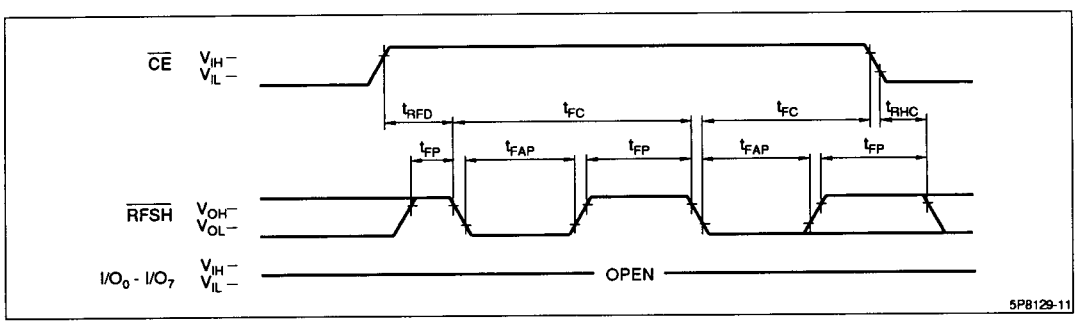


Figure 10. Auto Refresh Cycle

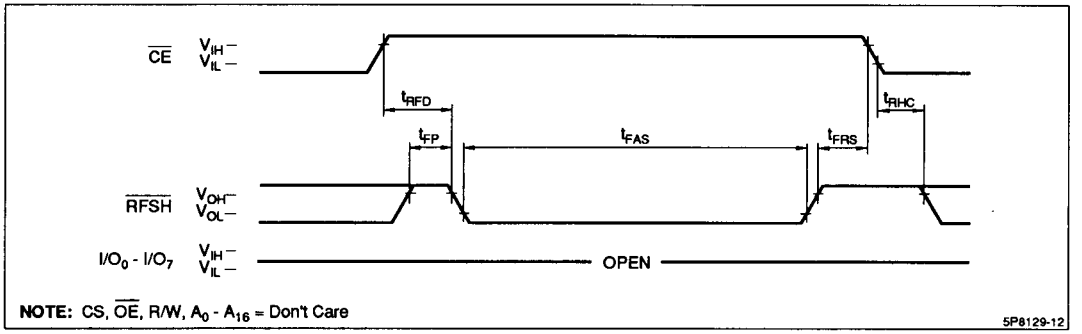


Figure 11. Self Refresh Cycle

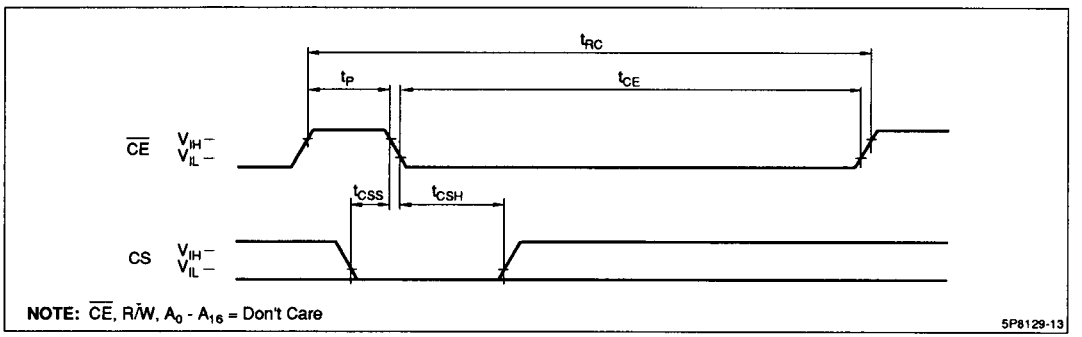


Figure 12. CS Standby Mode

ORDERING INFORMATION